UNITRODE

UCC2585
UCC3585
PRELIMINARY

Low Voltage Synchronous Buck Controller

FEATURES

- Resistor Programmable 1.25V to 4.5V V_{OUT}
- 2.5V to 6V Input Supply Range
- 1% DC Accuracy
- High Efficiency Synchronous Switching
- Drives P-channel (High Side) and N-channel (Low Side) MOSFETs
- Lossless Programmable Current Limit
- Logic Compatible Shutdown
- Programmable Frequency
- Start-up Voltage Tracking Protects Dual Rail Microprocessors

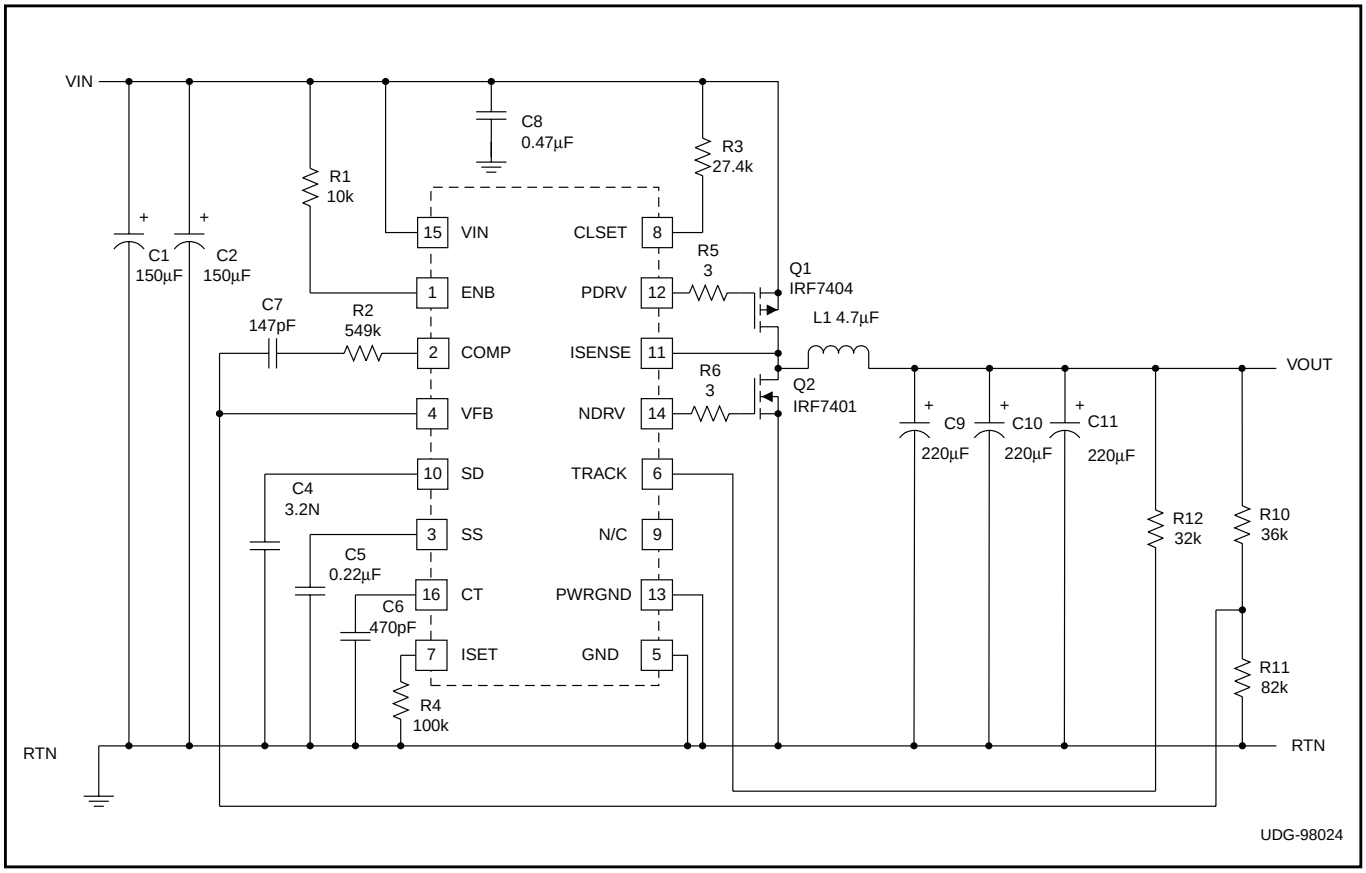
DESCRIPTION

The UCC2585/UCC3585 synchronous Buck controller provides flexible high efficiency power conversion for output voltages as low as 1.25V with guaranteed ±1% DC accuracy. Output currents are only limited by the choice of external logic level MOSFETs. With an input voltage range of 2.5V to 6.0V it is the ideal choice for 3.3V only, battery input, or other low voltage systems. Applications include local microprocessor core voltage power supplies for desktop and Notebook computers, and high speed GTL bus regulation. Its fixed frequency oscillator is capable of providing practical PWM operation to 700kHz.

With its low voltage capability and inherent “always on” operation, the UCC2585/UCC3585 causes VOUT to track VIN once VIN has exceeded the threshold voltage of the external P channel MOSFET. Tracking can be tailored for any application with a single resistor or disabled by connecting TRACK to VIN. For dual supply rail microprocessors this feature negates the need for external diodes to insure supply voltage tracking between the +3.3V and lower voltage microprocessor core supplies.

(continued)

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Analog Pins
Minimum and Maximum Forced Voltage
(Reference to GND) . . . . . –0.3V to +6.3V
Digital Pins
Minimum and Maximum Forced Voltage
(Reference to GND) . . . . . .–0.3V to 6.3V
Power Driver Output Pins
Maximum forced current . . . . . ±1.0A
Operating Junction Temperature . . . . . –55°C to +125°C
Storage Temperature. . . . . –65°C to +150°C

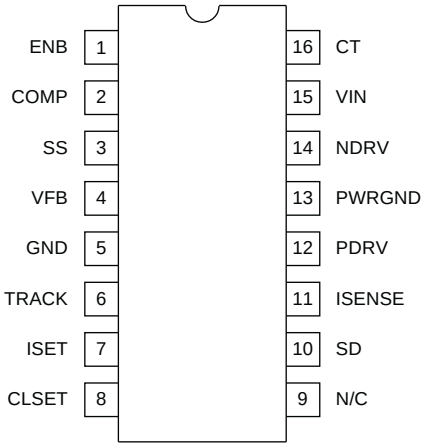
Note: *Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns.*

APPLICATIONS

- Low Voltage Microprocessor Power such as PowerPC 603 and 604
- High Power 5V or 3.3V to 1.25V–4.5V Regulators
- GTL Bus Termination

CONNECTION DIAGRAMS

DIL-16, SOIC-16, SSOP-16 (TOP VIEW)
J, N, D, and M Packages



DESCRIPTION (cont.)

The UCC2585/UCC3585 drives a complementary pair of power MOSFET transistors, P-channel on the high side, and N-channel on the low side to step down the input voltage at up to 90% efficiency.

A programmable two-level current limiting function is provided by sensing the voltage drop across the high side P channel MOSFET. This circuit can be configured to provide pulse-by-pulse limiting, timed shutdown after 7 consecutive faults, or latch-off after fault detection, allowing maximum application flexibility. The current limit threshold is programmed with a single resistor selected to match system MOSFET characteristics.

The UCC2585/UCC3585 also includes undervoltage lockout, a logic controlled enable, and softstart functions. The UCC2585/UCC3585 is offered in the 16 pin surface mount and through hole packages.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3585, and T_A = –40°C to 85°C for the UCC2585. $T_A = T_J$. VIN = 3.3V, ENB, $I_{SENSE} = V_{IN}$, V_{FB} = 1.25V, COMP = 1.5V, C_T = 330pF, R_{ISET} = 100k, RTRACK = 10k, RCLSET = 10k.

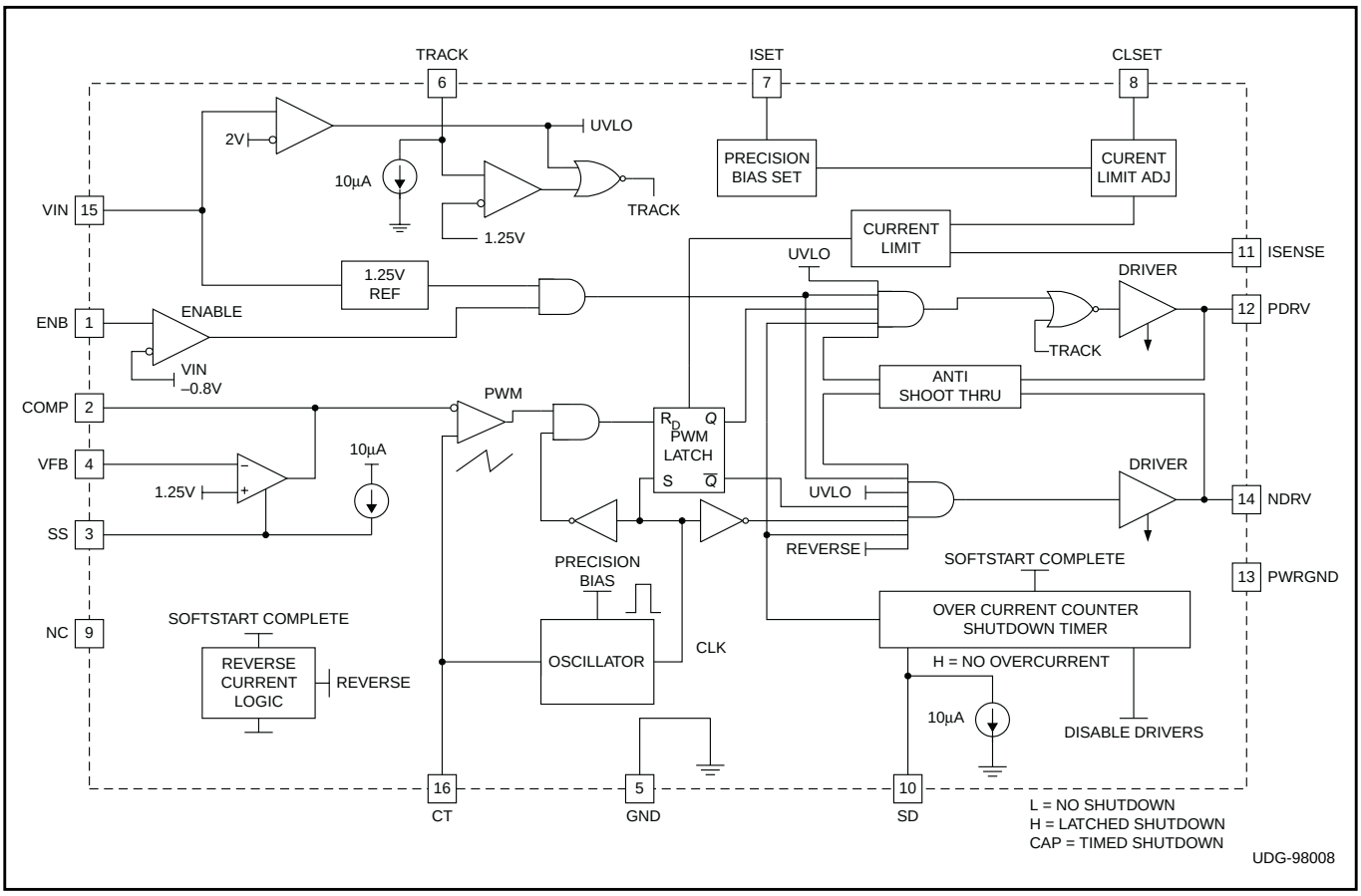
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Section					
Supply Current – Total (Active)			2.3	3.5	mA
Supply Current – Shutdown	ENABLE = 0V		10	25	µA
VIN Turn On Threshold (UVLO)			2.35	2.60	V
VIN Turn On Hysteresis			450	550	mV
Voltage Amplifier Section					
Input Voltage (Internal Reference)	T_A = 0°C to 70°C, VIN = 3.0V to 3.6V, Note 1	1.238	1.250	1.262	V
Input Voltage (Internal Reference)	VIN = 3.0V to 3.6V, IND/MIL Temp, Note 1	1.228	1.250	1.273	V
Open Loop Gain	COMP = 0.5 to 2.5V	65	80		dB
Output Voltage High	I(COMP) = –50µA	3.00	3.25		V
Output Voltage Low	I(COMP) = 50µA		0.10	0.25	V
Output Source Current		–100	–175		µA
Output Sink Current		0.4	1.0		mA
Oscillator/PWM Section					
Initial Accuracy	T_J = 25°C	405	450	495	kHz
Initial Accuracy	Over Temperature	390	450	510	kHz
CT Ramp Peak to Valley		1.8	2.1	2.4	V
CT Ramp Valley Voltage		0.3	0.4		V
PWM Maximum Duty Cycle	COMP = 3V, Measured on PDRV	100			%
PWM Minimum Duty Cycle	COMP = 0.2V, Measured on PDRV			0	%
PWM Delay to Outputs	COMP = 2.5V		45		ns
Tracking Current	Measured on TRACK, V_{TRACK} = 1.6V	10	12	15	µA
Enable High Threshold	Measured on ENABLE (Note 3)		2.8		V
Enable Low Threshold	Measured on ENABLE		0.5		V
Softstart Charge Current	SS = 0V	–10	–14	–18	µA
Current Limit Section					
Pulse to Pulse Threshold	Measured Between V_{IN} and I_{SENSE}	100	125	150	mV
CLSET Current		11	14	16	µA
SD Sink Current	SD = 2V	8	13	18	µA
SD Source Current	SD = 2V		–100	–140	µA
Restart Threshold	Measured on SDOWN	0.40	0.55	0.90	V
Output Driver Section (PDRV, NDRV)					
Pull Up Resistance	–100mA (Source) T_A = 25° C		6		Ω
Pull Down Resistance	100mA (Sink) T_A = 25° C		4		Ω
Deadtime Delay	Note 2	150	200	250	ns

Note 1. Measured on COMP with the Error Amp in a Unity Gain (voltage follower) configuration.

Note 2. 50% point of PDRV Rise to NDRV Rise and 50% point of NDRV Fall to PDRV Fall.

Note 3. Enable High Threshold = V_{IN} –0.5.

BLOCK DIAGRAM



PIN DESCRIPTIONS

CLSET: CLSET is used to program the pulse by pulse and overcurrent shutdown levels for the UCC1585. A resistor is connected between CLSET and VIN to set the thresholds. The threshold follows the following relationship:

$$Icl = \frac{\frac{1.25}{R_{ISET}} \bullet R_{CLSET}}{RDS(on)}$$

COMP: Output of the Voltage type error amplifier. Loop compensation components are connected between COMP and VFB.

CT: A high quality ceramic capacitor connected between this pin and ground sets the PWM oscillator frequency by the following relationship:

$$F = \frac{1}{(6700 \bullet CT)}$$

Use capacitor values greater than 100pF in order to minimize the effects of stray capacitance. The oscillator is capable of reliable operation in excess of 1MHz.

ENB: A LOGIC1 (V_{IN}–0.5V) on this input will activate the Output drivers. A logic zero (0.5V) will prevent switching of the output drivers. Do not allow ENB to remain between these levels steady state.

GND: Reference level for the IC. All voltages and currents are with respect to GND.

ISENSE: ISENSE performs two functions. The first is to monitor the voltage dropped across the high side P channel MOSFET switch while it is conducting. This information is used to detect over current conditions by the current limit circuitry. The second function of ISENSE is to measure current through the lowside N-channel MOSFET. When the current flow through this MOSFET is drain to source, (i.e. reversed), this FET is turned off for the remainder of the switching cycle.

PIN DESCRIPTIONS (cont.)

ISET: A resistor is connected between ISET and ground to program a precision bias for many of the UCC2585/UCC3585 circuit blocks. Allowable resistor values are 90kΩ to 110kΩ. 1.25V is provided to ISET via a buffered version the internal bandgap voltage reference. The resultant current is 1.25V / R_{ISET}.This current is mirrored directly over to CLSET to program the over current thresholds. A second use for this current is to set a basis for the charging current of the oscillator.

PDRV: High current driver output for the high side P channel MOSFET switch. A 3Ω to 10Ω series resistor between PDRV and the MOSFET gate may be inserted to reduce ringing on this pin. In some layout situations, a low V_F diode may be required from this pin to ground to keep the pin from ringing more than 0.5V below ground.

PWRGND: High current return path for the MOSFET drivers. PWRGND and GND should be terminated together as close to the IC package as possible.

SD: This pin can configure current limit to operate in any one of three different ways.

1) A forced voltage of less than 250mV on SD inhibits the shutdown function causing pulse by pulse limiting.

2) A capacitor from SD to GND provides a controller-converter shutdown timeout after 7 consecutive overcurrent signals are received by the current limit circuitry. An interval 10μA (typ) current source discharges the SD capacitor to the 0.5V (typ) restart threshold. The shutdown time is given by:

$$T_{SHUT} = \frac{[C_{SD} \bullet (V_{IN} - 0.5)]}{10\,\mu A},$$

where C_{SD} is the value of the capacitor from SD to GND, and VIN is the chip supply voltage (on pin 15). At this point, a softstart cycle is initiated, and a 100μA current (typ) quickly recharges SD to VIN. During softstart, pulse by pulse limiting is enabled, and the 7 cycle count is delayed until softstart is complete (i.e. charged to approximately VIN volts).

3) A forced voltage of greater than 1V on SD will cause the UCC2585/UCC3585 to latch OFF after 7 overcurrent signals are received. After the controller is latched off, SD must drop below 250mV to restart the controller.

SS: A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor will slowly charge on start-up via an internal current source. The output of the Voltage error amplifier (COMP) tracks this voltage thereby limiting the controller duty ratio.

NDRV: High current driver output for the low side MOSFET switch. A 3Ω to 10Ω series resistor between NDRV and the MOSFET gate may be inserted to reduce ringing on this pin. In some layout situations, a low V_F diode may be required from this pin to ground to keep the pin from ringing more than 0.5V below ground.

TRACK: A resistor is connected between TRACK and output voltage of the converter to set the start-up profile of the power converter. Certain dual supply rail microprocessors require that a maximum voltage differential between the supply rails is not exceeded. Failure to do so results in large currents in the microprocessor through the ESD (electrostatic discharge) protection devices. This can result in chip failure. The UCC2585/UCC3585 is designed such that it is “normally on” before V_{IN} reaches the 2.0V (nom.) UVLO threshold. That is, the high side P channel MOSFET switch driver output is actively held low allowing the MOSFET to conduct current to the output as soon as V_{IN} is high enough to exceed the gate turn on threshold. The resistor from TRACK to V_{OUT} sets the voltage level on VOUT at which the P channel MOSFET is turned off. The tracking cutoff voltage follows the following relationship:

$$V_{OUT}(\max) = 1.25\,V + 12\,\mu A \bullet (R_{TRACK})$$

This is necessary for very low output voltage applications (< 2.0V), where overvoltage may occur if the Pchannel MOSFET is not disabled before the UVLO threshold is reached. For applications with V_{OUT} greater than 2.0V, TRACK can be disabled by tying TRACK to V_{IN}.

VFB: Inverting input to the Voltage type error amplifier. The common mode input range for VFB extends from GND to 1.5V.

VIN: Supply voltage for the UCC2585/UCC3585.Bypass with a 0.1μF ceramic capacitor (minimum) to supply the switching transient currents required by the external MOSFET switches.

APPLICATION INFORMATION

Some of today's microprocessors require very low operating voltages. In some cases, as low as 1.8V of supply voltage are required in addition to already available 3.3V system voltage. Following is an illustration of a design using the UCC3585 as the power controller.

The design criteria are as follows:

- Input Voltage (V_{IN}) 3.3V DC
- Output Voltage (V_{OUT}) 1.8V DC
- Output Ripple Voltage (V_{OUT}) 18mV
- Output Current (I_{OUT}) 3.5A DC

Other features include

- Output Tracking
- Switching Frequency (F_S) 350kHz
- 100% Surface Mount

The first few steps in the design are to define the power stage (Schematic Fig. 1).

1) The normal operating duty cycle (δ) of the regulator is approximately

$$\delta = \frac{V_{OUT}}{V_{IN}} = \frac{1.8}{3.3} = 0.545$$

2) Select the output inductor to meet ripple current requirements. For this design, the allowable ripple current in the output inductor is selected to be 10% of the full load output current.

$$L1 = \frac{(V_{IN} - V_{OUT}) \bullet \delta}{F_S \bullet 0.1 \bullet I_{OUT}} = 4.6\,\mu H$$

A Pulse Engineering SMT inductor (PE-53682) is 4.7µH has a DC resistance (R_{L1}) of 8.3mΩ and will dissipate 0.1W under full load operation.

The resulting ΔI_{OUT} is now:

$$\Delta I_{OUT} = \frac{(V_{IN} - V_{OUT})}{4.7 \bullet 10^{-6}} \bullet \frac{\delta}{F_S} = 0.5\,A$$

3) Next, the output capacitors are determined based upon the output ripple criteria. Assuming the ripple is limited by the equivalent series resistance, or ESR, of the capacitors and not the impedance of the capacitors at the switching frequency, then the output capacitor selection is based upon ESR, size and voltage considerations.

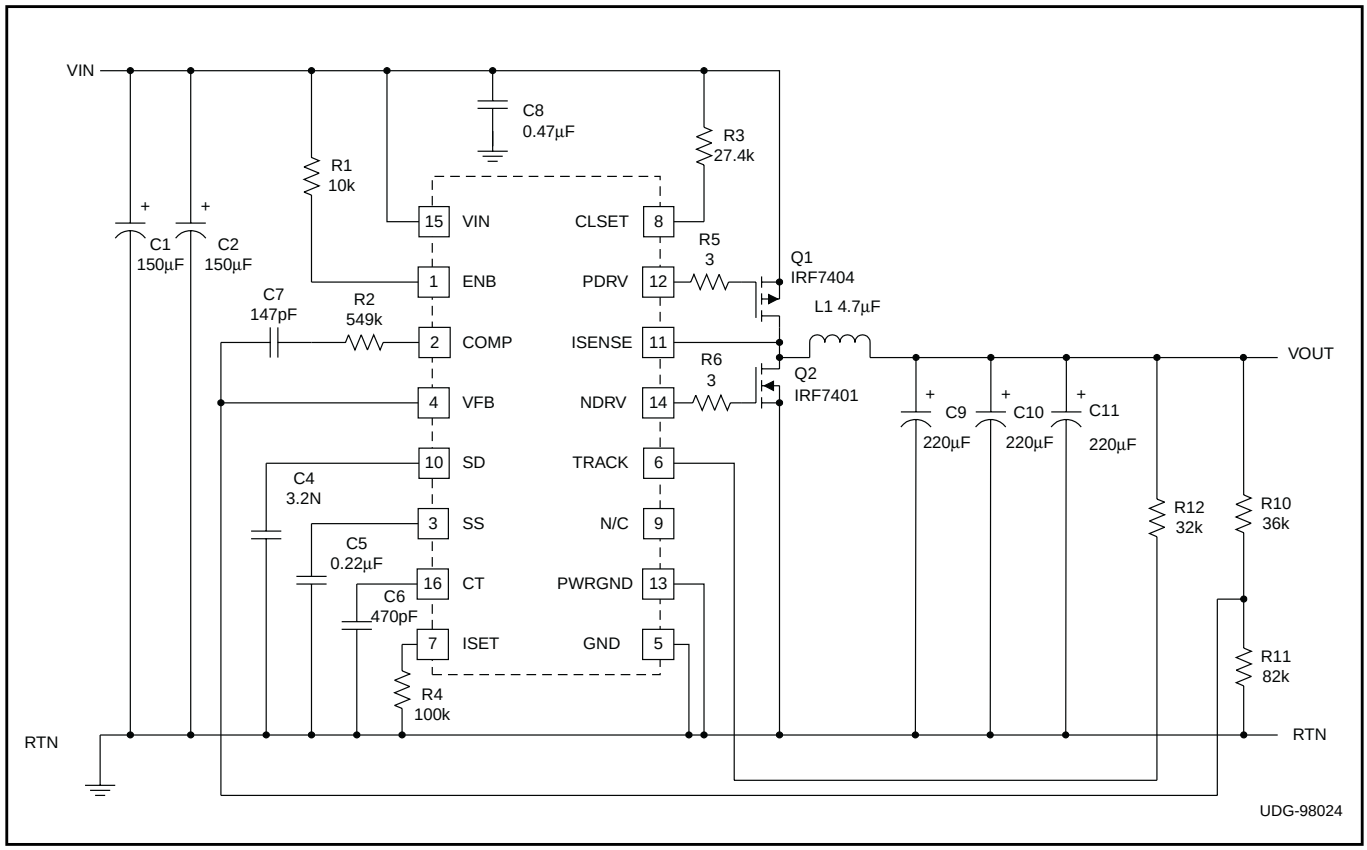


Figure 1. Application circuit schematic.

APPLICATION INFORMATION (cont.)

$$ESR = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{0.018}{0.5} = 0.026\,\Omega$$

A 220µF, 6.3V Sprague 594D capacitor has an ESR of 75mΩ. Three of these in parallel will result in an overall ESR of 25mΩ (C9, C10, and C11 in Fig. 1). Since the output ripple current is so low, the capacitor's ripple current rating of 1.45A is not a concern.

To check the assumption that the capacitor's impedance at the switching frequency is dominated by the ESR and not the capacitor's capacitance value, calculate the impedance and compare it to the ESR.

$$Z_C = \frac{1}{2\pi \bullet F_S \bullet C} = \frac{1}{2\pi \bullet 350k \bullet 220\,\mu} = 2m\Omega$$

The ESR of the capacitor is 37 times that of the impedance of the capacitor at the switching frequency, so the earlier assumption was valid.

4) Before selecting the switching MOSFETs, the current that will be flowing through them must first be determined.

$$I_{D_{PK}} = I_{OUT} + \frac{\Delta I_{OUT}}{2} = 3.8\,A$$

The RMS of this current in Q1 is

$$I_D Q1_{RMS} = I_{D_{PK}} \sqrt{\delta} = 2.8\,A$$

And in Q2

$$I_D Q2_{RMS} = I_{D_{PK}} \sqrt{1-\delta} = 2.5\,A$$

5) Since this regulator must be able to operate from a 3.3V source, the MOSFETs used must have a gate threshold level of no more than 2V.

For Q1, an IRF7404 is selected. It has an $R_{DS(on)}$ of 0.04Ω, a total gate charge (Q_G1) of 50nC, and a turn OFF ($t_{OFF}1$) time of 65ns. The conduction loss in Q1 will be:

$$P_D Q1_{ON} = I_D Q1_{RMS}{}^2 \bullet R_{DS_{ON}} Q1 = 0.593\,W$$

The gate drive losses will be

$$P_D Q1_{GATE} = Q_{G_1} \bullet V_{IN} \bullet F_S = 58\,mW$$

And finally the turn OFF losses are estimated

$$P_D Q1_{OFF} = \frac{1}{2} \bullet V_{IN} \bullet I_D Q1_{PK} \bullet T_{OFF1} \bullet F_S = 0.14W$$

The total power loss for Q1 is the sum of these three:

$$P_D Q1_{TOTAL} = 0.5W$$

6) Q2 has been selected to be an IRF7401, which has an $R_{DS(ON)}$ of 0.03Ω, and a total gate charge (Q_G2) of 48nC and a body diode turn OFF switching time ($t_{OFF}2$) of 59ns. In this topology, the N Channel MOSFET, Q2, is turned OFF prior to the turn ON of Q1, so when Q2 is turned OFF, current is being re-routed from the channel of the device into the intrinsic body diode. Therefore Q2's intrinsic body diode incurs switching loss during the turn OFF interval.

The conduction loss in Q2 is:

$$P_D Q2_{ON} = I_D Q2_{RMS}{}^2 \bullet R_{DS_{ON}} Q2 = 0.2W$$

The gate drive losses will be

$$P_D Q2_{GATE} = Q_{G_2} \bullet V_{IN} \bullet F_S = 55\,mW$$

And the body diode turn OFF loss:

$$P_D Q2_{D\_OFF} = \frac{1}{2} \bullet V_{IN} \bullet I_{D_{PK}} \bullet T_{OFF2} \bullet F_S = 0.13W$$

The total power loss for Q2 is the sum of these three:

$$P_D Q2_{TOTAL} = 0.4W$$

7) Thus far the power loss in the two MOSFETs and the output inductor total 1.0W. The average input current is:

$$I_{IN_{AVG}} = \frac{V_{OUT} \bullet I_{OUT} + P_{LOSS}}{V_{IN}} = 2.2A$$

The peak to peak ripple in the input capacitors is the peak current less the average input current during Q1's ON time, and equal to the average input current during Q1's OFF time. The RMS value of this current is then:

$$I_{IN\_CAP_{RMS}} = \sqrt{(I_{D_{PK}} - I_{IN_{AVG}})^2 \bullet \delta + (I_{IN_{AVG}})^2 \bullet (1-\delta)} = 1.9\,A$$

8) After the input capacitor's input ripple current is known, select the input capacitors. Again, Sprague 594D Solid Tantalum capacitors are chosen. A single 150µF, 10V capacitor has a ripple current rating of 1.35A RMS. Two in parallel (C1 and C2) will have a combined capability of 2.7A, and a total ESR of 40mΩ. The losses in the capacitors are:

$$P_{DIN\_CAP} = I_{IN\_CAP_{RMS}}{}^2 \bullet ESR = 0.14W$$

Adding the capacitor loss to that previously found, the total losses are now 2.1W.

9) The overall efficiency of the power train is then

$$E_{FF} = \frac{V_{OUT} \bullet I_{OUT}}{V_{OUT} \bullet I_{OUT} + 2.1} = 0.84$$

The losses are dominated by the MOSFETs Q1 and Q2. One way to improve the efficiency would be to reduce the conduction loss in Q1, either by choosing a device with a

APPLICATION INFORMATION (cont.)

lower $R_{DS(on)}$ or by paralleling it with another MOSFET. The conduction losses in Q2 may be improved by the same technique, but will prove detrimental in switching losses. To lower the switching losses, Q2 may be paralleled with a Schottky diode. In this manner, the switching loss may be absorbed by the Schottky, instead of the MOSFET.

10) After the power stage design is completed, attention is given to the feedback loop. The LC filter gain is described by the equation (10A) below: (where $\omega = j2\pi f$)

Where C_{OUT} is the combined capacitance of C9, C10, and C11 and R_{ESR} is the ESR of the capacitors.

There will be a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L1 \bullet C_{OUT}}} = 2.8\,kHz$$

and a zero at the point where the impedance of the output capacitors equals the ESR:

$$F_Z = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} = 9.6\,kHz$$

The modulator gain is given by

$$K_{PWM} = \frac{V_{IN}}{V_{RAMP}} = 1.65$$

where V_{RAMP} is the peak to peak amplitude of the oscillator ramp found on the CT pin. The overall open loop gain is shown in Fig. 2.

11) The voltage divider is next determined to give us the proper output voltage. First select one of the divider resistors R11 = 82k. The other resistor becomes:

$$R10 = R11 \bullet \frac{V_{OUT}}{V_{REF}} - R11 = 36\,k$$

12) The equation for the error amplifier in this configuration is:

$$K_{EA} = \frac{\frac{1}{j2\pi \bullet f \bullet C7} + R2}{R10}$$

For a gain of 5 and a zero at 2kHz

$$R2 = 15 \bullet R10 = 180\,k$$

and

$$C7 = \frac{1}{2\pi \bullet fp \bullet R2} = 440\,pF$$

The overall voltage loop gain now has a crossover at 34kHz with a phase margin of about 73 degrees.

13) Select the R_{ISET} resistor, R3, to be 100k. (The range of value should be between 90k and 110k.) Then choosing the current limit trip point to be 130% of I_{OUT}, the current limit set resistor is then found by the relationship

$$R3 = \frac{1.3 \bullet I_{OUT}}{1.25} \bullet R_{DS(on)}Q1 \bullet R_{ISET} = 27.2k$$

Note that the $R_{DS(on)}$ value used should include the effects of temperature.

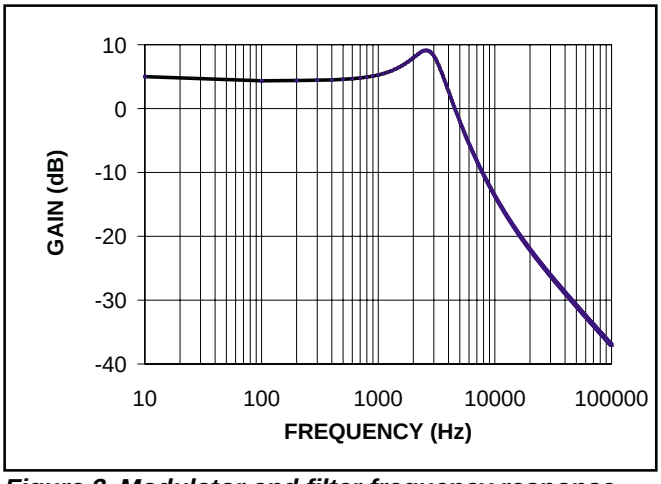


Figure 2. Modulator and filter frequency response.

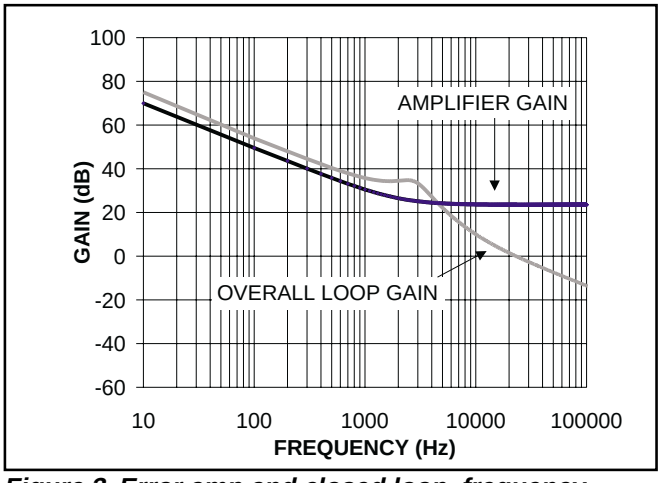


Figure 3. Error amp and closed loop frequency response.

(10A) $$KLC = \frac{1 + \omega \bullet R_{ESR} \bullet C_{OUT}}{1 + \omega^2 \bullet L1 \bullet C_{OUT} + \omega\left(R_{L1} \bullet C_{OUT} + R_{ESR} \bullet C_{OUT} + \frac{L1}{R_{LOAD}}\right)}$$

APPLICATION INFORMATION (cont.)

14) During normal power on of the UCC3585, the gate of Q1 is held low (Q1 turned ON) until the V_{CC} input to the IC reaches the 2V Under Voltage Lockout (UVLO) voltage. At UVLO, the UCC3585 wakes up and switching begins on Q1 and Q2. With a 1.8V output however, the output will reach 2V before regulation begins! This is where the tracking function comes into use. By selecting an appropriate resistive divider from the output, we can select the point below UVLO at which Q1 will be shut off. Upon reaching UVLO, the UCC3585 will then begin to regulate normally.

With a 1.8V nominal output voltage, select the tracking turn off point to be 1.6V.

$$R3 = \frac{1.6 - 1.25}{12\mu} = 29\,k\Omega$$

Note that the tracking function ONLY makes a difference below UVLO. If V_{OUT} were to be 2V or above, then the tracking pin should be tied to V_{IN}.

15) A capacitor on the SD pin will allow the converter to shutdown in the event seven consecutive over current pulses occur. If a timing shutdown interval of 1ms is chosen as the shutdown time, T_{SD}, then the value of the capacitor is:

$$C4 = \frac{T_{SD}}{(V_{IN} - 0.5) \bullet \left(\frac{1}{I_{CHG}} + \frac{1}{I_{DICHG}} \right)} = 3.2nF$$

Where I_{CHG} and I_{DISCHG} are 100µA and 10µA respectfully.

16) The next step is to find the value of timing capacitor.

$$C6 = \frac{T_S}{6000} = 476pF$$

A 470pF capacitor will result in a switching frequency of 354kHz.

17) The softstart capacitor is selected for a 5ms startup time. Knowing that a 10µA current source will charge the capacitor to 2.5V, the softstart capacitor is given by:

$$C5 = \frac{T_{SS} \bullet I_{CHG}}{V_{SS}} = \frac{5m \bullet 10\mu}{2.5} = 20\,nF$$

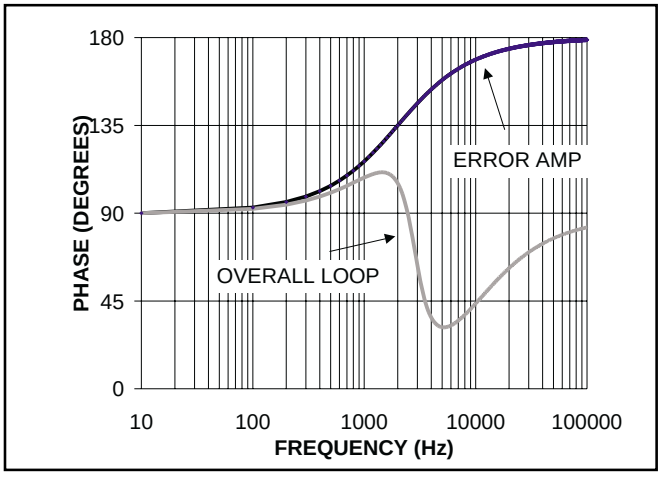


Figure 4. Error amp and closed loop frequency response.

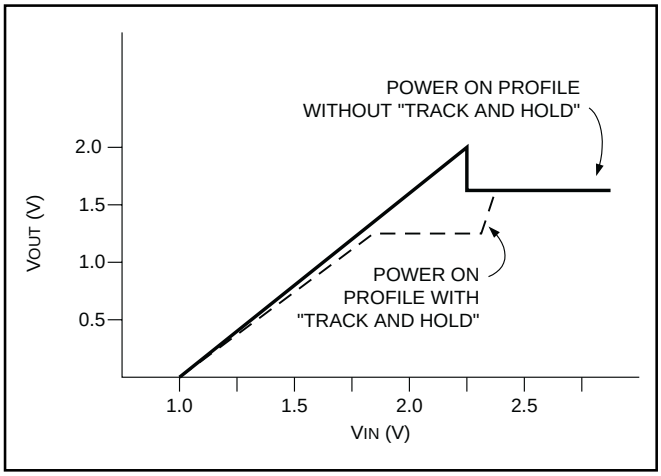


Figure 5. Power on profile.

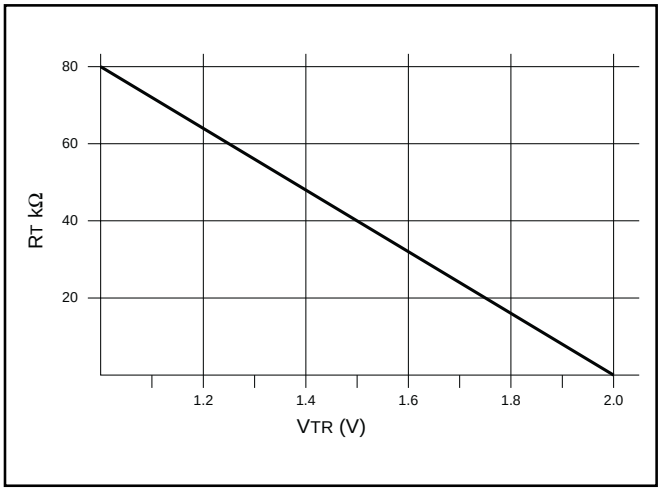


Figure 6. Tracking resistor value as a function of turn off voltage.

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