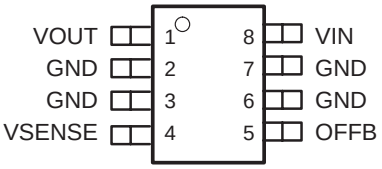
UCC386, UCC387, UCC388
LOW-DROPOUT 200-mA LINEAR REGULATOR

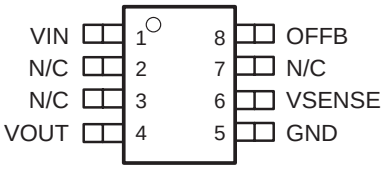
SLUS377B - JULY 1999 - REVISED MAY 2000

- **Precision Positive Linear Voltage Regulator**
- **0.2 V Dropout at 200 mA**
- **Ensured Reverse Input/Output Voltage Isolation with Low Leakage**
- **Adjustable Output Voltage (Down to 1.25 V)**
- **Load Independent Low Quiescent Current (10 A typical)**
- **Load Regulation of 5 mV from 0 mA to 200 mA**
- **Logic Shutdown Capability**
- **Shutdown Quiescent Current Below 2 A**
- **Short Circuit Protection - Duty Cycle Limiting**
- **Remote Load Voltage Sense for Accurate Load Regulation**

SOIC
DP PACKAGES
(TOP VIEW)



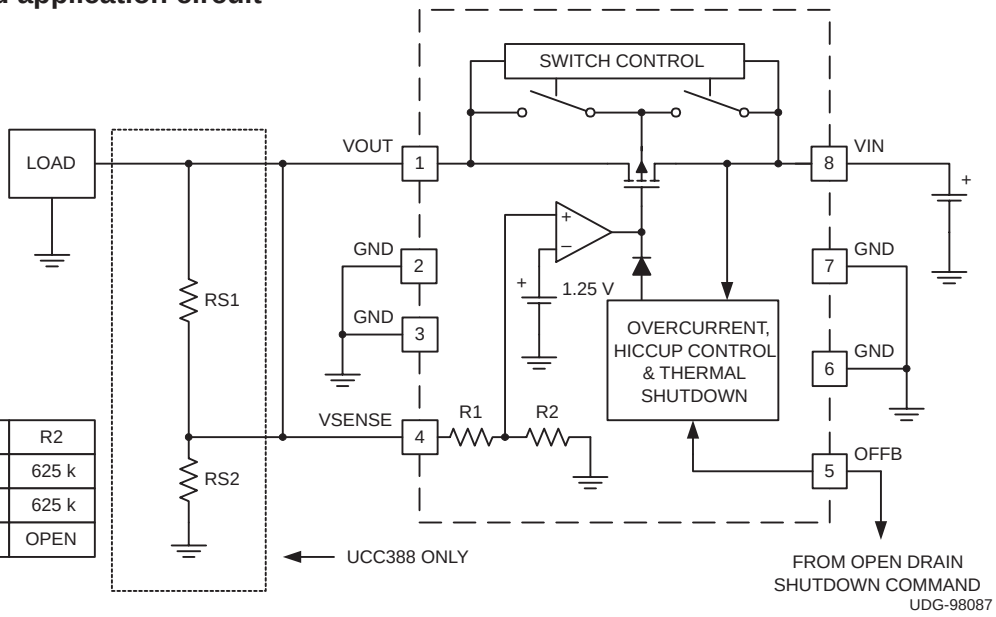
TSSOP
PW PACKAGES
(TOP VIEW)



description

The UCC386/7/8 positive linear pass regulator series is tailored for low-dropout applications where extremely low quiescent power is required. Fabricated with BiCMOS technology ideally suited for low input to output differential applications, the UCC386/7/8 will pass 200 mA while requiring only 200 mV of input voltage headroom. Quiescent current is typically less than 10 μA. To prevent reverse current conduction, on-chip circuitry limits the minimum forward voltage to 50 mV typical. Once the forward voltage limit is reached, the input-output differential voltage is maintained as the input voltage drops until undervoltage lockout disables the regulator.

block diagram and application circuit



	R1	R2
UCC386	1.025 m	625 k
UCC387	1.875 m	625 k
UCC388	0	OPEN

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description (continued)

The UCC386 has an on-chip resistor network for preset to regulate at 3.3 V, while the UCC387 has a fixed 5-V output. The UCC388 requires an external resistor network that can be programmed for output voltages down to 1.25 V. The output voltage is regulated to 1.5% at room temperature and better than 2.5% over the entire operating temperature range.

Short-circuit current is internally limited. The device responds to a sustained overcurrent condition by limiting the duty cycle of the load to 12.5% typical. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 140°C. The chip remains in the off state until the temperature drops to 115°C.

Pulling OFFB low commands a low-power shutdown mode, which requires less than 2-μA quiescent current. These devices are available in the 8-pin TSSOP (PW) and 8-pin SOIC (DP) surface-mount power packages. For other packaging options consult the factory.

AVAILABLE OPTIONS

T_A	OUTPUT VOLTAGE (V)			PACKAGE DEVICES	
	MIN	TYP	MAX	SOIC-8 (DP)	TSSOP-8 (PW)
0°C to 70°C	3.22	3.30	3.38	UCC386DP	UCC386PW
	4.785	5.000	5.125	UCC387DP	UCC387PW
		ADJ		UCC388DP	UCC388PW

† All package types are available taped and reeled. Add TR suffix to device type (e.g. UCC386DPTR) to order quantities of 3000 devices per reel.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

VIN . . . . . 9 V
OFFB . . . . . –0.3 V to VIN 0.3 V
Storage Temperature, T_{stg} . . . . . –65°C to 150°C
Junction Temperature, T_J . . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

electrical characteristics, $T_A = T_J = 0$ C to 70 C, VIN = VOUT+1.5 V, $I_{OUT} = 0$ mA, $C_{OUT} = 0.1$ F (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
UCC386 Fixed 3.3 V Output						
Output voltage	T_A = 25°C		3.25	3.3	3.35	V
	Over temperature		3.22	3.3	3.38	V
Line regulation	VIN = 3.45 V to 8.5 V,	I_{OUT} = 10 mA		13	25	mV
Load regulation	I_{OUT} = 1 mA to 200 mA			5	10	mV
Output noise voltage	T_J = 25°C,	BW = 10 Hz to 10 kHz		200		μV_{RMS}
Dropout voltage, VIN-VOUT	I_{OUT} = 200 mA,	VOUT = 3.20 V		200	500	mV
	I_{OUT} = 50 mA,	VOUT = 3.20 V		50		mV

electrical characteristics, $T_A = T_J = 0$ C to 70 C, VIN = VOUT+1.5 V, $I_{OUT} = 0$ mA, $C_{OUT} = 0.1$ F (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
UCC386 Fixed 3.3 V Output (continued)						
Peak current limit	VOUT = 0V		260	550	850	mA
Overcurrent threshold			225	375	525	mA
Current limit duty cycle	VOUT = 0 V			12.5	14	%
Overcurrent timeout, T_{ON}	VOUT = 0 V		550	900	1250	µs
Quiescent current	OFFB = VIN			10	20	µA
Shutdown quiescent current	VIN ≤ 8.5 V,	OFFB ≤ 0.5 V		2	5	µA
Shutdown threshold (OFF)	VIN = 8.5 V		0		0.5	V
Shutdown threshold (ON)	See Note 1		V_{IN} - 0.5 V			V
Reverse leakage current	0 V < VIN < VOUT,	VOUT < 3.35 V, at VIN			10	µA
	0 V < VIN < VOUT,	VOUT < 3.35 V, at VOUT			10	µA
Bias current at VSENSE pin				2		µA
UCC387 Fixed 5 V Output						
Output voltage	T_A = 25°C		4.925	5	5.075	V
	Over full temperature range		4.785	5	5.125	V
Line regulation	VIN = 5.5 V to 8.5 V,	I_{OUT} = 10 mA		13	25	mV
Load regulation	I_{OUT} = 1 mA to 200 mA			5	10	mV
Output noise voltage	T_J = 25°C,	BW = 10 Hz to 10 kHz		200		μV_{RMS}
Dropout voltage, VIN-VOUT	I_{OUT} = 200 mA,	VOUT = 4.75 V		200	500	mV
	I_{OUT} = 50 mA,	VOUT = 4.75 V		50		mV
Peak current limit	VOUT = 0 V		260	550	850	mA
Overcurrent threshold			225	375	525	mA
Current limit duty cycle	VOUT = 0 V			12.5	14	%
Overcurrent timeout, T_{ON}	VOUT = 0 V		550	900	1250	µs
Quiescent current	OFFB = VIN			10	20	µA
Shutdown quiescent current	VIN ≤ 8.5 V,	OFFB ≤ 0.5 V		2	5	µA
Shutdown threshold (OFF)	VIN = 8.5 V		0		0.5	V
Shutdown threshold (ON)	See Note 1		V_{IN} - 0.5 V			V
Reverse leakage current	0 V < VIN < VOUT,	VOUT < 3.35 V, at VIN			10	µA
	0 V < VIN < VOUT,	VOUT < 3.35 V, at VOUT			10	µA
Bias current at VSENSE pin				2		µA
UCC388 Adjustable Output						
Output voltage	T_A = 25°C		1.23	1.25	1.27	V
	Over full temperature range		1.22	1.25	1.28	V
Line regulation	VIN = 2.5V to 8.5 V,	I_{OUT} = 10 mA, V_{OUT} = 1.25 V		10	40	mV
Load regulation	I_{OUT} = 1 mA to 200 mA			5	10	mV
Output noise voltage	T_J = 25°C,	BW = 10 Hz to 10 kHz		200		μV_{RMS}
Dropout voltage, VIN-VOUT	I_{OUT} = 200 mA,	VOUT = 3.20 V		200	500	mV
	I_{OUT} = 50 mA,	VOUT = 3.20 V		50		mV
Peak current limit	VOUT = 0 V		260	550	850	mA
Overcurrent threshold			225	375	525	mA

NOTE 1: An internal 100-nA pullup is provided for this function.

electrical characteristics, $T_A = T_J = 0$ C to 70 C, VIN = VOUT+1.5 V, $I_{OUT} = 0$ mA, $C_{OUT} = 0.1$ F (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
UCC388 Adjustable Output (continued)						
Current limit duty cycle	VOUT = 0 V			12.5	14	%
Overcurrent timeout, T_{ON}	VOUT = 0 V		550	900	1250	μs
Quiescent current	OFFB = VIN			10	20	μA
Shutdown quiescent current	VIN ≤ 8.5 V,	OFFB ≤ 0.5 V		2	5	μA
Shutdown threshold (OFF)	VIN = 8.5 V		0		0.5	V
Shutdown threshold (ON)	See Note 1		V_{IN} - 0.5 V			V
Reverse leakage current	0 V < VIN < VOUT,	VOUT < 3.35 V, at VIN			10	μA
	0 V < VIN < VOUT,	VOUT < 3.35 V, at VOUT			10	μA
Bias current at VSENSE pin				50		nA
Minimum operating voltage					2.5	V

NOTE 1: An internal 100-nA pullup is provided for this function.

pin descriptions

GND: Chip Ground. All voltages are measured with respect to this pin. This is the low-noise ground reference for input regulation. The output decoupling capacitor should be tied between VOUT and GND.

OFFB: Shutdown, active low. This pin must be externally pulled to GND to turn off the IC. Pulling this pin high turns on the IC. This pin is internally pulled to VIN by 100-nA current source.

VIN: Positive supply input for the regulator. Bypass this pin to GND with at least 0.1 μF of low ESR, ESL capacitance if the source is located further than 1 inch from the device.

VOUT: Output of the regulator. The regulator does not require a minimum output capacitance for stability, however a small capacitor is recommended to improve transient response. Choose the appropriate size capacitor for the application with respect to the required transient loading. For example, if the load is very dynamic, a large capacitor will smooth out the response to load steps.

VSENSE: Externally programmable voltage sense node. For the UCC388, connect resistor divider network between VOUT, VSENSE and GND to provide custom regulation level. For the UCC386 and UCC387, connect this pin to VOUT as close to the load as possible.

APPLICATION INFORMATION

load independent current consumption

This series of LDOs is based on CMOS circuitry and uses a high-side P-channel pass element. Consequently, the current consumed by the LDO is extremely low at 10 μA under normal operating conditions and does not vary with load. The shutdown mode (OFFB = GND) consumes only 2 μA, making this series an excellent choice for battery applications.

reverse voltage standoff

These LDOs are designed to operate with the voltage at the output greater than the voltage at the input. This can be an advantage where a circuit needs to be powered from two separate power sources that must be kept isolated, such as selecting between one of two or more batteries.

APPLICATION INFORMATION

overcurrent protection

The UCC386/7/8 uses a fixed, absolute, current limit in conjunction with a timed overcurrent function that significantly reduces power dissipation in the event of a shorted load (see Figure 1). In this diagram, a 100-mA load is applied to the output of the LDO. At some point, a fault is applied. When the current level exceeds the overcurrent threshold of about 300 mA, a timer is started. If the current does not fall below the overcurrent threshold before the timer times out, about 5.6 ms, the LDO declares an overcurrent condition exists and turns off its output for about 5.6 ms. Note that the output current is internally limited to 600 mA. After the output has been off for 5.6 ms, it is turned on for about 800 μs and again limited to 600 mA. If the current does not fall below the overcurrent threshold before the 800-μs timer expires, the output is again turned off for 5.6 ms. This process repeats itself until the fault condition is removed from the output of the LDO. The average current supplied to the faulted load by the LDO is approximately 112 mA. This is well below the maximum rated current of 200 mA of the LDO. Therefore, for most applications that have adequate thermal dissipation for the LDO to operate at full rated load, the thermal dissipation will also be adequate in a faulted condition.

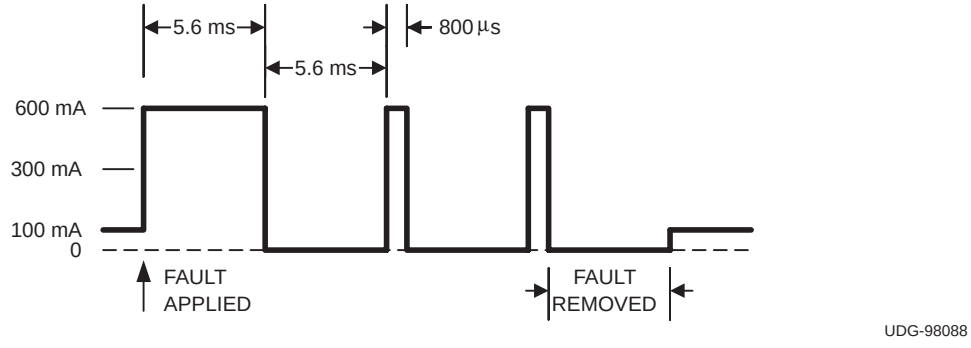

Figure 1. Current Waveform During a Fault

thermal shutdown

The LDOs have a thermal shutdown circuit that will turn the LDO output off before the die temperature reaches damaging levels. When the die cools, the LDO will again function. The thermal shutdown circuit has a turn-off threshold of nominally 140°C, and a turn-on threshold of 115°C. These temperatures insure that the LDO will not be damaged due to excessive power dissipation.

maximum load recovery

The LDO will start a load that has a large capacitance and a dc current component. One of the consequences of the LDOs fault behavior is a maximum output capacitor value and load current that the LDO can restart after an overcurrent condition has been declared. Figure 2 shows the maximum load that the LDO can re-start from a faulted condition with a given output filter capacitor. Note that the LDO can start a much higher load than it can restart after a fault. If the LDO is hiccuping into a load that it cannot re-start, either momentarily disconnecting the load or a power cycle allows the LDO to start the load.

APPLICATION INFORMATION

maximum load recovery (continued)

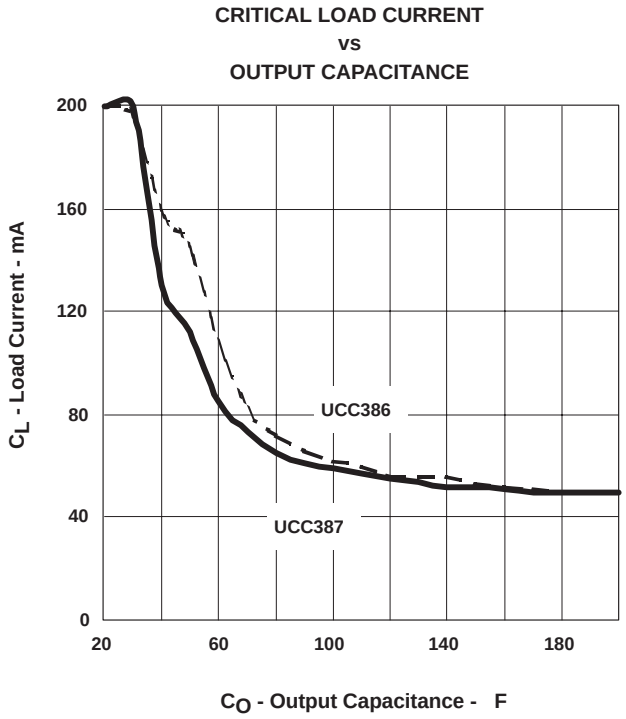

Figure 2.

using OFFB

The OFFB pin is used to turn the output of the LDO on or off from some external source. There are two things to note when using this pin. The first is that after taking OFFB high (on), the LDO will require up to about 2 ms to start and stabilize. The second item is that OFFB is designed to be driven from an open-drain-type output. Internally, this pin is pulled high by a weak 100-nA current source, and will normally be at the input supply voltage, so the driving circuitry must be able to withstand the voltage applied to the input of the regulator. Also, depending upon load, if the OFFB pin is driven (overriding the internal pull-up) high with a fast edge signal, there may be a brief pulse on the output, followed by no output, with the regulator coming on and stabilizing about 2 ms after the OFFB pin was driven high. This output pulse is never more than the normal output voltage of the regulator and is about 200 μs in length.

APPLICATION INFORMATION

output capacitance and transient response

The transient response of the regulator is heavily influenced by the capacitor on the output. In general, larger capacitors produce less voltage variation during load changes, but take longer to stabilize (quit wiggling). Note that no output capacitor is required for a stable output. However, if the load exhibits sharp changes in current requirements, and temporary deviations from the nominal output voltage must be minimized, some output filter capacitor will be needed.

UCC388 output voltage programming

Referring to the applications diagram on the front page of the data sheet, the output voltage is given by:

$$V_O = 1.25\left(\frac{R_{S1} + R_{S2}}{R_{S2}}\right)$$

Note that for the UCC388, the internal resistor R2 is open.

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