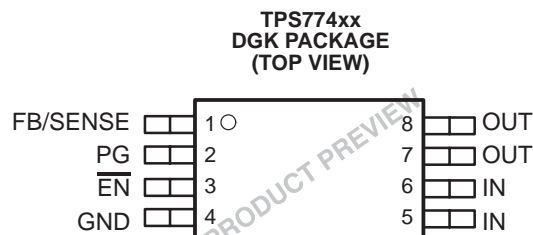
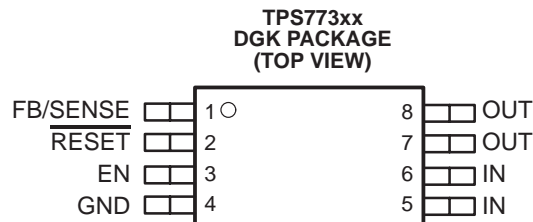


TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH RESET OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG

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- Open Drain Power-On Reset With 220-ms Delay (TPS773xx)
- Open Drain Power-Good (PG) Status Output (TPS774xx)
- 250-mA Low-Dropout Voltage Regulator
- Available in 1.8-V, 2.7-V, 2.8-V, 3.3-V, Fixed Output and Adjustable Versions
- Dropout Voltage Typically 200 mV at 250 mA (TPS77333, TPS77433)
- Ultra Low 92- $\mu$ A Quiescent Current (Typ)
- 8-Pin MSOP (DGK) Package
- Low Noise (55  $\mu$ V<sub>rms</sub>) Without an External Filter (Bypass) Capacitor (TPS77318, TPS77418)
- 2% Tolerance Over Specified Conditions For Fixed-Output Versions
- Fast Transient Response
- Thermal Shutdown Protection
- See the TPS779xx Family of Devices for Active High Enable

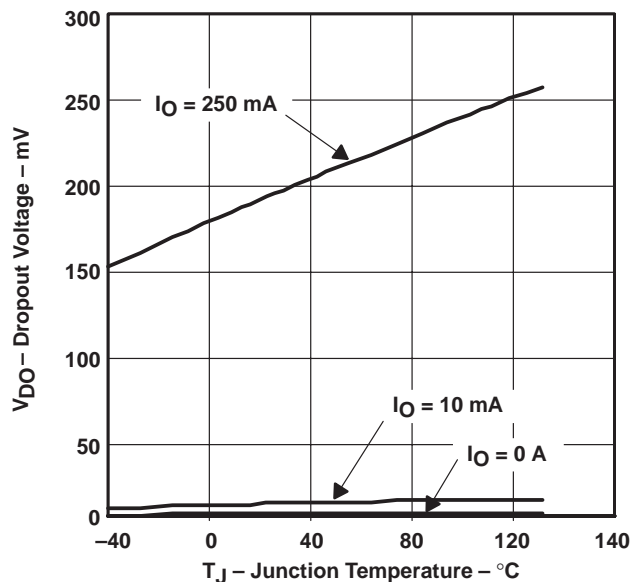


**description**

The TPS773xx and TPS774xx are low dropout regulators with integrated power-on reset and power good (PG) function respectively. These devices are capable of supplying 250 mA of output current with a dropout of 200 mV (TPS77333, TPS77433). Quiescent current is 92  $\mu$ A at full load dropping down to 1  $\mu$ A when device is disabled. These devices are optimized to be stable with a wide range of output capacitors including low ESR ceramic (10  $\mu$ F) or low capacitance (1  $\mu$ F) tantalum capacitors. These devices have extremely low noise output performance (55  $\mu$ V<sub>rms</sub>) without using any added filter capacitors. TPS773xx and TPS774xx are designed to have fast transient response for larger load current changes.

The TPS773xx or TPS774xx is offered in 1.8-V, 2.7-V, 2.8-V and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is 2% over line, load, and temperature ranges. The TPS773xx and TPS774xx families are available in 8-pin MSOP (DGK) packages.

TPS77x33  
DROPOUT VOLTAGE  
vs  
JUNCTION TEMPERATURE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**description (continued)**

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 200 mV at an output current of 250 mA for 3.3 volt option) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 92  $\mu\text{A}$  over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when the  $\overline{\text{EN}}$  pin is connected to a low-level input voltage. This LDO family also features a sleep mode; applying a TTL high signal to  $\overline{\text{EN}}$  (enable) shuts down the regulator, reducing the quiescent current to less than 1  $\mu\text{A}$  at  $T_J = 25^\circ\text{C}$ .

The TPS773xx features an integrated power-on reset, commonly used as an supply voltage supervisor (SVS), or reset output voltage. The  $\overline{\text{RESET}}$  output of the TPS773xx initiates a reset in DSP, microcomputer or microprocessor systems at power-up and in the event of an undervoltage condition. An internal comparator in the TPS773xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT reaches 95% of its regulated voltage,  $\overline{\text{RESET}}$  will go to a high-impedance state after a 220 ms delay.  $\overline{\text{RESET}}$  will go to low-impedance state when OUT is pulled below 95% (i.e. over load condition) of its regulated voltage.

For the TPS774xx, the power good terminal (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator. An internal comparator in the TPS774xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When OUT falls below 82% of its regulated voltage, PG will go to a low-impedance state. PG will go to a high-impedance state when OUT is above 82% of its regulated voltage.

**AVAILABLE OPTIONS**

$T_J$	OUTPUT VOLTAGE (V)	PACKAGED DEVICES	
	TYP	MSOP (DGK)	
-40°C to 125°C	3.3	TPS77333DGK	TPS77433DGK
	2.8	TPS77328DGK	TPS77428DGK
	2.7	TPS77327DGK	TPS77427DGK
	1.8	TPS77318DGK	TPS77418DGK
	Adjustable 1.5 V to 5.5 V	TPS77301DGK	TPS77401DGK

The TPS77301 and TPS77401 are programmable using an external resistor divider (see application information). The DGK package is available taped and reeled. Add an R suffix to the device type (e.g., TPS77301DGKR).



TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG

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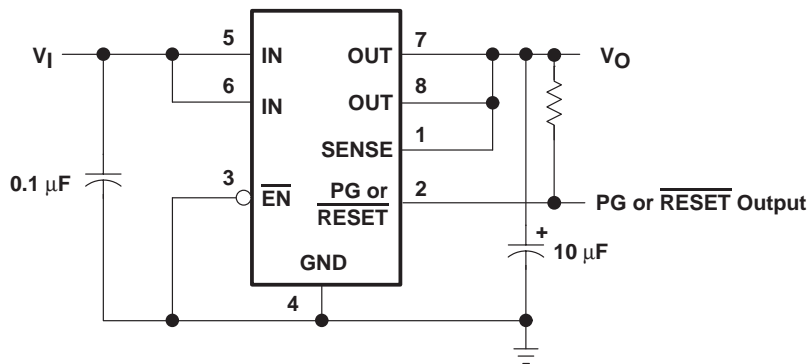
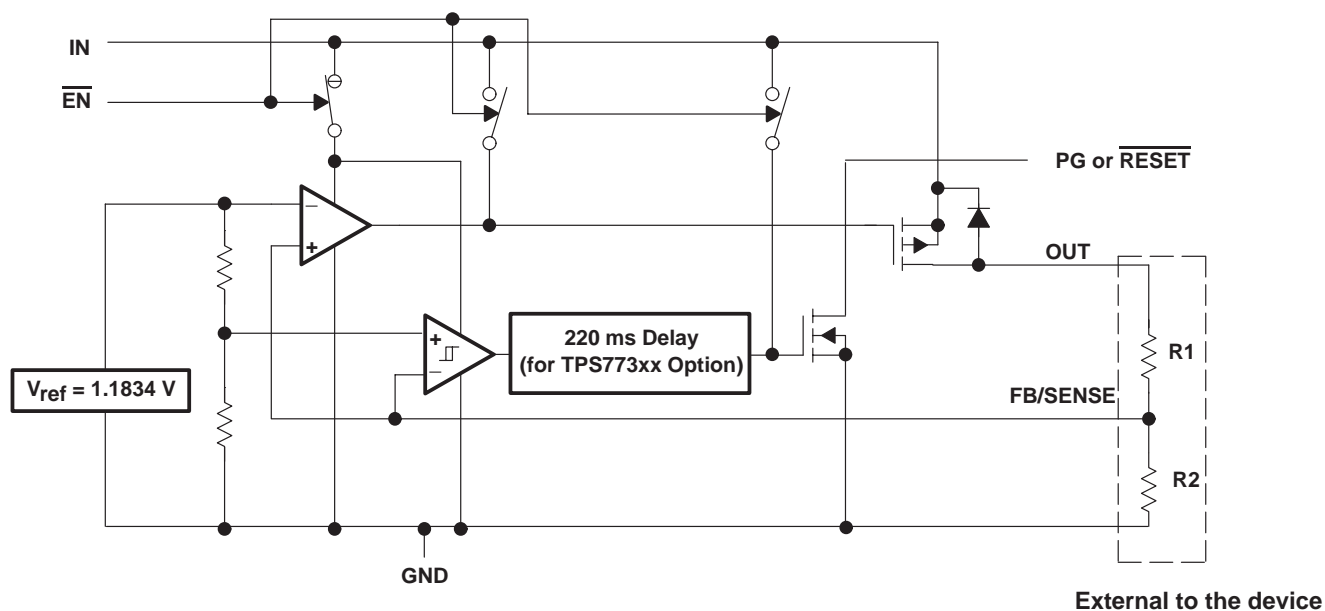


Figure 1. Typical Application Configuration (For Fixed Output Options)

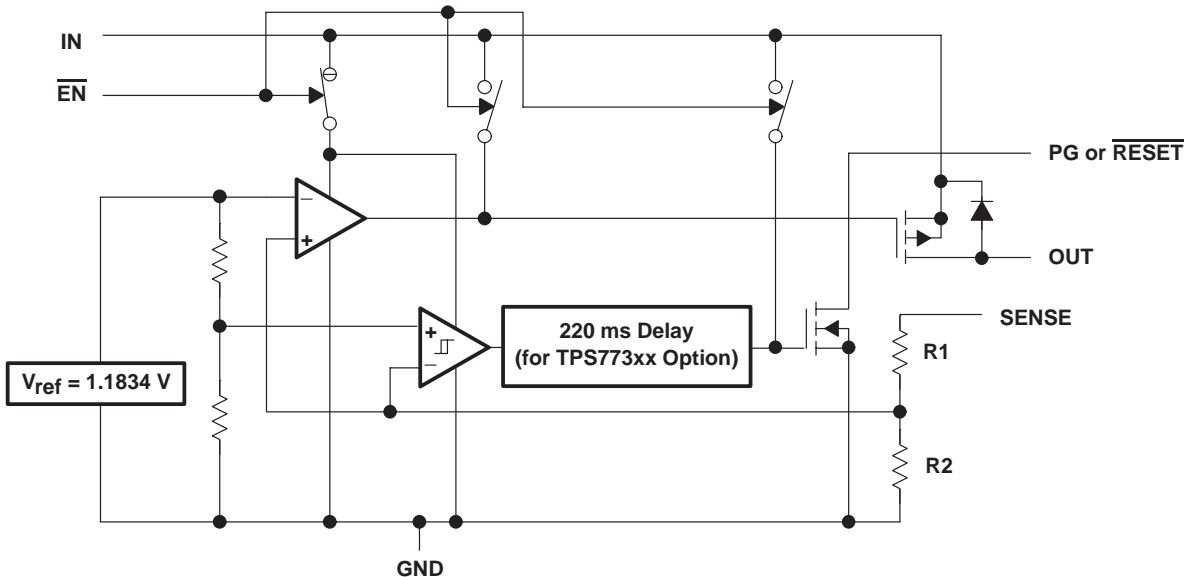
functional block diagram—adjustable version



**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT**  
**TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT**  
**250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**functional block diagram—fixed-voltage version**



**Terminal Functions (TPS773xx)**

TERMINAL NAME	NO.	I/O	DESCRIPTION
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
RESET	2	O	Reset output
EN	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage

**Terminal Functions (TPS774xx)**

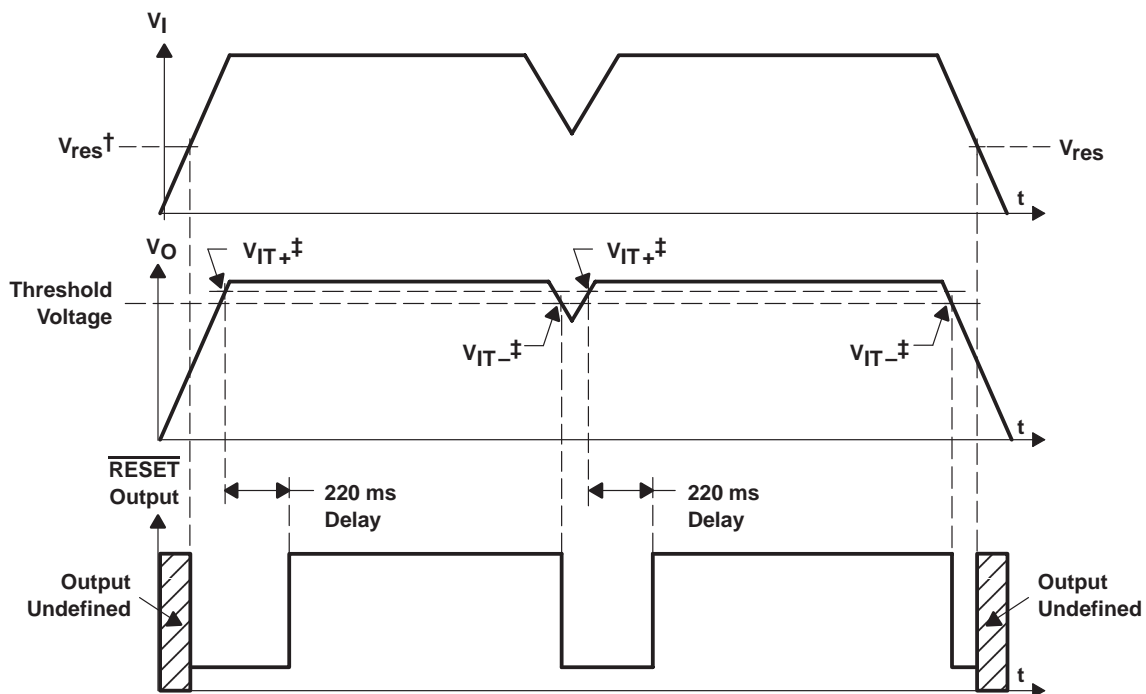
TERMINAL NAME	NO.	I/O	DESCRIPTION
FB/SENSE	1	I	Feedback input voltage for adjustable device (sense input for fixed options)
PG	2	O	Power good
EN	3	I	Enable input
GND	4		Regulator ground
IN	5, 6	I	Input voltage
OUT	7, 8	O	Regulated output voltage



TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG

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TPS773xx  $\overline{\text{RESET}}$  timing diagram



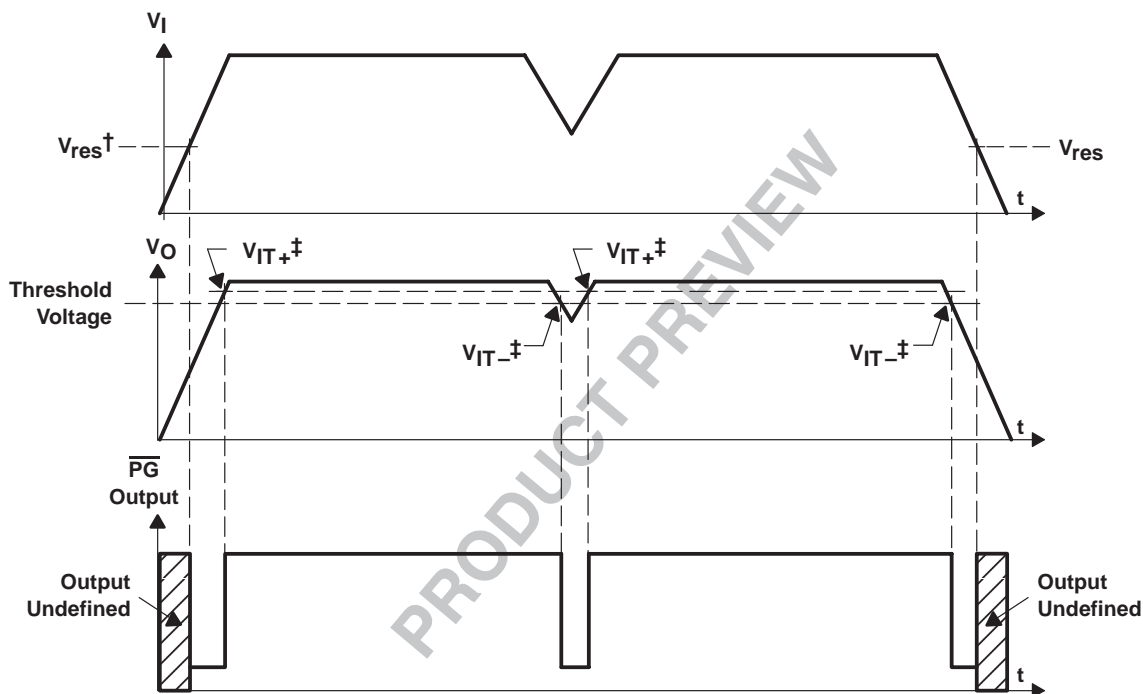
†  $V_{res}$  is the minimum input voltage for a valid  $\overline{\text{RESET}}$ . The symbol  $V_{res}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡  $V_{IT-}$  – Trip voltage is typically 5% lower than the output voltage ( $95\%V_o$ )  $V_{IT-}$  to  $V_{IT+}$  is the hysteresis voltage.

TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG

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TPS774xx PG timing diagram



†  $V_{res}$  is the minimum input voltage for a valid PG. The symbol  $V_{res}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡  $V_{IT-}$  Trip voltage is typically 18% lower than the output voltage ( $82\%V_O$ )  $V_{IT-}$  to  $V_{IT+}$  is the hysteresis voltage.

**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH RESET OUTPUT  
TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**absolute maximum ratings over operating junction temperature range  
(unless otherwise noted)†**

Input voltage range‡, $V_I$ .....	–0.3 V to 13.5 V
Voltage range at $\overline{EN}$ .....	–0.3 V to 16.5 V
Maximum $\overline{RESET}$ voltage (TPS773xx) .....	16.5 V
Maximum PG voltage (TPS774xx) .....	16.5 V
Peak output current .....	Internally limited
Continuous total power dissipation .....	See dissipation rating tables
Output voltage, $V_O$ (OUT, FB) .....	5.5 V
Operating virtual junction temperature range, $T_J$ .....	–40°C to 125°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C
ESD rating, HBM .....	2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

**DISSIPATION RATING TABLE – FREE-AIR TEMPERATURES**

PACKAGE	AIR FLOW (CFM)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)	T <sub>A</sub> < 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGK	0	266.2	3.84	376 mW	3.76 mW/°C	207 mW	150 mW
	150	255.2	3.92	392 mW	3.92 mW/°C	216 mW	157 mW
	250	242.8	4.21	412 mW	4.12 mW/°C	227 mW	165 mW

**recommended operating conditions**

	MIN	MAX	UNIT
Input voltage, $V_I$ §	2.7	10	V
Output voltage range, $V_O$	1.5	5.5	V
Output current, $I_O$ (see Note 1)	0	250	mA
Operating virtual junction temperature, $T_J$ (see Note 1)	–40	125	°C

§ To calculate the minimum input voltage for your maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$ .  
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH RESET OUTPUT**  
**TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT**  
**250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**electrical characteristics over recommended operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_I = V_{O(\text{typ})} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 10\text{ }\mu\text{F}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (see Notes 2 and 4)	Adjustable voltage	$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$ , $T_J = 25^\circ\text{C}$	$V_O$			V
		$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$	$0.98V_O$	$1.02V_O$		
	1.8 V Output	$T_J = 25^\circ\text{C}$ , $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.8			
		$2.8\text{ V} < V_{IN} < 10\text{ V}$	1.764	1.836		
	2.7 V Output	$T_J = 25^\circ\text{C}$ , $3.7\text{ V} < V_{IN} < 10\text{ V}$	2.7			
		$3.7\text{ V} < V_{IN} < 10\text{ V}$	2.646	2.754		
	2.8 V Output	$T_J = 25^\circ\text{C}$ , $3.8\text{ V} < V_{IN} < 10\text{ V}$	2.8			
		$3.8\text{ V} < V_{IN} < 10\text{ V}$	2.744	2.856		
3.3 V Output	$T_J = 25^\circ\text{C}$ , $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.3				
	$4.3\text{ V} < V_{IN} < 10\text{ V}$	3.234	3.366			
Quiescent current (GND current) (see Notes 2 and 4)		$T_J = 25^\circ\text{C}$		92		$\mu\text{A}$
Output voltage line regulation ( $\Delta V_O/V_O$ ) (see Note 3)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$ , $T_J = 25^\circ\text{C}$	0.005			%/V
		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$			0.05	%/V
Load regulation		$T_J = 25^\circ\text{C}$	1			mV
Output noise voltage		BW = 300 Hz to 100 kHz, $T_J = 25^\circ\text{C}$ , TPS77318, TPS77418	55			$\mu\text{Vrms}$
Output current limit		$V_O = 0\text{ V}$	0.9	1.3		A
Peak output current		2 ms pulse width, 50% duty cycle	400			mA
Thermal shutdown junction temperature			144			$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$ , $T_J = 25^\circ\text{C}$			1	$\mu\text{A}$
		$\overline{\text{EN}} = V_I$			3	$\mu\text{A}$
FB input current	Adjustable voltage	FB = 1.5 V			1	$\mu\text{A}$
High level enable input voltage			2			V
Low level enable input voltage					0.7	V
Enable input current			-1	1		$\mu\text{A}$
Power supply ripple rejection (TPS77318, TPS77418)		f = 1 kHz, $T_J = 25^\circ\text{C}$	55			dB
PG (TPS774xx)	Minimum input voltage for valid PG	$I_{(\text{PG})} = 300\text{ }\mu\text{A}$ , $V_{(\text{PG})} \leq 0.8\text{ V}$	1.1			V
	Trip threshold voltage	$V_O$ decreasing	79	85		% $V_O$
	Hysteresis voltage	Measured at $V_O$	0.5			% $V_O$
	Output low voltage	$V_I = 2.7\text{ V}$ , $I_{(\text{PG})} = 1\text{ mA}$	0.15	0.4		V
	Leakage current	$V_{(\text{PG})} = 5\text{ V}$	1			$\mu\text{A}$

NOTES: 2. Minimum input operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1\text{ V}$ , whichever is greater. Maximum input voltage = 10 V, minimum output current 1 mA.

3. If  $V_O < 1.8\text{ V}$  then  $V_{\text{imax}} = 10\text{ V}$ ,  $V_{\text{imin}} = 2.7\text{ V}$ :

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7\text{ V})}{100} \times 1000$$

If  $V_O > 2.5\text{ V}$  then  $V_{\text{imax}} = 10\text{ V}$ ,  $V_{\text{imin}} = V_O + 1\text{ V}$ :

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1))}{100} \times 1000$$

4.  $I_O = 1\text{ mA}$  to 250 mA





**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH RESET OUTPUT  
TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**electrical characteristics over recommended operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_I = V_O(\text{typ}) + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 10\ \mu\text{F}$  (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset (TPS773xx)	Minimum input voltage for valid RESET	$I(\text{RESET}) = 300\ \mu\text{A}$		1.1		V
	Trip threshold voltage	$V_O$ decreasing	92		98	% $V_O$
	Hysteresis voltage	Measured at $V_O$		0.5		% $V_O$
	Output low voltage	$V_I = 2.7\text{ V}$ , $I(\text{RESET}) = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{RESET}) = 5\text{ V}$			1	$\mu\text{A}$
	RESET time-out delay			220		ms
$V_{\text{DO}}$	Dropout voltage (see Note 5)	2.8 V Output	$I_O = 250\text{ mA}$ , $T_J = 25^\circ\text{C}$		270	mV
			$I_O = 250\text{ mA}$		475	
		3.3 V Output	$I_O = 250\text{ mA}$ , $T_J = 25^\circ\text{C}$		200	
			$I_O = 250\text{ mA}$		330	

NOTE 5:  $I_{\text{IN}}$  voltage equals  $V_O(\text{Typ}) - 100\text{ mV}$ ; 1.8 V, and 2.7 V dropout voltage limited by input voltage range limitations (i.e., 3.3 V input voltage needs to drop to 3.2 V for purpose of this test).

## TYPICAL CHARACTERISTICS

### Table of Graphs

			FIGURE
$V_O$	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5
	Ground current	vs Junction temperature	6
	Power supply rejection ratio	vs Frequency	7
	Output spectral noise density	vs Frequency	8
$Z_O$	Output impedance	vs Frequency	9
$V_{\text{DO}}$	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
	Line transient response		12, 14
	Load transient response		13, 15
	Output voltage	vs Time	16
	Equivalent series resistance (ESR)	vs Output current	18 – 21



TYPICAL CHARACTERISTICS

TPS77x33  
 OUTPUT VOLTAGE  
 VS  
 OUTPUT CURRENT

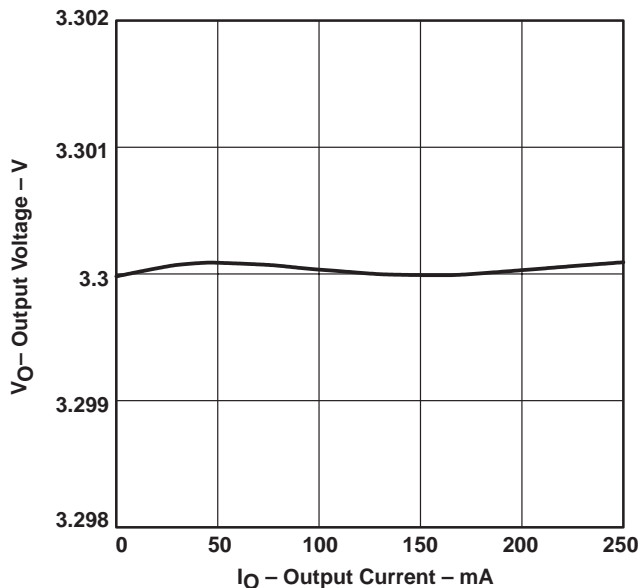


Figure 2

TPS77x18  
 OUTPUT VOLTAGE  
 VS  
 OUTPUT CURRENT

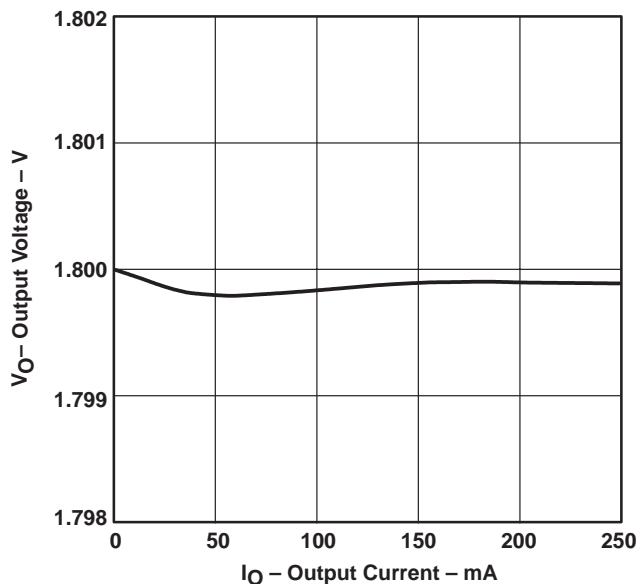


Figure 3

TPS77x33  
 OUTPUT VOLTAGE  
 VS  
 JUNCTION TEMPERATURE

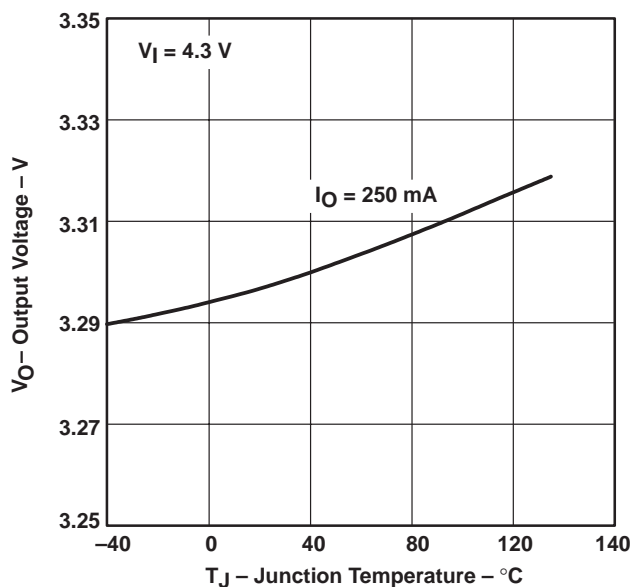


Figure 4

TPS77x18  
 OUTPUT VOLTAGE  
 VS  
 JUNCTION TEMPERATURE

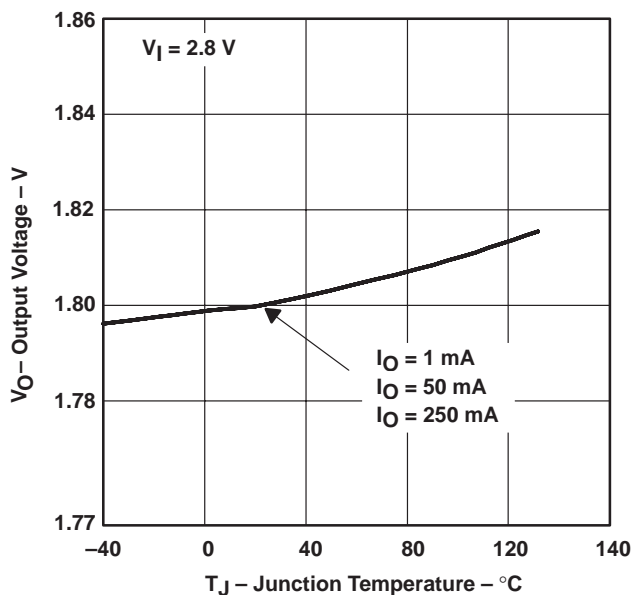


Figure 5

TYPICAL CHARACTERISTICS

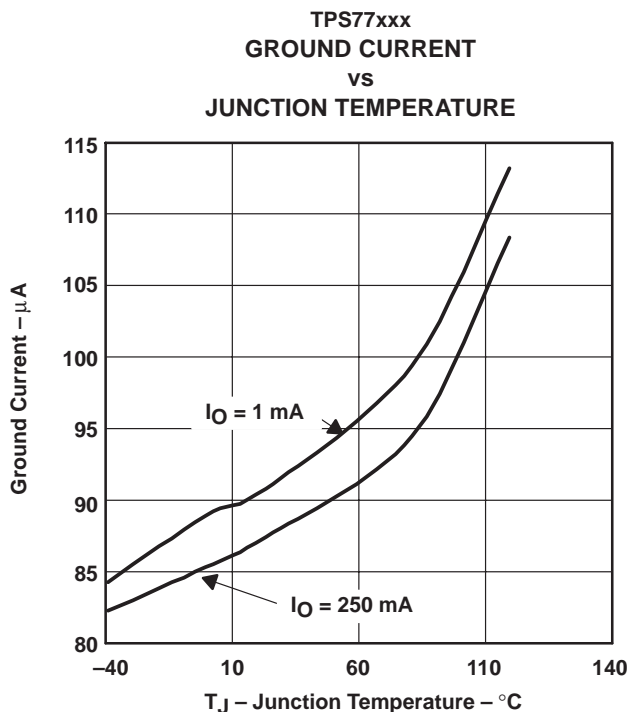


Figure 6

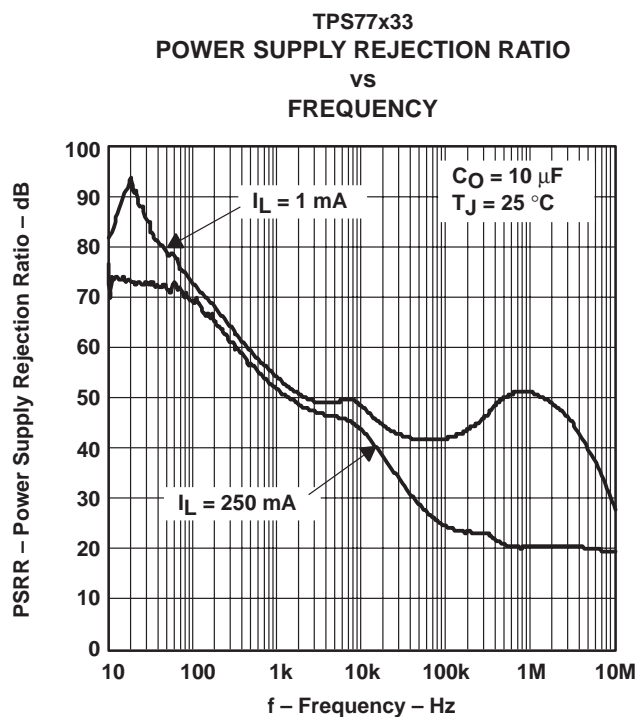


Figure 7

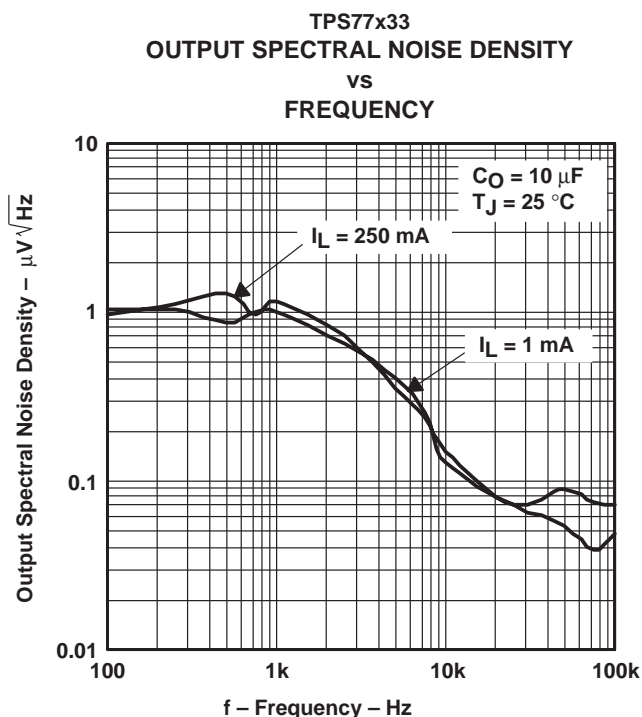


Figure 8

TYPICAL CHARACTERISTICS

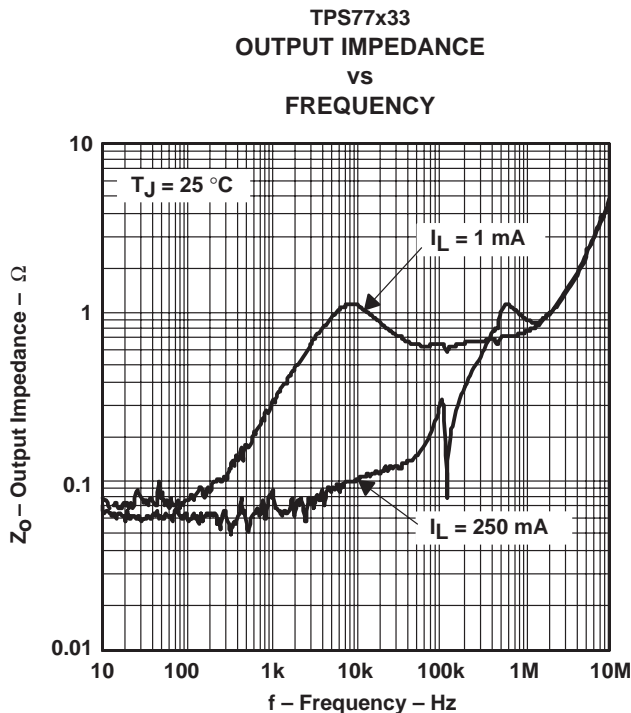


Figure 9

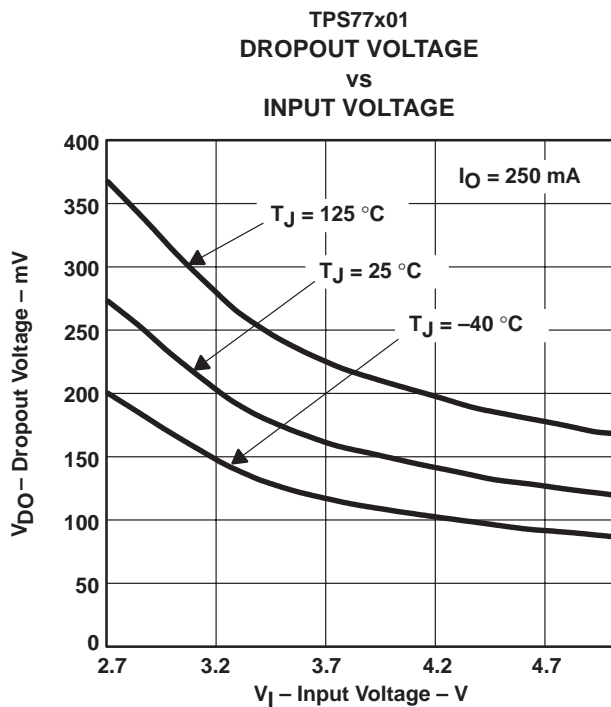


Figure 10

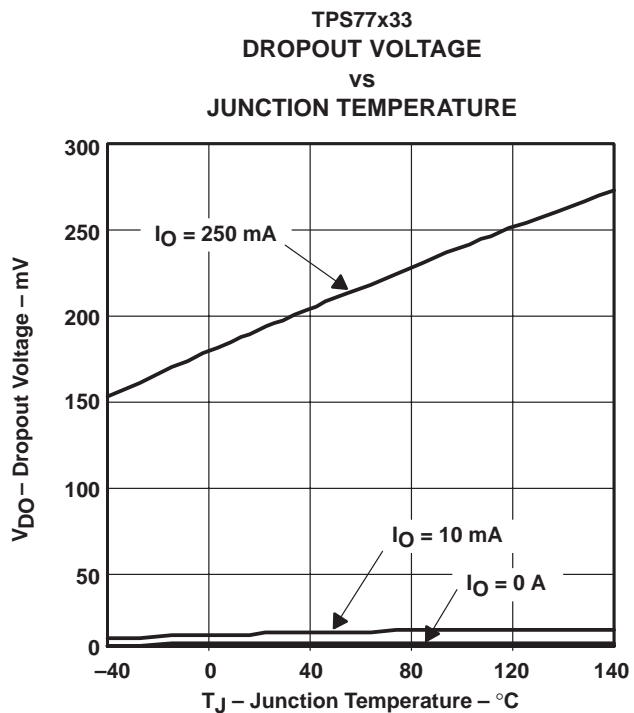


Figure 11

TYPICAL CHARACTERISTICS

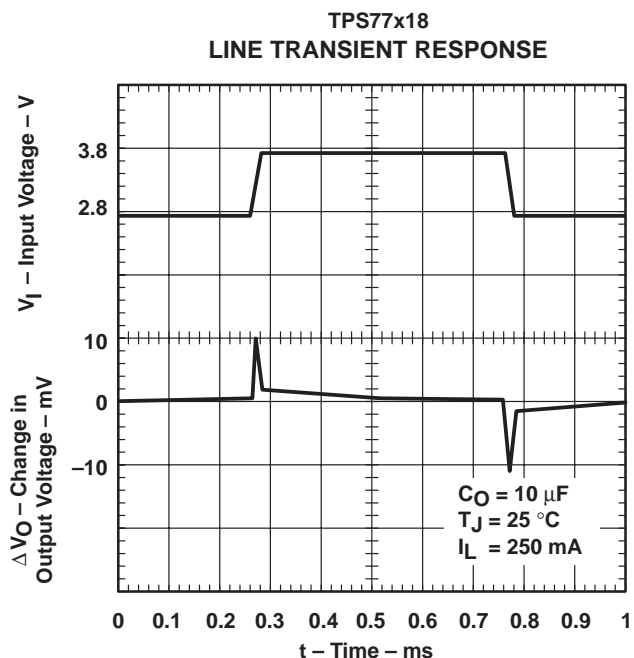


Figure 12

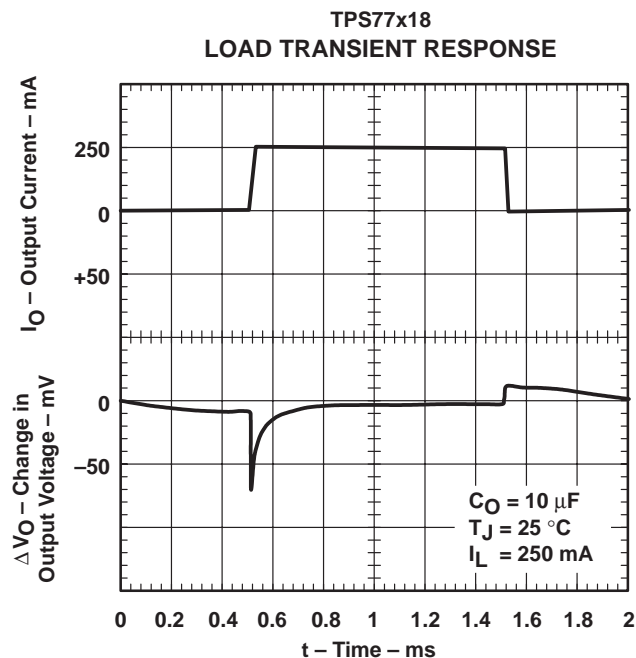


Figure 13

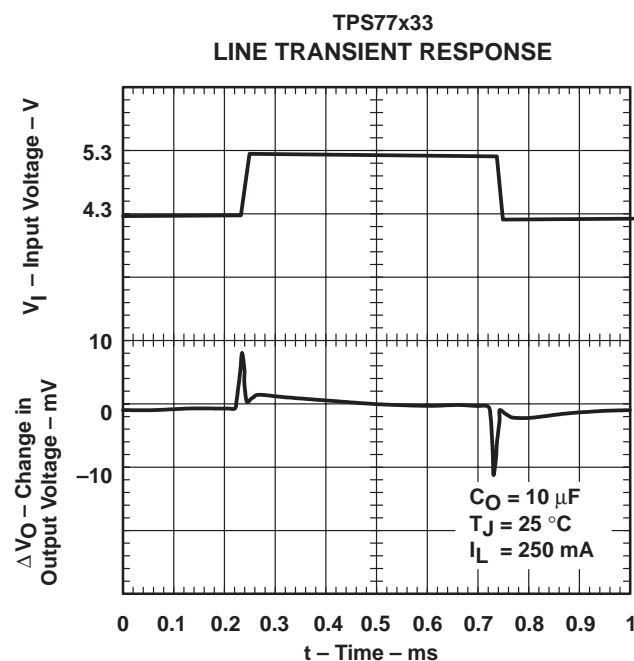


Figure 14

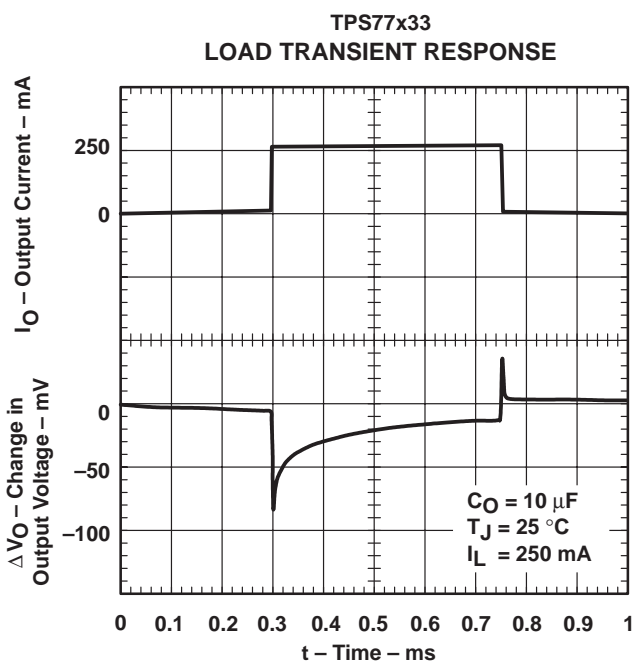


Figure 15

TYPICAL CHARACTERISTICS

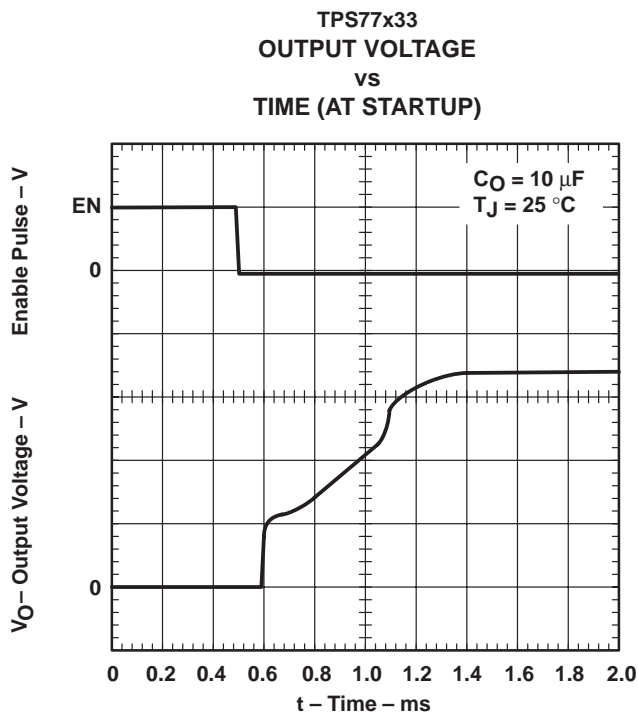


Figure 16

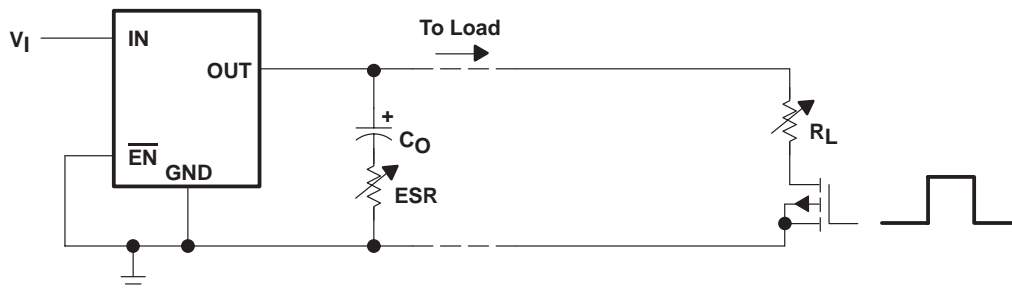


Figure 17. Test Circuit for Typical Regions of Stability (Figures 25 through 28) (Fixed Output Options)

TYPICAL CHARACTERISTICS

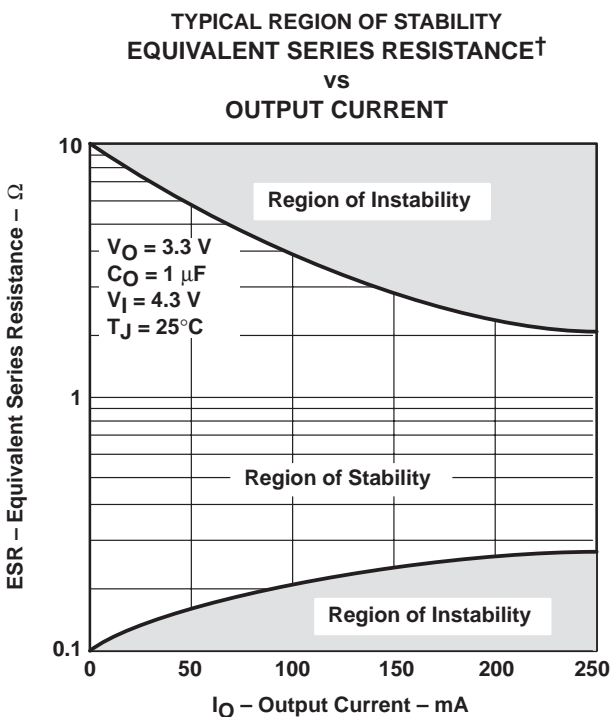


Figure 18

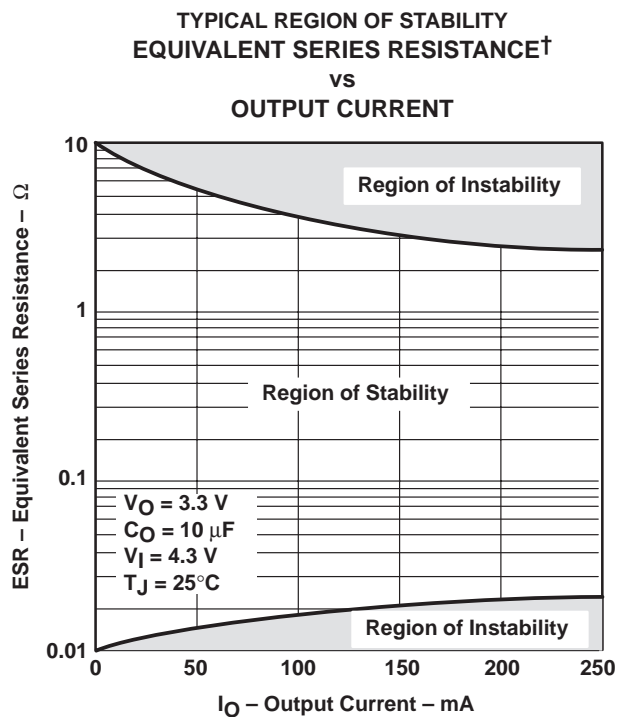


Figure 19

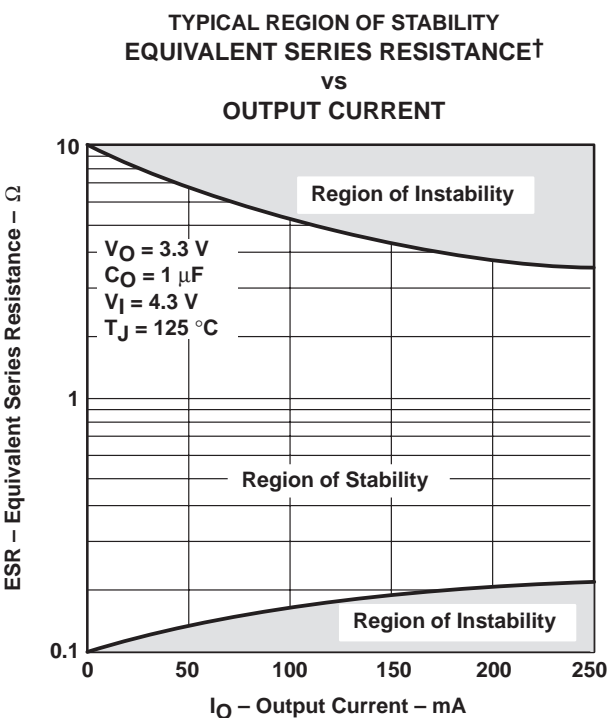


Figure 20

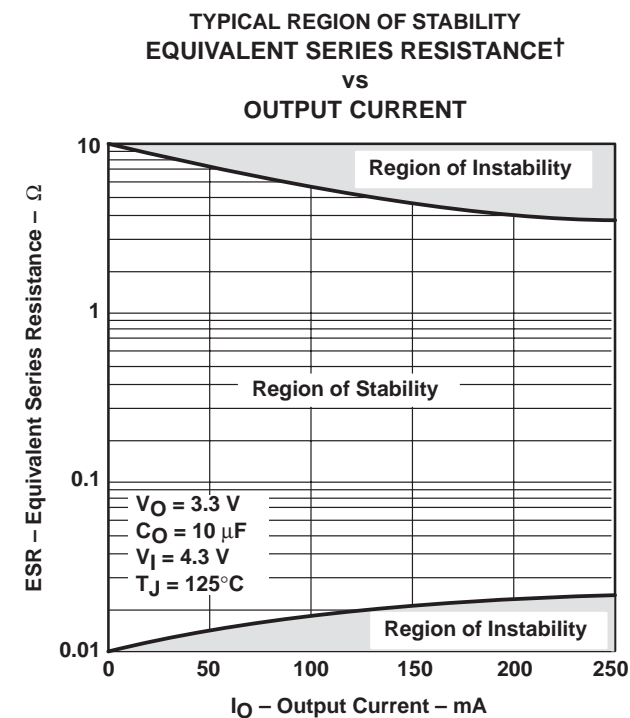


Figure 21

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

# TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH $\overline{\text{RESET}}$ OUTPUT TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT 250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG

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## APPLICATION INFORMATION

### pin functions

#### enable ( $\overline{\text{EN}}$ )

The  $\overline{\text{EN}}$  terminal is an input which enables or shuts down the device. If  $\overline{\text{EN}}$  is a logic high, the device will be in shutdown mode. When  $\overline{\text{EN}}$  goes to logic low, then the device will be enabled.

#### power good (PG) (TPS774xx)

The PG terminal is an open drain, active high output that indicates the status of  $V_{\text{out}}$  (output of the LDO). When  $V_{\text{out}}$  reaches 82% of the regulated voltage, PG will go to a high impedance state. It will go to a low-impedance state when  $V_{\text{out}}$  falls below 82% (i.e. over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

#### sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and  $V_{\text{out}}$  to filter noise is not recommended because it may cause the regulator to oscillate.

#### feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and  $V_{\text{out}}$  to filter noise is not recommended because it may cause the regulator to oscillate.

#### reset ( $\overline{\text{RESET}}$ ) (TPS773xx)

The  $\overline{\text{RESET}}$  terminal is an open drain, active low output that indicates the status of  $V_{\text{out}}$ . When  $V_{\text{out}}$  reaches 95% of the regulated voltage,  $\overline{\text{RESET}}$  will go to a low-impedance state after a 220-ms delay.  $\overline{\text{RESET}}$  will go to a high-impedance state when  $V_{\text{out}}$  is below 95% of the regulated voltage. The open-drain output of the  $\overline{\text{RESET}}$  terminal requires a pullup resistor.



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## APPLICATION INFORMATION

### external capacitor requirements

An input capacitor is not usually required; however, a bypass capacitor (0.047  $\mu$ F or larger) improves load transient response and noise rejection if the TPS773xx or TPS774xx is located more than a few inches from the power supply. A higher-capacitance capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

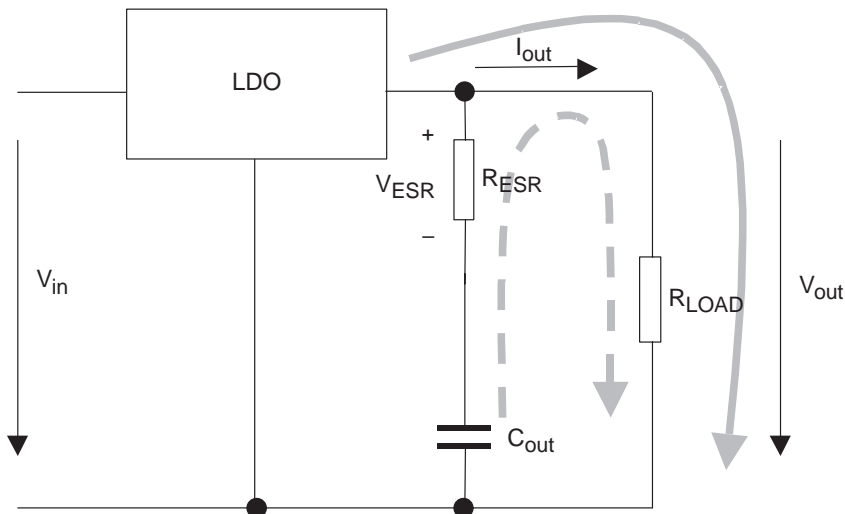
Most low noise LDOs require an external capacitor to further reduce noise. This will impact the cost and board space. The TPS773xx and TPS774xx have very low noise specification requirements without using any external components.

Like all low dropout regulators, the TPS773xx or TPS774xx requires an output capacitor connected between OUT (output of the LDO) and GND (signal ground) to stabilize the internal control loop. The minimum recommended capacitance value is 1  $\mu$ F provided the ESR meets the requirement in Figures 19 and 21. In addition, a low-ESR capacitor can be used if the capacitance is at least 10  $\mu$ F and the ESR meets the requirements in Figures 18 and 20. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

Ceramic capacitors have different types of dielectric material with each exhibiting different temperature and voltage variation. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic type capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable to use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature; therefore, the Y5U and Z5U are not generally recommended for use on this LDO. Independent of which type of capacitor is used, one must make certain that at the worst case condition the capacitance/ESR meets the requirement specified in Figures 18 – 21.

### APPLICATION INFORMATION

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.



**Figure 22. – LDO Output Stage With Parasitic Resistances ESR and ESL**

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ( $V_{C_{out}} = V_{out}$ ). This means no current is flowing into the  $C_{out}$  branch. If  $I_{out}$  suddenly increases (transient condition), the following occurs;

The LDO is not able to supply the sudden current need due to its response time ( $t_1$  in Figure 23). Therefore, capacitor  $C_{out}$  provides the current for the new load condition (dashed arrow).  $C_{out}$  now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at  $R_{ESR}$ . This voltage is shown as  $V_{ESR}$  in Figure 22.

When  $C_{out}$  is conducting current to the load, initial voltage at the load will be  $V_{out} = V_{C_{out}} - V_{ESR}$ . Due to the discharge of  $C_{out}$ , the output voltage  $V_{out}$  will drop continuously until the response time  $t_1$  of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as  $t_2$  in Figure 23.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

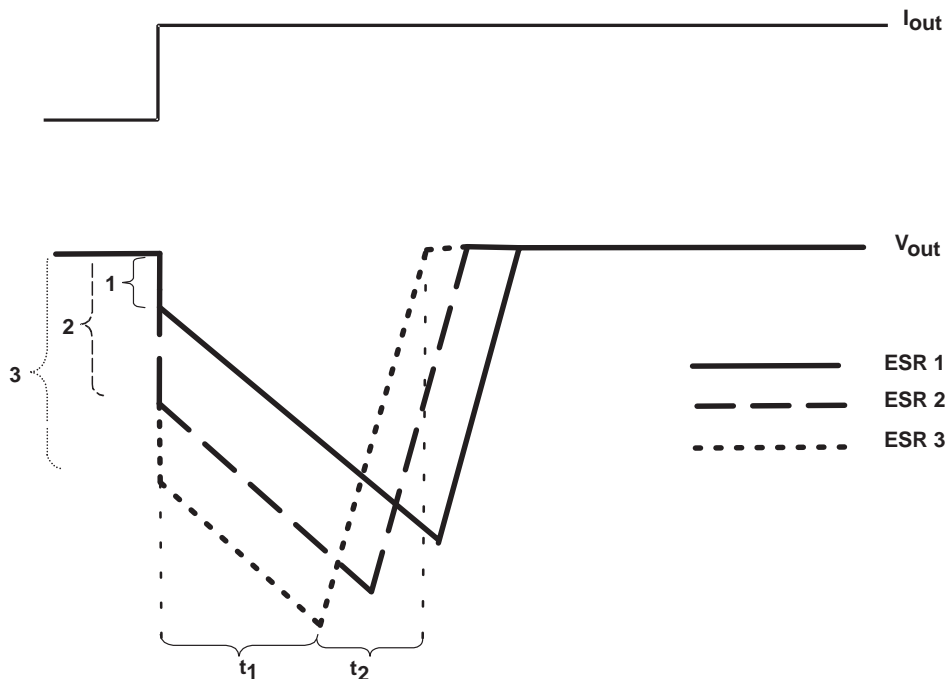


Figure 23. – Correlation of Different ESRs and Their Influence to the Regulation of  $V_{out}$  at a Load Step From Low-to-High Output Current

**TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH  $\overline{\text{RESET}}$  OUTPUT**  
**TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT**  
**250-mA LDO REGULATORS WITH INTEGRATED RESET OR PG**

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**APPLICATION INFORMATION**

**programming the TPS77x01 adjustable LDO regulator**

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 28. The output voltage is calculated using:

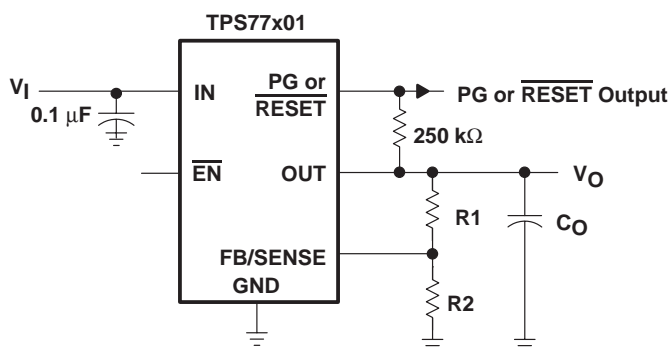
$$V_O = V_{\text{ref}} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where:

$$V_{\text{ref}} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7- $\mu\text{A}$  divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose  $R2 = 30.1 \text{ k}\Omega$  to set the divider current at 7  $\mu\text{A}$  and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R2 \tag{2}$$



**OUTPUT VOLTAGE PROGRAMMING GUIDE**

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	174	169	k $\Omega$
3.3 V	287	169	k $\Omega$
3.6 V	324	169	k $\Omega$

**NOTE:** To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

**Figure 24. TPS77x01 Adjustable LDO Regulator Programming**

## APPLICATION INFORMATION

### regulator protection

The TPS773xx or TPS774xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS773xx or TPS774xx also features internal current limiting and thermal protection. During normal operation, the TPS773xx or TPS774xx limits output current to approximately 0.9 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, i.e., 266.2°C/W for the 8-terminal MSOP with no airflow.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

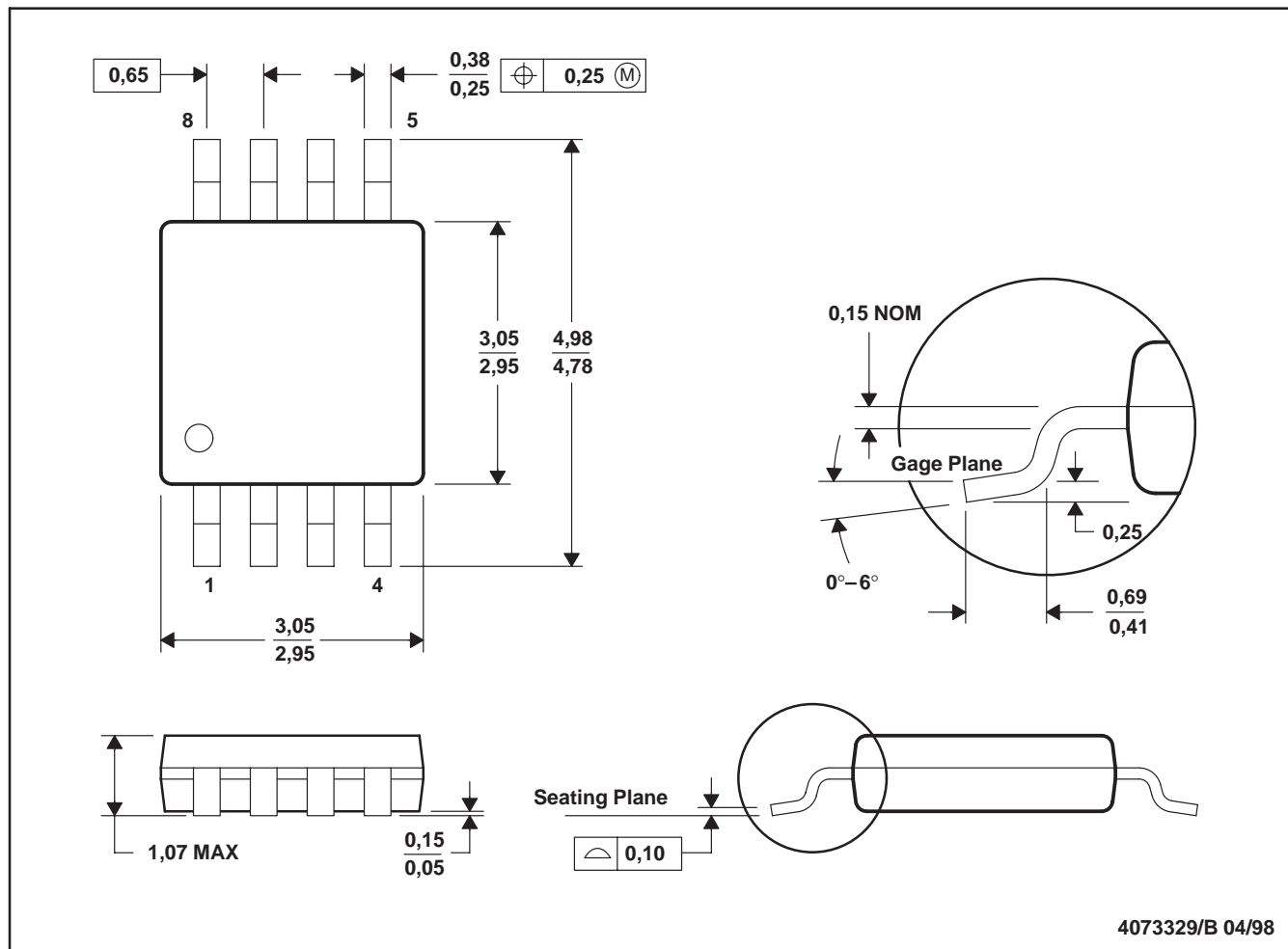
TPS77301, TPS77318, TPS77327, TPS77328, TPS77333 WITH RESET OUTPUT  
 TPS77401, TPS77418, TPS77427, TPS77428, TPS77433 WITH POWER GOOD OUTPUT  
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MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/B 04/98

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-187

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