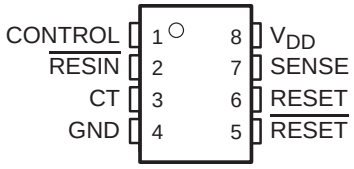
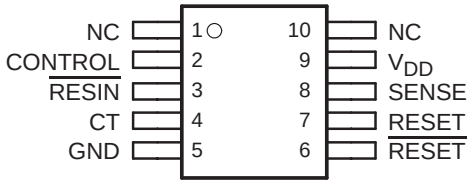
SLVS087K – DECEMBER 1994 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**
- **Temperature Range . . . –40°C to 125°C**

D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

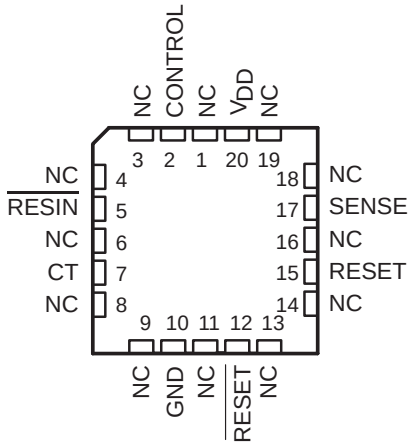
$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

FK PACKAGE
(TOP VIEW)



Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

description (continued)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{CS}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxI is characterized for operation over a temperature range of –40°C to 85°C; the TLC77xxQ is characterized for operation over a temperature range of –40°C to 125°C; and the TLC77xxM is characterized for operation over the full Military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE (V)	PACKAGED DEVICES					
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC DUAL FLATPACK (U)	PLASTIC DIP (P)	THIN SHRINK SMALL OUTLINE (PW)‡
–40°C to 85°C	1.1	TLC7701ID	—	—	—	TLC7701IP	TLC7701IPW
	2.25	TLC7725ID	—	—	—	TLC7725IP	TLC7725IPW
	2.63	TLC7703ID	—	—	—	TLC7703IP	TLC7703IPW
	2.93	TLC7733ID	—	—	—	TLC7733IP	TLC7733IPW
	4.55	TLC7705ID	—	—	—	TLC7705IP	TLC7705IPW
–40°C to 125°C	1.1	TLC7701QD	—	—	—	TLC7701QP	TLC7701QPW
	2.25	TLC7725QD	—	—	—	TLC7725QP	TLC7725QPW
	2.63	TLC7703QD	—	—	—	TLC7703QP	TLC7703QPW
	2.93	TLC7733QD	—	—	—	TLC7733QP	TLC7733QPW
	4.55	TLC7705QD	—	—	—	TLC7705QP	TLC7705QPW
–55°C to 125°C	2.93	—	TLC7733MFK	TLC7733MJG	—	—	—
	4.55	—	TLC7705MFK	TLC7705MJG	TLC7705MU	—	—

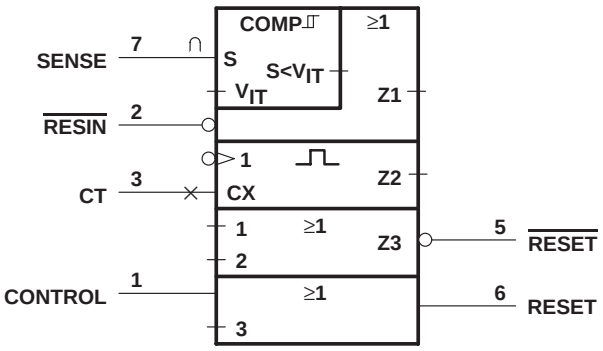
† The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TLC7705QPWLE).

FUNCTION TABLE

CONTROL	$\overline{RESIN}$	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L§	H§
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H§

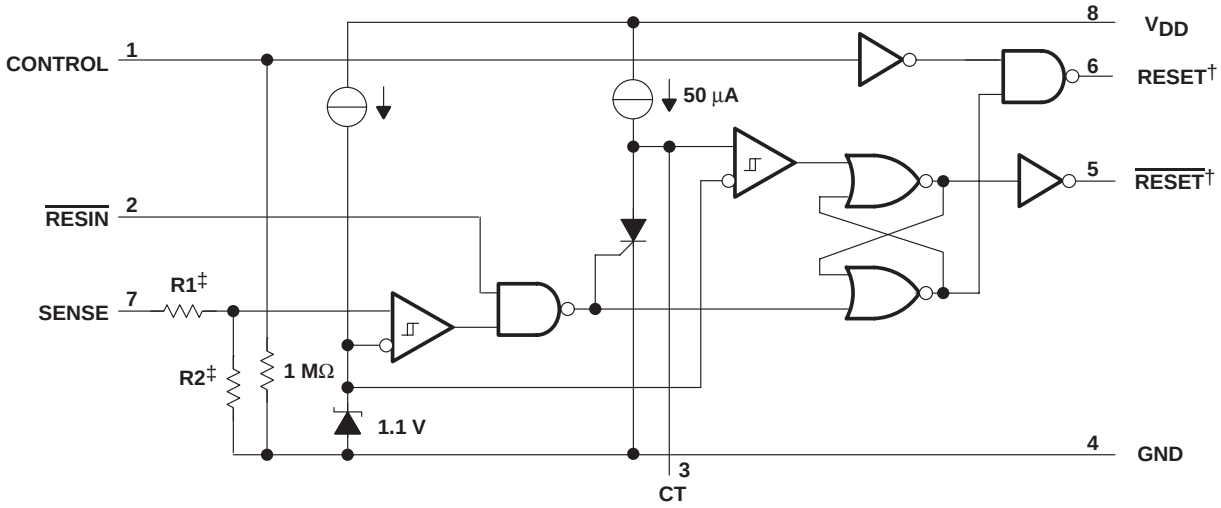
§ RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.

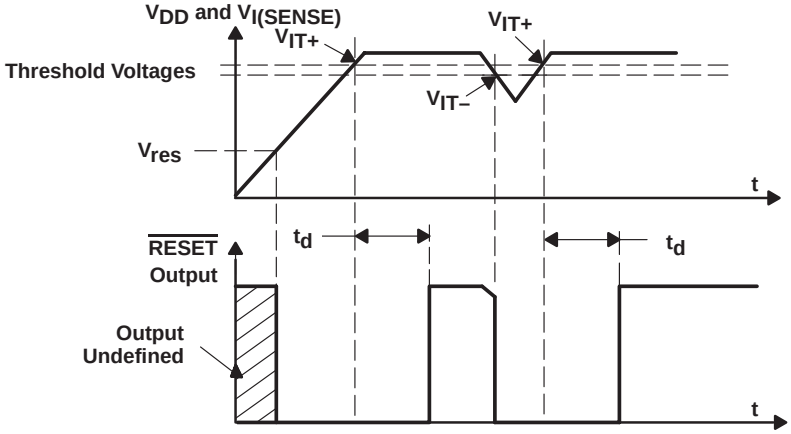
functional block diagram



† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7725	600 kΩ	600 kΩ
TLC7703	698 kΩ	502 kΩ
TLC7733	750 kΩ	450 kΩ
TLC7705	910 kΩ	290 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, CONTROL, $\overline{\text{RESIN}}$, SENSE (see Note 1) . . . . . –0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 10 mA
Maximum high output current, I_{OH} . . . . . –10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxI . . . . . –40°C to 85°C
TL77xxQ . . . . . –40°C to 125°C
TL77xxM . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW	525 mW	4.2 mW/°C	273 mW	105 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Input voltage, V_I		0	V_{DD}	V
High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IH}		$0.7\times V_{DD}$		V
Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IL}			$0.2\times V_{DD}$	V
High-level output current, I_{OH}	$V_{DD} \ge 2.7$ V		–2	mA
Low-level output current, I_{OL}	$V_{DD} \ge 2.7$ V		2	mA
Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A	TLC77xxI	–40	85	°C
	TLC77xxQ	–40	125	
Operating free-air temperature range, T_A	TLC77xxM	–55	125	°C

‡ To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} – 0.3$ V.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TLC77xx MIN	TLC77xx TYP†	TLC77xx MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –20 μA		V_{DD} = 2 V	1.8			V
				V_{DD} = 2.7 V	2.5			
				V_{DD} = 4.5 V	4.3			
		I_{OH} = –2 mA		V_{DD} = 4.5 V	3.7			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA		V_{DD} = 2 V			0.2	V
				V_{DD} = 2.7 V			0.2	
				V_{DD} = 4.5 V			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16	V
			TLC7725		2.18	2.25	2.32	
			TLC7703		2.56	2.63	2.70	
			TLC7733		2.86	2.93	3	
			TLC7705		4.47	4.55	4.63	
V_{hys}	Hysteresis voltage, SENSE		TLC7701	V_{DD} = 2 V to 6 V		30		mV
			TLC7725	V_{DD} = 2 V to 6 V		70		mV
			TLC7703, TLC7733, TLC7705					
V_{res}	Power-up reset voltage‡			I_{OL} = 20 μA			1	V
I_I	Input current	RESIN		V_I = 0 V to V_{DD}			2	μA
		CONTROL		V_I = V_{DD}		7	15	
		SENSE		V_I = 5 V		5	10	
		SENSE, TLC7701 only		V_I = 5 V			2	
I_{DD}	Supply current			RESIN = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open		9	16	μA
$I_{DD(d)}$	Supply current during t_d			V_{DD} = 5 V, V_{CT} = 0 , RESIN = V_{DD}, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	μA
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be connected near the supply terminals.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS		TLC77xxM			UNIT
						MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 μA		V_{DD} = 2 V,	T_A = 25°C	1.8			V
					T_A = –55°C to 125°C	1.7			
				V_{DD} = 2.7 V	T_A = 25°C	2.5			
					T_A = –55°C to 125°C	2.3			
				V_{DD} = 4.5 V	T_A = 25°C	4.3			
					T_A = –55°C to 125°C	4.2			
		I_{OH} = –2 mA		V_{DD} = 4.5 V	T_A = 25°C	3.7			
					T_A = –55°C to 125°C	3.6			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA		V_{DD} = 2 V	T_A = 25°C			0.2	V
					T_A = –55°C to 125°C			0.2	
				V_{DD} = 2.7 V	T_A = 25°C			0.2	
					T_A = –55°C to 125°C			0.2	
				V_{DD} = 4.5 V	T_A = 25°C			0.2	
					T_A = –55°C to 125°C			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V	T_A = 25°C			0.5	
					T_A = –55°C to 125°C			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7733	V_{DD} = 2 V to 6 V		2.86	2.93	3.1	V
			TLC7705			4.3	4.5	4.8	
V_{hys}	Hysteresis voltage, SENSE			V_{DD} = 2 V to 6 V	V_{DD} = 2 V to 6 V		70		mV
V_{res}	Power-up reset voltage‡			I_{OL} = 20 μA				1	V
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 0 V to V_{DD}				2	μA
		CONTROL		V_I = V_{DD}			7	15	
		SENSE		V_I = 5 V			5	10	
		SENSE, TLC7701 only		V_I = 5 V				2	
I_{DD}	Supply current			$\overline{\text{RESIN}}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open			9	16	μA
$I_{DD(d)}$	Supply current during t_d		TLC7733	$\overline{V_{CT}}$ = 0, $\overline{\text{RESIN}}$ = V_{DD}, CONTROL = 0 V, SENSE = V_{DD}, Outputs open	V_{DD} = 3.3 V			250	μA
			TLC7705		V_{DD} = 5 V		120	150	
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}			50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = 25°C

PARAMETER		MEASURED		TEST CONDITIONS	TLC77xx			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, C_T = 100 nF, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						5	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						40	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, $\overline{\text{SENSE}}$ = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CT = NC†			38	ns
t_{PHL}	Propagation delay time, high-to-low-level output						38	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V,	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

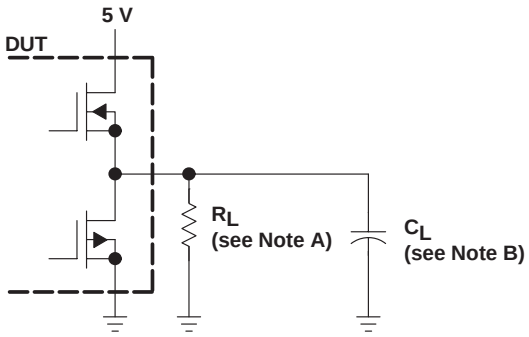
† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF

PARAMETER		MEASURED		TEST CONDITIONS	T_A	TLC77xxM			UNIT
		FROM (INPUT)	TO (OUTPUT)			MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, C_T = 100 nF, See timing diagram	25°C	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			5	µs
					Full range			7	
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			5	µs
					Full range			7	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			45	ns
					Full range			65	
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			40	ns
					Full range			60	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, $\overline{\text{SENSE}}$ = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CT = NC†	25°C			38	ns
					Full range			58	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			38	ns
					Full range			58	
	Low-level minimum pulse duration	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min – 0.2 V,	Full range	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.4 V, V_{IH} = 2.7 V		1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%	Full range		8		ns/V
t_f	Fall time			90% to 10%			4		

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, R_L = 2 kΩ.
B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations

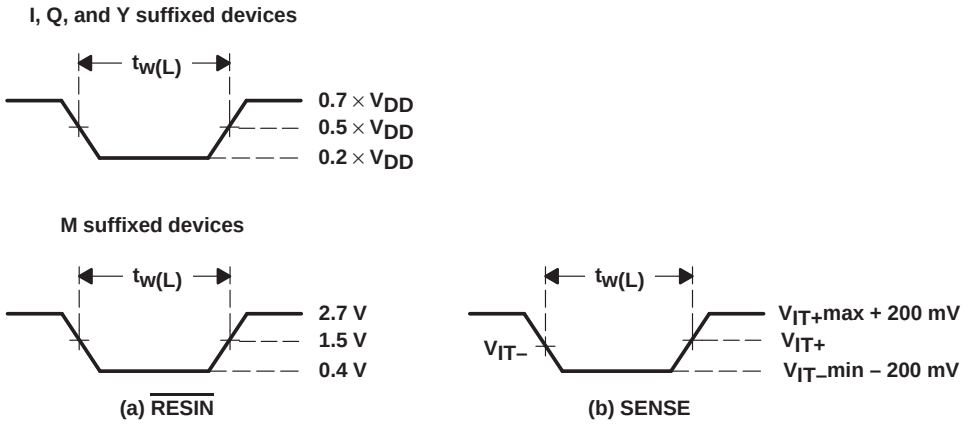


Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
TEMPERATURE

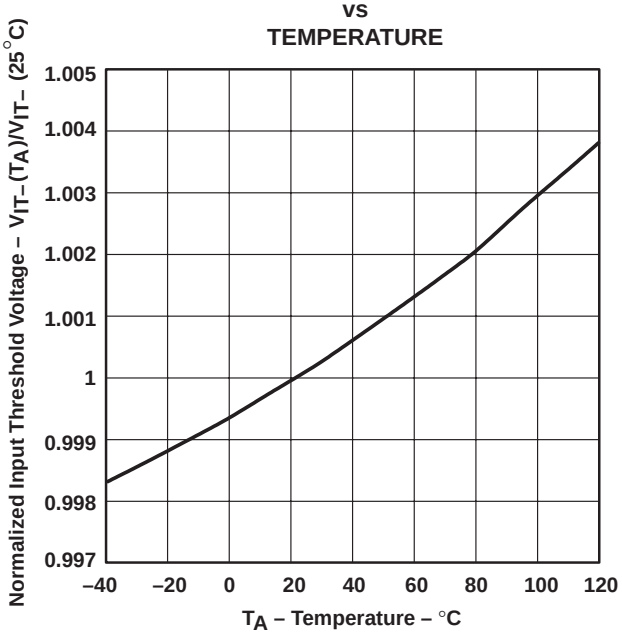


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

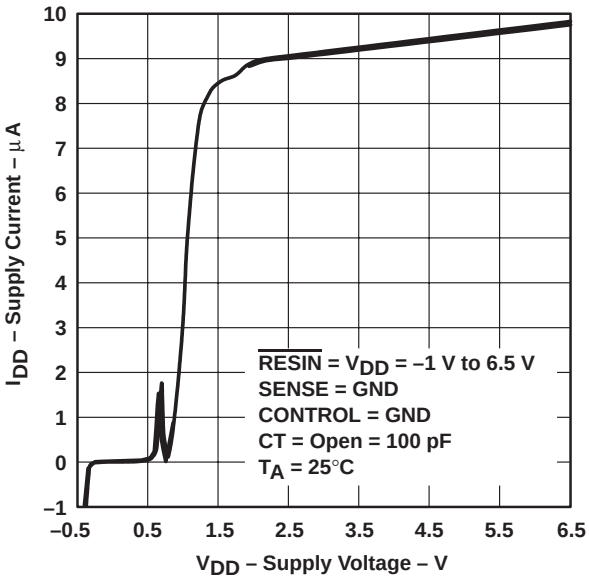


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

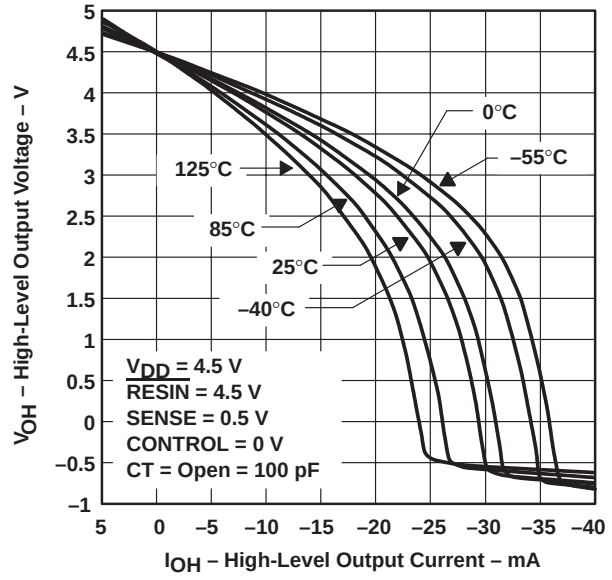


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

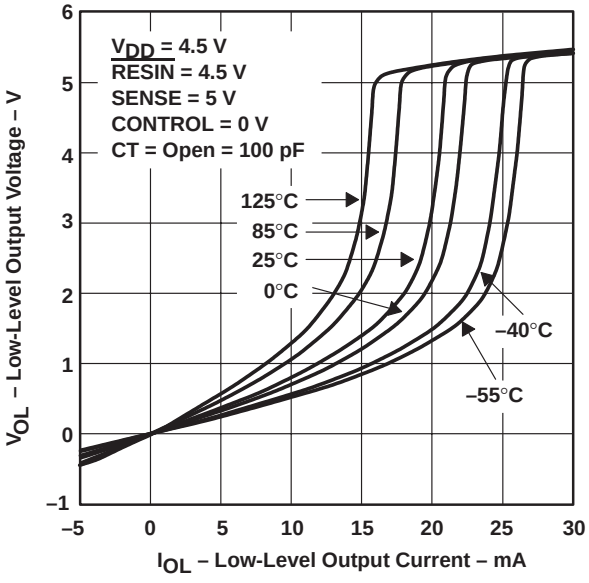


Figure 6

TYPICAL CHARACTERISTICS

**INPUT CURRENT
vs
INPUT VOLTAGE AT SENSE**

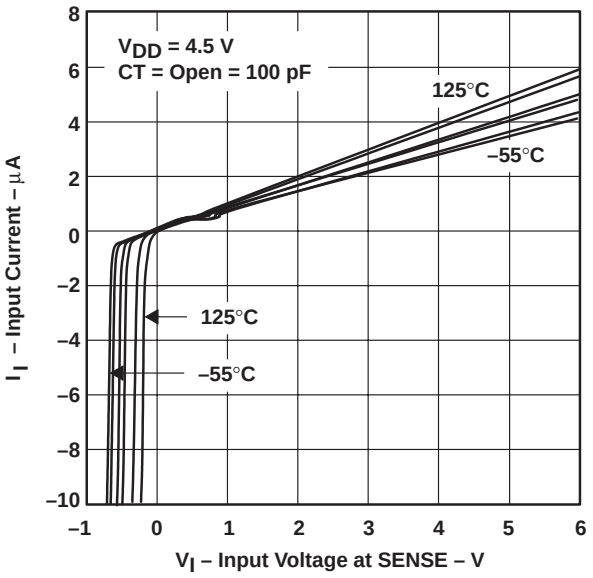


Figure 7

**MINIMUM PULSE DURATION AT SENSE
vs
SENSE THRESHOLD OVERDRIVE**

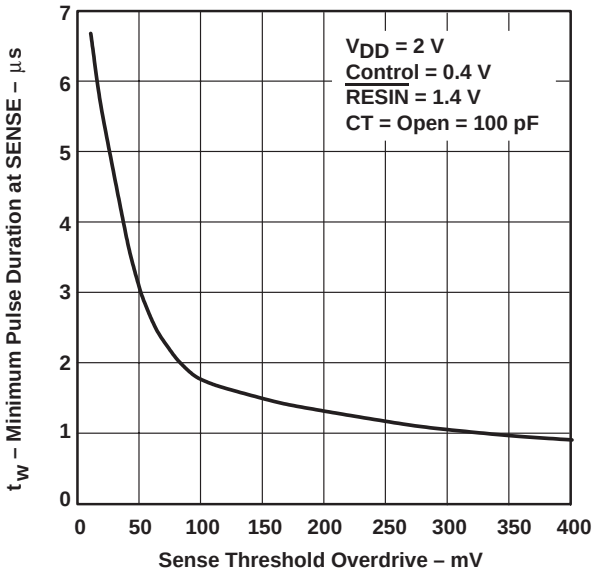


Figure 8

APPLICATION INFORMATION

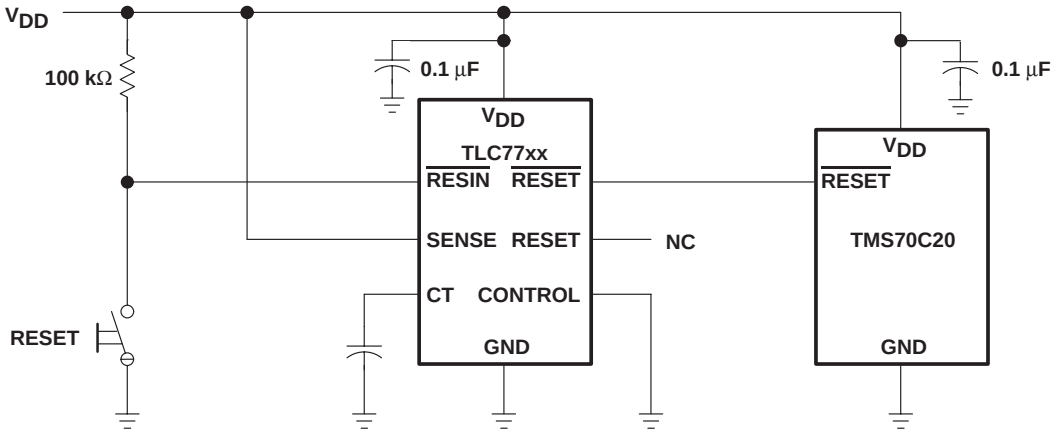


Figure 9. Reset Controller in a Microcomputer System

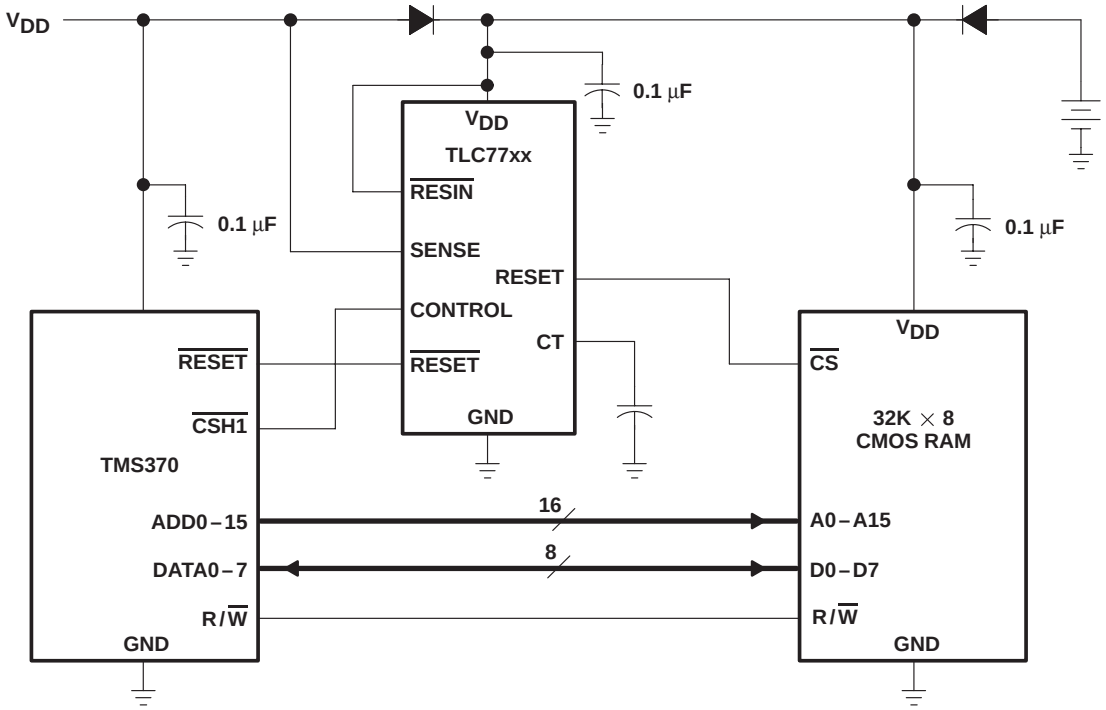
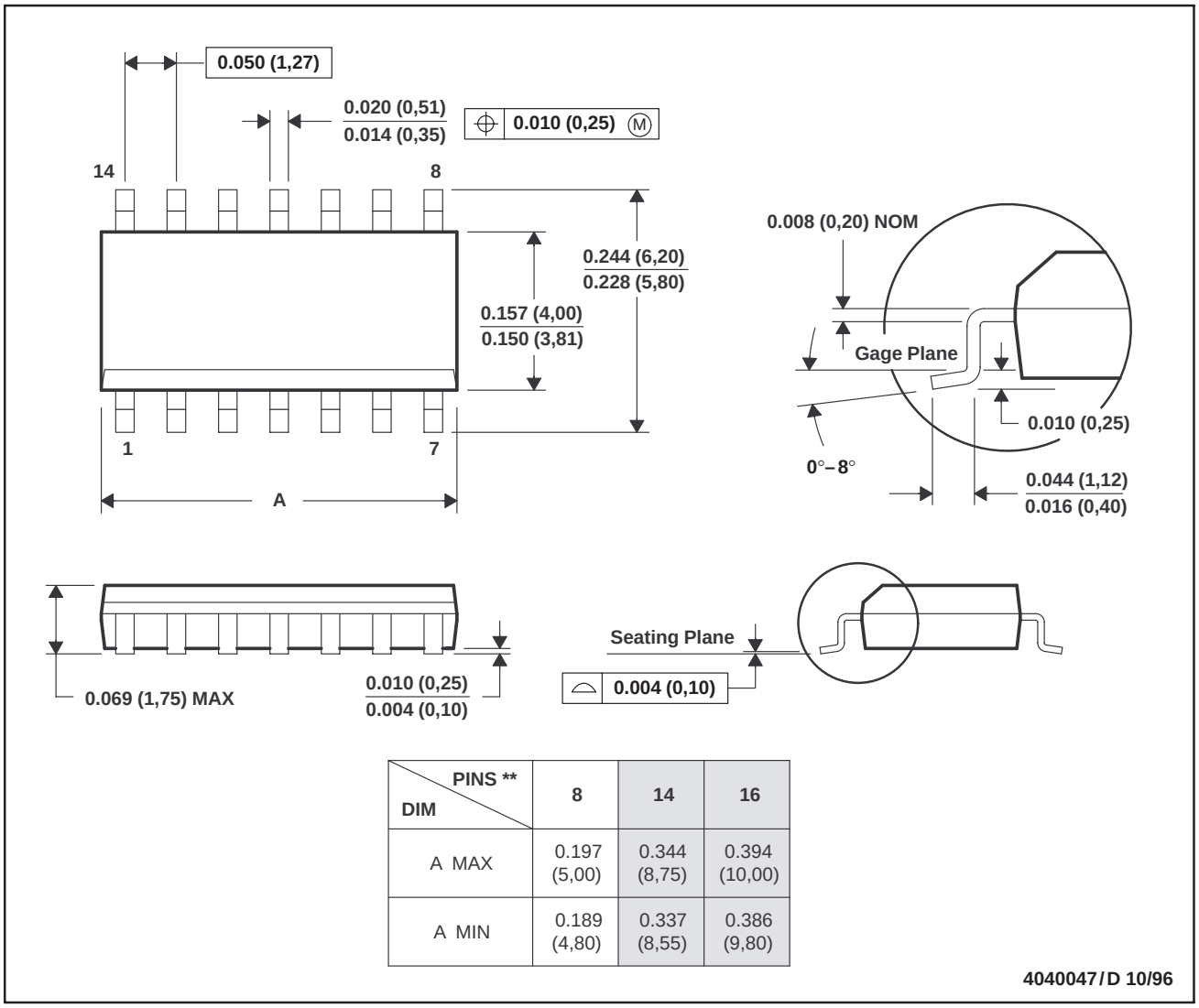


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

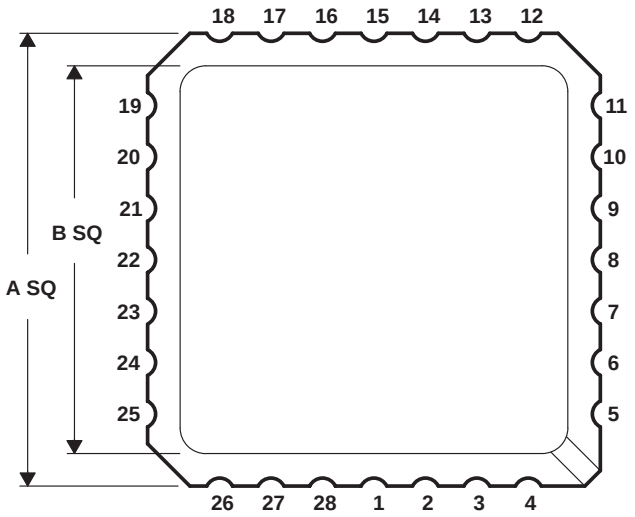
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

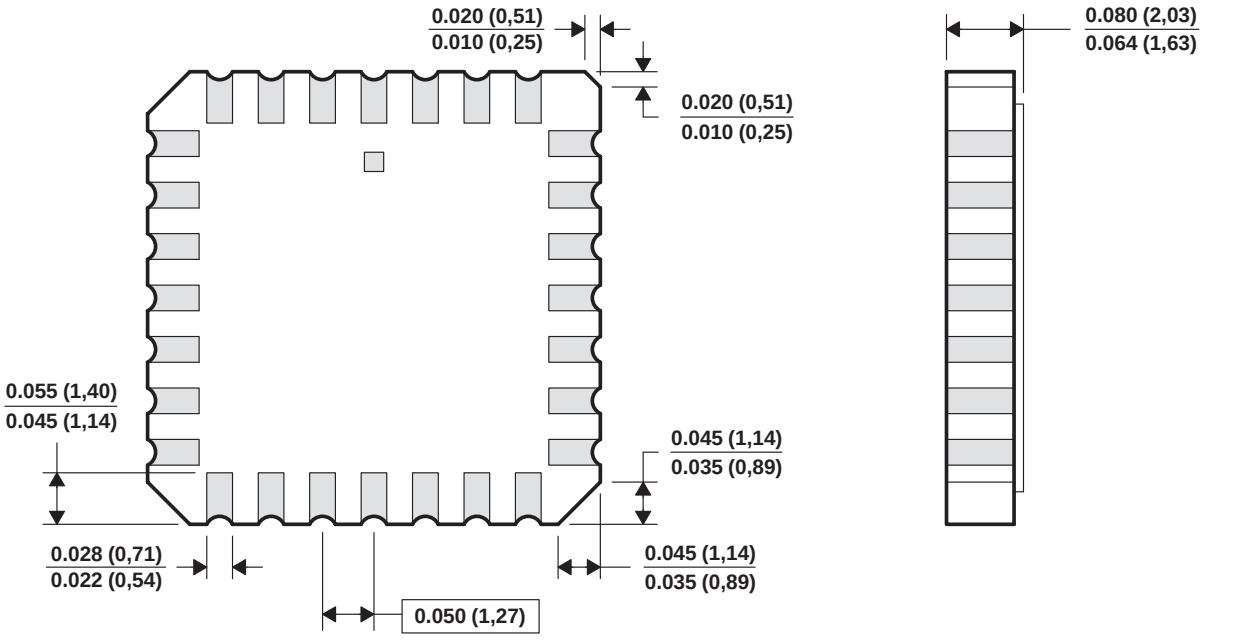
MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

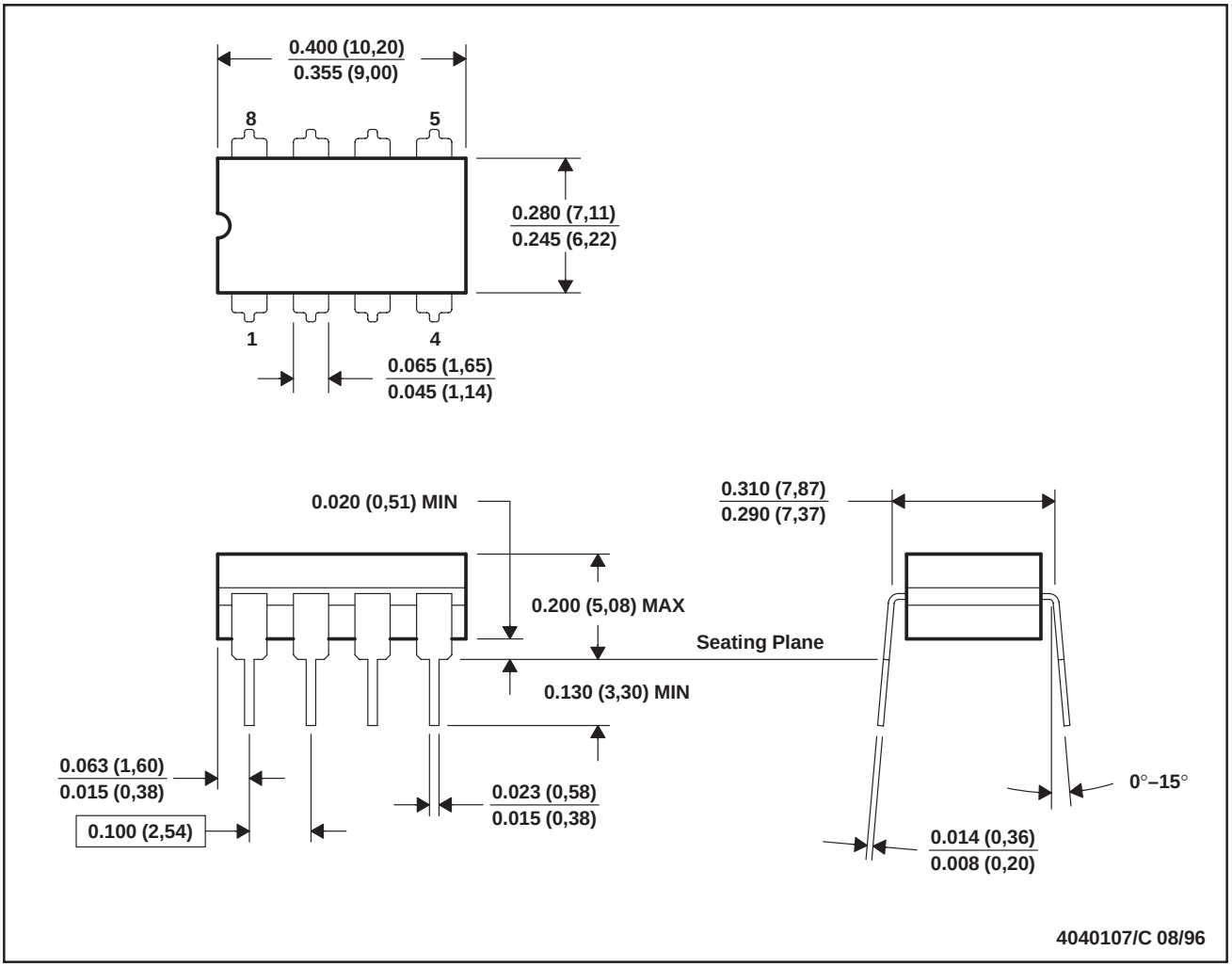


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

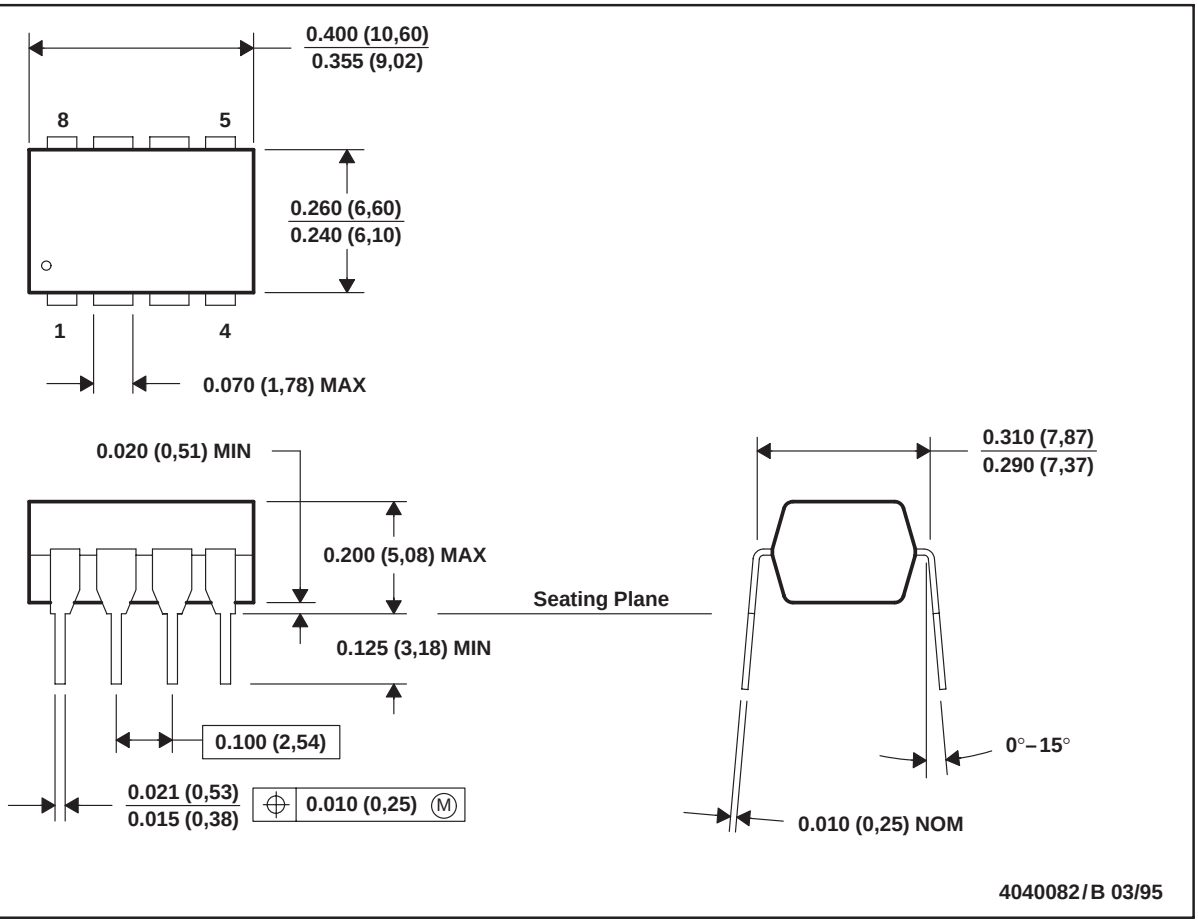
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

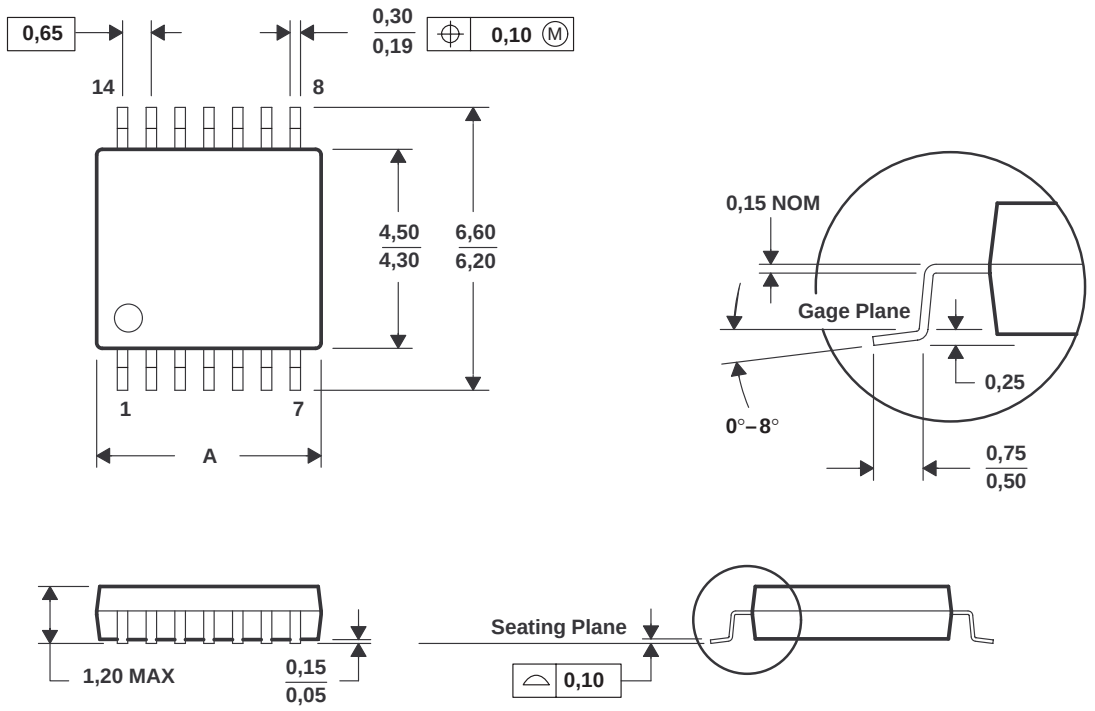


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



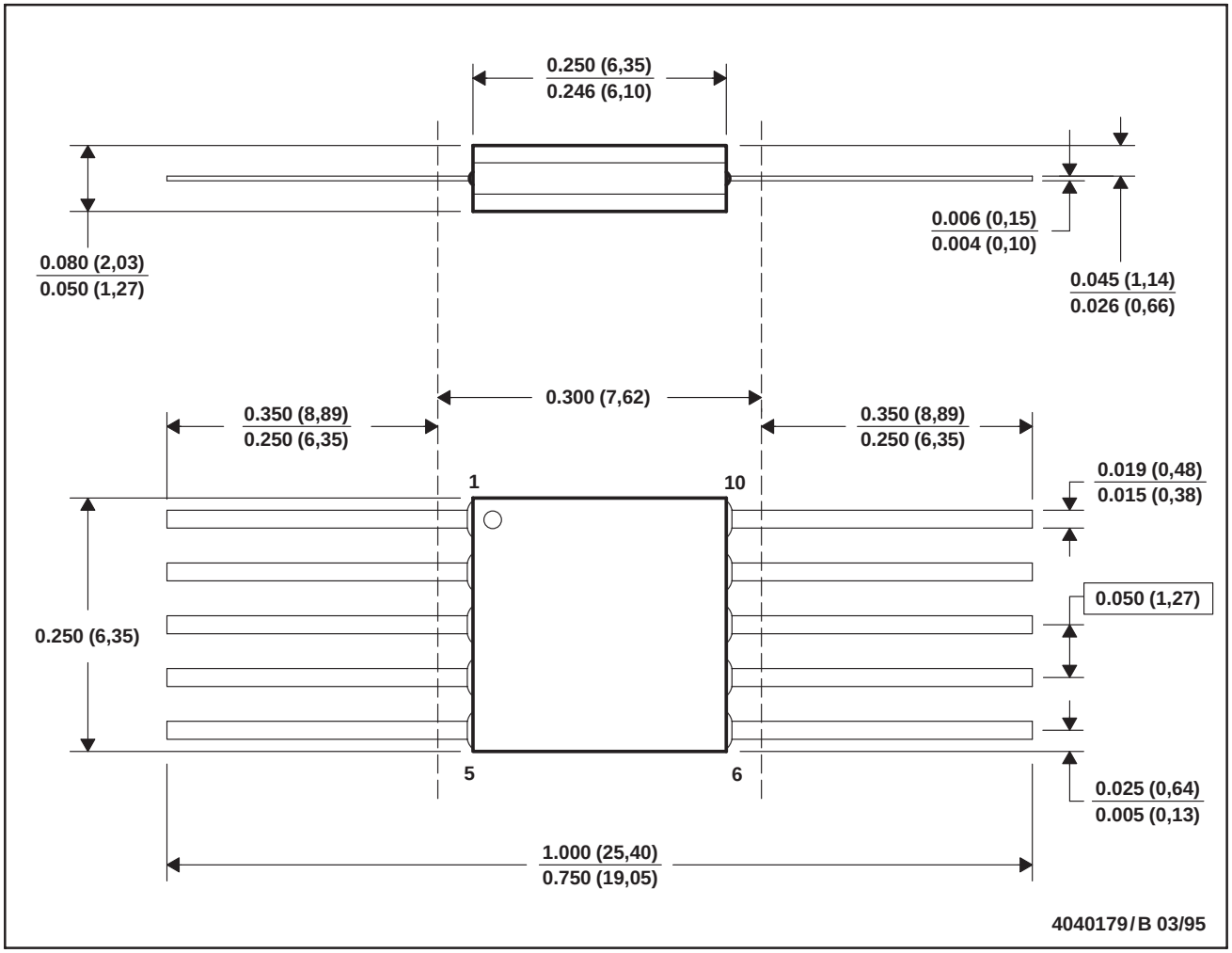
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

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