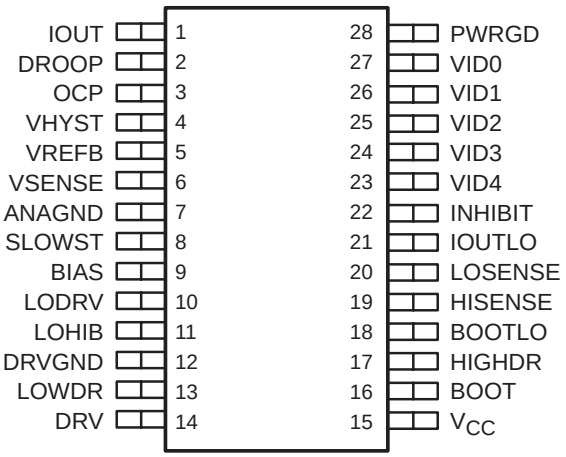
# TPS5211
# HIGH FREQUENCY PROGRAMMABLE HYSTERETIC REGULATOR CONTROLLER

SLVS243 – SEPTEMBER 1999

- **700 KHz Operation**
- **1.25 MHz Operation With External Driver**
- **1.5% Reference Over Full Operating Temperature Range**
- **Synchronous Rectifier Driver for Greater Than 90% Efficiency**
- **Programmable Reference Voltage Range of 1.3 V to 3.5 V**
- **User–Selectable Hysteretic Type Control**
- **Droop Compensation for Improved Load Transient Regulation**
- **Adjustable Overcurrent Protection**
- **Programmable Softstart**
- **Overvoltage Protection**
- **Active Deadtime Control**
- **Power Good Output**
- **Internal Bootstrap Schottky Diode**
- **Low Supply Current . . . 3-mA Typ**
- **Reduced System Component Count and Size**

**PWP PACKAGE**
**(TOP VIEW)**




## description

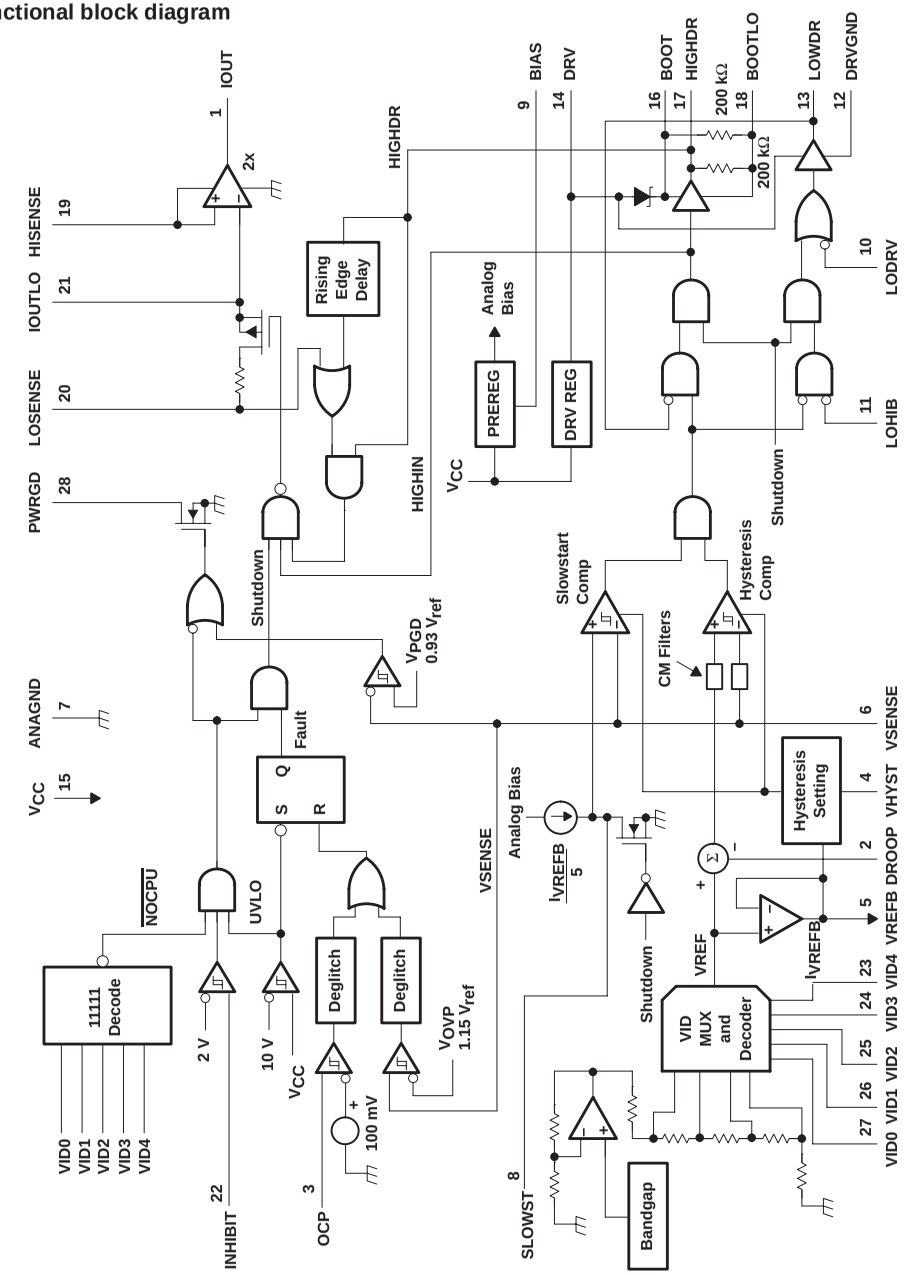
The TPS5211 is a hysteretic regulator controller which provides an accurate, programmable supply voltage to microprocessors. An internal 5-bit DAC is used to program the reference voltage to within a range of 1.3 V to 3.5 V. The output voltage can be set to equal the reference voltage or some multiple of the reference voltage. A hysteretic controller with user-selectable hysteresis and programmable droop compensation is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. The softstart current source is proportional to the reference voltage, thereby eliminating variation of the softstart timing when changes are made to the output voltage. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops 7% below the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures the 12-V supply voltage and system supply voltage (5 V or 3.3 V) is within proper operating limits before the controller starts. Single-supply (12 V) operation is easily accomplished using a low-current divider for the required 5-V signals. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5211 is available in a 28-pin TSSOP PowerPAD™ package. It operates over a junction temperature range of 0°C to 125°C.

**AVAILABLE OPTIONS**

| $T_J$ | PACKAGE |
|---|---|
| | **TSSOP (PWP)** |
| 0°C to 125°C | TPS5211PWPR |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## functional block diagram



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## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| ANAGND | 7 | | Analog ground |
| BIAS | 9 | O | Analog BIAS pin. A 1-μF ceramic capacitor should be connected from BIAS to ANAGND. |
| BOOT | 16 | I | Bootstrap. Connect a 1-μF low-ESR capacitor from BOOT to BOOTLO. |
| BOOTLO | 18 | O | Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration. |
| DROOP | 2 | I | Droop voltage. Voltage input used to set the amount of output-voltage set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND. |
| DRV | 14 | O | Drive regulator for the FET drivers. A 1-μF ceramic capacitor should be connected from DRV to DRVGND. |
| DRVGND | 12 | | Drive ground. Ground for FET drivers. Connect to FET PWRGND. |
| HIGHDR | 17 | O | High drive. Output drive to high-side power switching FETs |
| HISENSE | 19 | I | High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain. |
| INHIBIT | 22 | I | Disables the drive signals to the MOSFET drivers. Can also serve as UVLO for system logic supply (either 3.3 V or 5 V). |
| IOUT | 1 | O | Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times R_{ds(on)} \times IOUT$. In applications requiring very accurate current sensing, a sense resistor should be connected between the input supply and the drain of the high-side FETs. |
| IOUTLO | 21 | O | Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 μF and 0.1 μF. |
| LODRV | 10 | I | Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low. |
| LOHIB | 11 | I | Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode. |
| LOSENSE | 20 | I | Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain. |
| LOWDR | 13 | O | Low drive. Output drive to synchronous rectifier FETs |
| OCP | 3 | I | Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND. |
| PWRGD | 28 | O | Power good. Power good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output. |
| SLOWST | 8 | O | Slowstart (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$ |
| $V_{CC}$ | 15 | | 12-V supply. A 1-μF ceramic capacitor should be connected from $V_{CC}$ to DRVGND. |
| VHYST | 4 | I | HYSTERESIS set pin. The hysteresis is set with a resistor divider from $V_{REFB}$ to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$ |
| VID0 | 27 | I | Voltage identification input 0 |
| VID1 | 26 | I | Voltage identification input 1 |
| VID2 | 25 | I | Voltage identification input 2 |
| VID3 | 24 | I | Voltage identification input 3 |
| VID4 | 23 | I | Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from $V_{CC}$. |
| VREFB | 5 | O | Buffered reference voltage from VID network |
| VSENSE | 6 | I | Voltage sense input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise. |

## detailed description

### $V_{REF}$

The reference/voltage identification (VID) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VID terminals are inputs to the VID selection network and are TTL-compatible inputs internally pulled up to 5 V by a resistor divider connected to $V_{CC}$. The VID codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 3.5 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VID settings. Voltages higher than $V_{REF}$ can be implemented using an external divider. Refer to Table 1 for the VID code settings. The output voltage of the VID network, $V_{REF}$, is within ±1.5% of the nominal setting over the VID range of 1.3 V to *2*.5 V, including a junction temperature range of 5°C to +125°C, and a $V_{CC}$ supply voltage range of 11.4 V to 12.6 V. The output of the reference/VID network is indirectly brought out through a buffer to the $V_{REFB}$ pin. The voltage on this pin will be within 5mV of $V_{REF}$. It is not recommended to drive loads with $V_{REFB}$, other than setting the hysteresis of the hysteretic comparator, because the current drawn from $V_{REFB}$ sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

### hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on $V_{REF}$. The 2 external resistors form a resistor divider from $V_{REFB}$ to ANAGND, with the output voltage connecting to the VHYST pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the VREFB and VHYST pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.

### low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is internally connected to the DRV regulator.

### high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or $V_{CC}$. The rms current through the drivers output should not exceed 110 mA. Refer to the application information section to determine how to calculate an operating frequency to meet this requirement.

### deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

## detailed description (continued)

### current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 μF and 0.1 μF. Internal logic controls the turnon and turnoff of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

### droop compensation

The droop compensation network reduces the load transient overshoot/undershoot on $V_O$, relative to $V_{REF}$. $V_O$ is programmed to a voltage greater than $V_{REF}$ by an external resistor divider from $V_O$ to VSENSE to reduce the undershoot on $V_O$ during a low-to-high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage on DROOP from $V_{REF}$. The voltage on IOUT is divided with an external resistor divider, and connected to DROOP.

### inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. The 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

### $V_{CC}$ undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the $V_{CC}$ supply is below the 10-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When $V_{CC}$ exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

### slowstart

The slowstart circuit controls the rate at which $V_O$ powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of $C_{SLOWST}$ is proportional to the reference voltage. By making the charging current proportional to $V_{REF}$, the power-up time for $V_O$ will be independent of $V_{REF}$. Thus, $C_{SLOWST}$ can remain the same value for all VID settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(VREFB) / 5 \quad \text{(amps)}$$

Where I(VREFB) is the current flowing out of VREFB.

It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the VREFB circuit is 500 μA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad \text{(seconds)}$$

Where $R_{VREFB}$ is the total external resistance from $V_{REFB}$ to ANAGND.

## detailed description (continued)

### power good

The power-good circuit monitors for an undervoltage condition on $V_O$. If $V_O$ is 7% below $V_{REF}$, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

### overvoltage protection

The overvoltage protection (OVP) circuit monitors $V_O$ for an overvoltage condition. If $V_O$ is 15% above $V_{REF}$, then a fault latch is set and both output drivers are turned off. The latch will remain set until $V_{CC}$ goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted fault across the high-side power FET.

### overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until $V_{CC}$ goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

### drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1-µF ceramic capacitor from DRV to DRVGND.

### LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5211 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with $V_{in}$ should be added to disconnect the short-circuit.

**Table 1. Voltage Identification Codes**

| VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V) | | | | | $V_{REF}$ |
|---|---|---|---|---|---|
| VID4 | VID3 | VID2 | VID1 | VID0 | (Vdc) |
| 0 | 1 | 1 | 1 | 1 | 1.30 |
| 0 | 1 | 1 | 1 | 0 | 1.35 |
| 0 | 1 | 1 | 0 | 1 | 1.40 |
| 0 | 1 | 1 | 0 | 0 | 1.45 |
| 0 | 1 | 0 | 1 | 1 | 1.50 |
| 0 | 1 | 0 | 1 | 0 | 1.55 |
| 0 | 1 | 0 | 0 | 1 | 1.60 |
| 0 | 1 | 0 | 0 | 0 | 1.65 |
| 0 | 0 | 1 | 1 | 1 | 1.70 |
| 0 | 0 | 1 | 1 | 0 | 1.75 |
| 0 | 0 | 1 | 0 | 1 | 1.80 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.90 |

**Table 1. Voltage Identification Codes (Continued)**

| VID TERMINALS (0 = GND, 1 = floating or pull-up to 5 V) | | | | | $V_{REF}$ |
|---|---|---|---|---|---|
| VID4 | VID3 | VID2 | VID1 | VID0 | (Vdc) |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.00 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | No CPU |
| 1 | 1 | 1 | 1 | 0 | 2.10 |
| 1 | 1 | 1 | 0 | 1 | 2.20 |
| 1 | 1 | 1 | 0 | 0 | 2.30 |
| 1 | 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 1 | 0 | 2.50 |
| 1 | 1 | 0 | 0 | 1 | 2.60 |
| 1 | 1 | 0 | 0 | 0 | 2.70 |
| 1 | 0 | 1 | 1 | 1 | 2.80 |
| 1 | 0 | 1 | 1 | 0 | 2.90 |
| 1 | 0 | 1 | 0 | 1 | 3.00 |
| 1 | 0 | 1 | 0 | 0 | 3.10 |
| 1 | 0 | 0 | 1 | 1 | 3.20 |
| 1 | 0 | 0 | 1 | 0 | 3.30 |
| 1 | 0 | 0 | 0 | 1 | 3.40 |
| 1 | 0 | 0 | 0 | 0 | 3.50 |

## absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note1) . . . . . –0.3 V to 14 V
Input voltage range: BOOT to DRVGND (High-side Driver ON) . . . . . –0.3 V to 30 V
BOOT to HIGHDRV . . . . . –0.3 V to 15 V
BOOT to BOOTLO . . . . . –0.3 V to 15 V
INHIBIT, VIDx, LODRV . . . . . –0.3 V to 7.3 V
PWRGD, OCP, DROOP . . . . . –0.3 V to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE . . . . . –0.3 V to 14 V
VSENSE . . . . . –0.3 V to 5 V
Voltage difference between ANAGND and DRVGND . . . . . ±0.5 V
Output current, $V_{REFB}$ . . . . . 0.5 mA
Short circuit duration, DRV . . . . . Continuous
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ . . . . . 0°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| PWP | 1150 mW | 11.5 mW/°C | 630 mW | 460 mW |

### recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | 11.4 | 13 | V |
| Input voltage, BOOT to DRVGND | 0 | 28 | V |
| Input voltage, BOOT to BOOTLO | 0 | 13 | V |
| Input voltage, INHIBIT, VIDx, LODRV, PWRGD, OCP, DROOP | 0 | 6 | V |
| Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE | 0 | 13 | V |
| Input voltage, VSENSE | 0 | 4.5 | V |
| Voltage difference between ANAGND and DRVGND | 0 | ±0.2 | V |
| Output current, $V_{REFB}$† | 0 | 0.4 | mA |

† Not recommended to load $V_{REFB}$ other than to set hystersis since $I_{VREFB}$ sets slowstart time.

### electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 12 V, $I_{DRV}$ = 0 A (unless otherwise noted)

#### reference/voltage identification

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REF}$ | Cumulative reference accuracy (see Note 2) | $V_{CC}$ = 11.4 to 12.6 V, 1.3 V ≤ $V_{REF}$ ≤ 3.5 V | –0.015 | | 0.015 | V/V |
| VIDx | High-level input voltage | | 2.25 | | | V |
| VIDx | Low-level input voltage | | | | 1 | V |
| $V_{REFB}$ | Output voltage | $I_{VREFB}$ = 50 µA | $V_{REF}$–5mV | $V_{REF}$ | $V_{REF}$+5mV | V |
| | Output regulation | 10 µA ≤ $I_O$ ≤ 500 µA | | 2 | | mV |
| VIDx | Input resistance | VIDx = 0 V | 36 | 73 | 95 | kΩ |
| | Input pull-up voltage divider | | 4.8 | 4.9 | 5 | V |

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.
3. This parameter is ensured by design and is not production tested.

#### power good

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Undervoltage trip threshold | | 90 | 93 | 95 | %$V_{REF}$ |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 5 mA | | 0.5 | 0.75 | V |
| $I_{OH}$ | High-level input current | $V_{PWRGD}$ = 6 V | | 1 | | µA |
| $V_{hys}$ | Hysteresis voltage | | 1.3 | 2.9 | 4.5 | %$V_{REF}$ |

#### slowstart

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Charge current | $V_{SLOWST}$ = 0.5 V, $V_{VREFB}$ = 1.3 V, $I_{VREFB}$ = 65 µA | 10.4 | 13 | 15.6 | µA |
| Discharge current | $V_{SLOWST}$ = 1 V | | 3 | | mA |
| Comparator input offset voltage | | | | 10 | mV |
| Comparator input bias current | See Note 3 | | 10 | 100 | nA |
| Comparator hysteresis | | –7.5 | | 7.5 | mV |

NOTE 3: This parameter is ensured by design and is not production tested.

## electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 12 V, $I_{DRV}$ = 0 A (unless otherwise noted) (continued)

### hysteretic comparator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input offset voltage | $V_{DROOP}$ = 0 V (see Note 3) | –2.5 | | 2.5 | mV |
| Input bias current | See Note 3 | | | 500 | nA |
| Hysteresis accuracy | $V_{REFB} - V_{HYST}$ = 15 mV (Hysteresis window = 30 mV) | –3.5 | | 3.5 | mV |
| Maximum hysteresis setting | $V_{REFB} - V_{HYST}$ = 30 mV | | 60 | | mV |

NOTE 3: This parameter is ensured by design and is not production tested.

### high-side VDS sensing

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Gain | | | 2 | | V/V |
| | Initial accuracy | $V_{HISENSE}$ = 12 V, $V_{LOSENSE}$ = 11.9 V, Differential input to $V_{ds}$ sensing amp = 100 mV | 194 | | 206 | mV |
| IOUTLO | Sink current | 5 V ≤ $V_{IOUTLO}$ ≤ 13 V | | | 250 | nA |
| IOUT | Source current | $V_{IOUT}$ = 0.5 V, $V_{HISENSE}$ = 12 V, $V_{IOUTLO}$ = 11.5 V | 500 | | | µA |
| IOUT | Sink current | $V_{IOUT}$ = 0.05 V, $V_{HISENSE}$ = 12 V, $V_{IOUTLO}$ = 12 V | 50 | | | µA |
| | Output voltage swing | $V_{HISENSE}$ = 11 V, $R_{IOUT}$ = 10 kΩ | 0 | | 2 | V |
| | | $V_{HISENSE}$ = 4.5 V, $R_{IOUT}$ = 10 kΩ | 0 | | 1.5 | V |
| | | $V_{HISENSE}$ = 3 V, $R_{IOUT}$ = 10 kΩ | 0 | | 0.75 | V |
| LOSENSE | High-level input voltage | $V_{HISENSE}$ = 4.5 V (see Note 3) | 2.85 | | | V |
| | Low-level input voltage | | | | 2.4 | V |
| | Sample/hold resistance | 11.4 V ≤ $V_{HISENSE}$ ≤ 12.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V | 50 | 60 | 80 | Ω |
| | | 4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V | 62 | 85 | 123 | |
| | | 3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V | 67 | 95 | 144 | |
| CMRR | | $V_{HISENSE}$ = 12.6 V to 3 V, $V_{HISENSE} - V_{OUTLO}$ = 100 mV | 69 | 75 | | dB |

NOTE 3. This parameter is ensured by design and is not production tested.

### inhibit

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Start threshold | | 1.9 | 2.1 | 2.35 | V |
| Hysteresis | | 0.08 | 0.1 | 0.12 | V |
| Stop threshold | | 1.85 | | | V |

## electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 12 V, $I_{DRV}$ = 0 A (unless otherwise noted) (continued)

### overvoltage protection

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Overvoltage trip threshold | | 112 | 115 | 120 | $\%V_{REF}$ |
| Hysteresis | See Note 3 | | 10 | | mV |

NOTE 3: This parameter is ensured by design and is not production tested.

### overcurrent protection

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| OCP trip threshold | | 90 | 100 | 110 | mV |
| Input bias current | | | | 100 | nA |

### deadtime

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| LOHIB | High-level input voltage | | 2.4 | | | V |
| | Low-level input voltage | | | | 1.4 | |
| LOWDR | High-level input voltage | See Note 3 | 3 | | | V |
| | Low-level input voltage | See Note 3 | | | 1.7 | |

NOTE 3: This parameter is ensured by design and is not production tested.

### LODRV

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| LODRV | High-level input voltage | | 1.85 | | | V |
| | Low-level input voltage | | | | 0.95 | |

### droop compensation

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Initial accuracy | $V_{DROOP}$ = 50 mV | 46 | | 54 | mV |

### drive regulator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output voltage | 11.4 V ≤ $V_{CC}$ ≤ 12.6 V, $I_{DRV}$ = 120 mA | 7 | | 9 | V |
| Output regulation | 1 mA ≤ $I_{DRV}$ ≤ 50 mA | | 100 | | mV |
| Short-circuit current | | 120 | | | mA |

### bias regulator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output voltage | 11.4 V ≤ $V_{CC}$ ≤ 12.6 V, See Note 4 | 6 | | | V |

NOTE 4: The bias regulator is designed to provide a quiet bias supply for the TPS5211 controller. External loads should not be driven by the bias regulator.

### input undervoltage lockout

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Start threshold | | 9.25 | 10 | 10.75 | V |
| Hysteresis | | 1.9 | 2 | 2.2 | V |
| Stop threshold | | 7.5 | | | V |

## electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 12 V, $I_{DRV}$ = 0 A (unless otherwise noted) (continued)

### output drivers

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Peak output current (see Note 5) | High-side sink | Duty cycle < 2%, $t_{pw}$ < 100 µs, $T_J$ = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 1.5 V (source) or 6 V (sink), See Note 3 | 2 | | | A |
| | High-side source | | 2 | | | |
| | Low-side sink | Duty Cycle < 2%, $t_{pw}$ < 100 µs, $T_J$ = 125°C, $V_{DRV}$ = 6.5 V, $V_{LOWDR}$ = 1.5 V (source) or 5 V (sink), See Note 3 | 2 | | | |
| | Low-side source | | 2 | | | |
| Output resistance (see Note 5) | High-side sink | $T_J$ = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 6 V (source) or 0.5 V (sink) | | | 3 | Ω |
| | High-side source | | | | 45 | |
| | Low-side sink | $T_J$ = 125°C, $V_{DRV}$ = 6.5 V, $V_{LOWDR}$ = 6 V (source) or 0.5 V (sink) | | | 5.7 | |
| | Low-side source | | | | 45 | |

NOTES: 3. This parameter is ensured by design and is not production tested.
5. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

### supply current

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | 11.4 | 12 | 13 | V |
| $V_{CC}$ | Quiescent current | $V_{INHIBIT}$ = 5 V, $V_{CC}$ > 10.75 V at startup, VID code ≠ 11111, $V_{BOOTLO}$ = 0 V | | 3 | 10 | mA |
| | | $V_{INHIBIT}$ = 5 V, $V_{CC}$ > 10.75 V at startup, $C_{HIGHDR}$ = 50 pF, $f_{SWX}$ = 200 kHz, VID code ≠ 11111, $V_{BOOTLO}$ = 0 V, $C_{LOWDR}$ = 50 pF, See Note 3 | | 5 | | |
| | High-side driver quiescent current | $V_{INHIBIT}$ = 0 V or VID code = 11111 or $V_{CC}$ < 9.25 V at startup, $V_{BOOT}$ = 13 V, $V_{BOOTLO}$ = 0 V | | | 80 | µA |
| | | $V_{INHIBIT}$ = 5 V, $V_{BOOT}$ = 13 V, $C_{HIGHDR}$ = 50 pF, VID code ≠ 11111, $V_{CC}$ > 10.75 V at startup, $V_{BOOTLO}$ = 0 V, $f_{SWX}$ = 200 kHz (see Note 3) | | 2 | | mA |

NOTE 3: This parameter is ensured by design and is not production tested.

**switching characteristics over recommended operating virtual-junction temperature range, $V_{CC}$ = 12 V, $I_{DRV}$ = 0 A (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation delay | VSENSE to HIGHDR or LOWDR (excluding dead-time) | 1.3 V ≤ $V_{VREF}$ ≤ 3.5 V, 10 mV overdrive (see Note 3) | | 150 | 250 | ns |
| | | 1.3 V ≤ $V_{VREF}$ ≤ 3.5 V, 20 mV overdrive | | | 200 | |
| | | 1.3 V ≤ $V_{VREF}$ ≤ 3.5 V, 30 mV overdrive | | | 190 | |
| | | 1.3 V ≤ $V_{VREF}$ ≤ 3.5 V, 40 mV overdrive | | | 180 | |
| | OCP comparator | See Note 3 | | 1 | | µs |
| | OVP comparator | | | 1 | | |
| | PWRGD comparator | | | 1 | | |
| | SLOWST comparator | Overdrive = 10 mV (see Note 3) | | 560 | 900 | ns |
| Rise time | HIGHDR output | $C_L$ = 50 pF, $V_{BOOTLO}$ = 0 V | | | 8 | ns |
| | | $C_L$ = 3 nF | | | 35 | |
| | LOWDR output | $C_L$ = 50 pF | | | 8 | |
| | | $C_L$ = 3 nF | | | 40 | |
| Fall time | HIGHDR output | $C_L$ = 50 pF, $V_{BOOTLO}$ = 0 V | | | TBD | ns |
| | | $C_L$ = 3 nF | | | 35 | |
| | LOWDR output | $C_L$ = 50 pF | | | TBD | |
| | | $C_L$ = 3 nF | | | 40 | |
| Deglitch time (Includes comparator propagation delay) | OCP | See Note 3 | 2 | | 5 | µs |
| | OVP | | 2 | | 5 | |
| Response time | High-side VDS sensing | $V_{HISENSE}$ = 12 V, $V_{IOUTLO}$ pulsed from 12 V to 11.9 V, 100 ns rise/fall times (see Note 3) | | | 2 | µs |
| | | $V_{HISENSE}$ = 4.5 V, $V_{IOUTLO}$ pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3) | | | 3 | |
| | | $V_{HISENSE}$ = 3 V, $V_{IOUTLO}$ pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3) | | | 3 | |
| Short-circuit protection rising-edge delay | SCP | LOSENSE = 0 V (see Note 3) | 300 | | 500 | ns |
| Turnon/turnoff delay | $V_{DS}$ sensing sample/hold switch | 3 V ≤ $V_{HISENSE}$ ≤ 11 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 3) | 30 | | 100 | ns |
| Crossover delay time | LOWDR to HIGHDRV, and LOHIB to LOWDR | See Note 3 | 30 | | 100 | ns |
| Prefilter pole frequency | Hysteretic comparator | See Note 3 | | 5 | | MHz |
| Propagation delay | LODRV | See Note 3 | | | 400 | ns |

NOTE 3: This parameter is ensured by design and is not production tested.

## TYPICAL CHARACTERISTICS

SLOWSTART TIME
vs
SLOWSTART CAPACITANCE

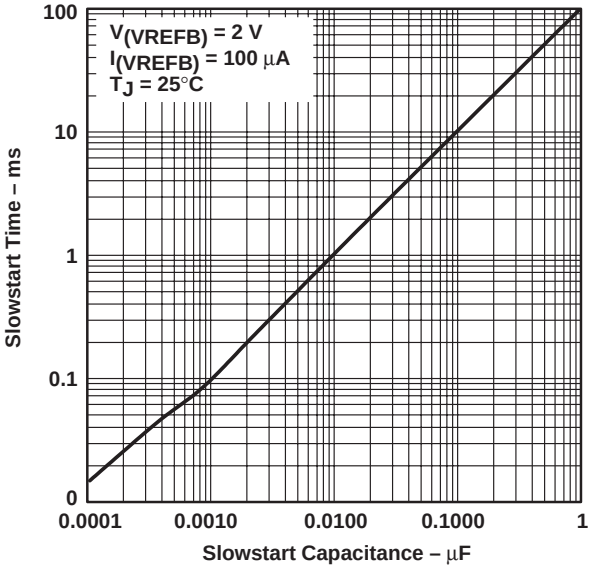



Figure 1

SLOWSTART TIME
vs
SUPPLY CURRENT (VREFB)

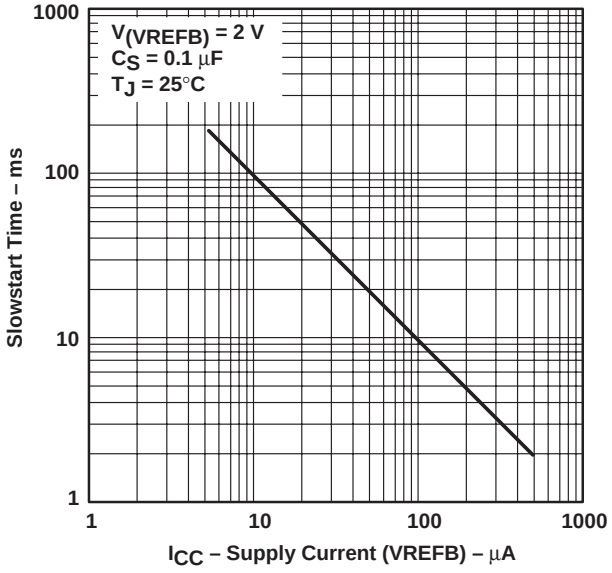



Figure 2

DRIVER
OUTPUT RISE TIME
vs
LOAD CAPACITANCE

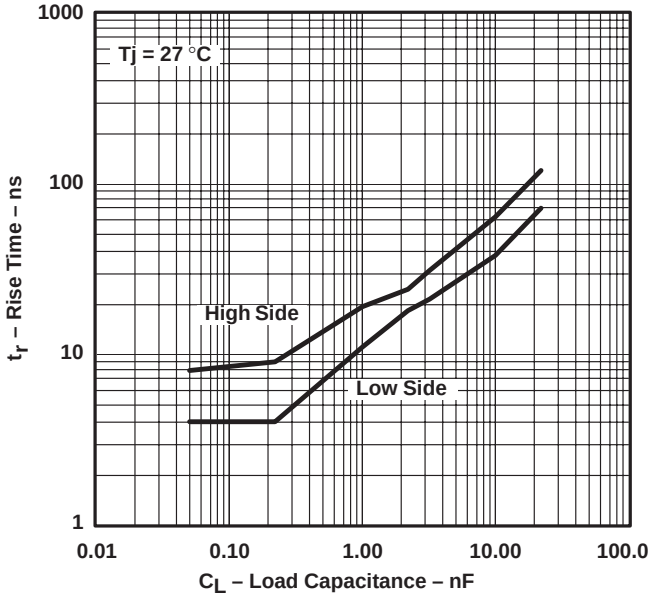



Figure 3

DRIVER
OUTPUT FALL TIME
vs
LOAD CAPACITANCE

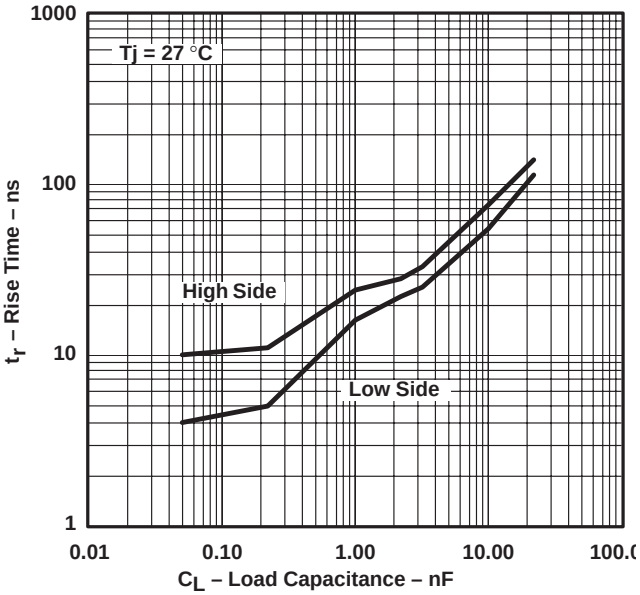



Figure 4

## TYPICAL CHARACTERISTICS

OVP THRESHOLD
vs
JUNCTION TEMPERATURE

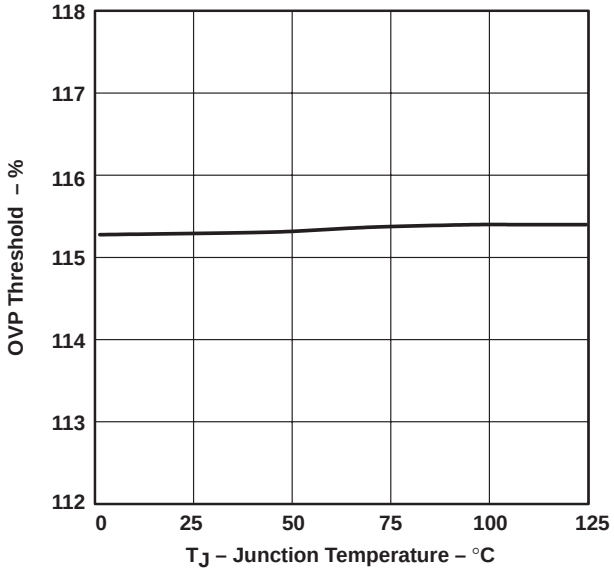



Figure 5

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

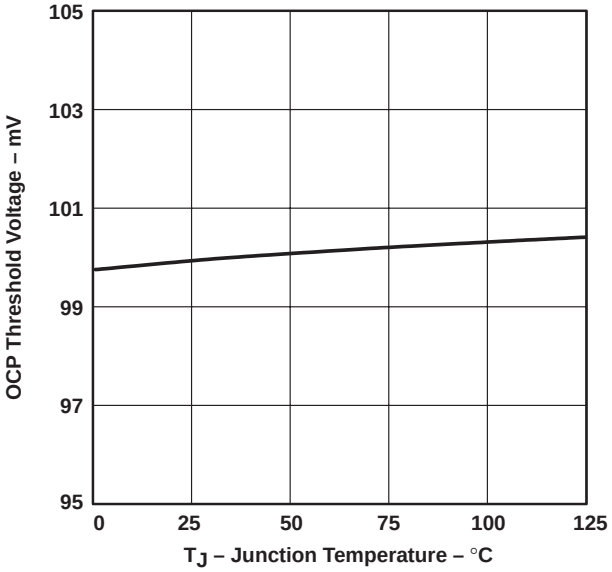



Figure 6

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

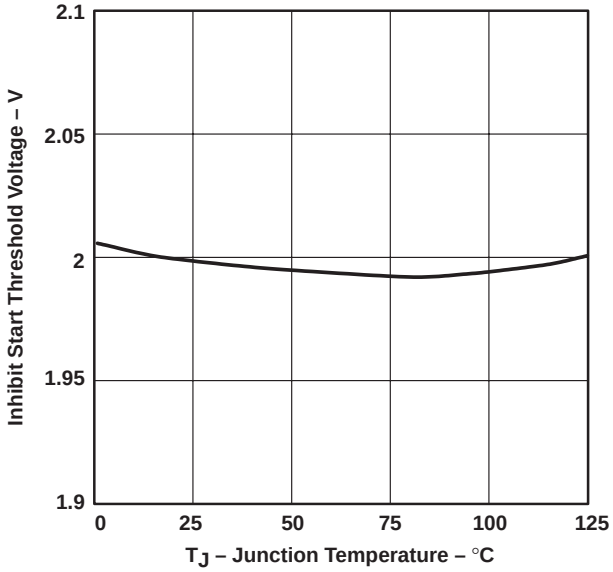



Figure 7

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

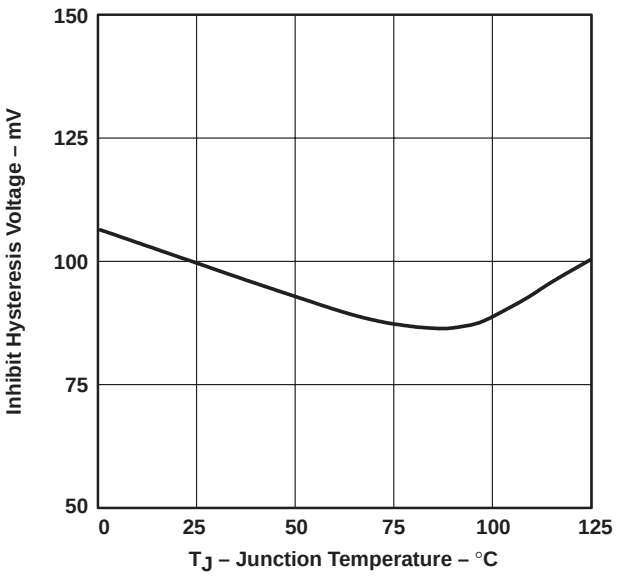



Figure 8

## TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

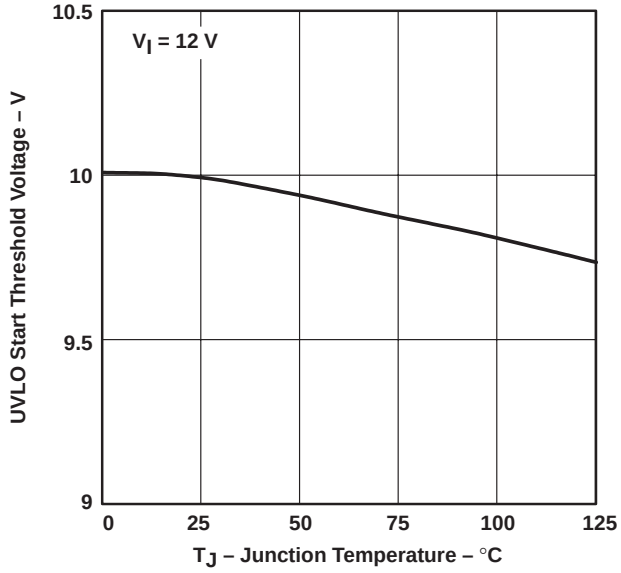



Figure 9

UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

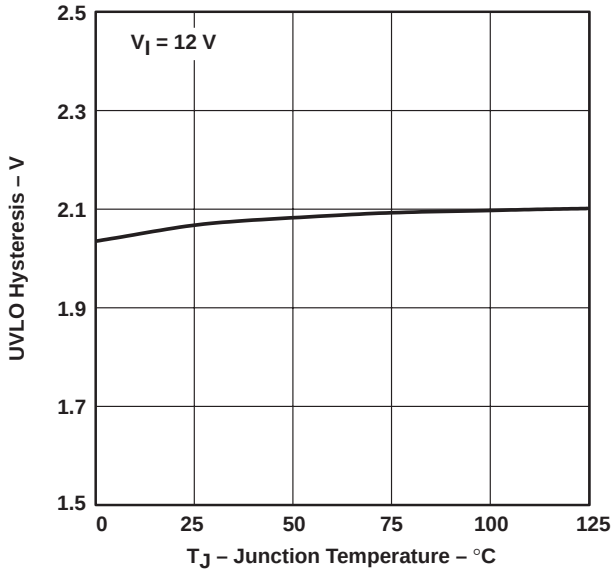



Figure 10

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

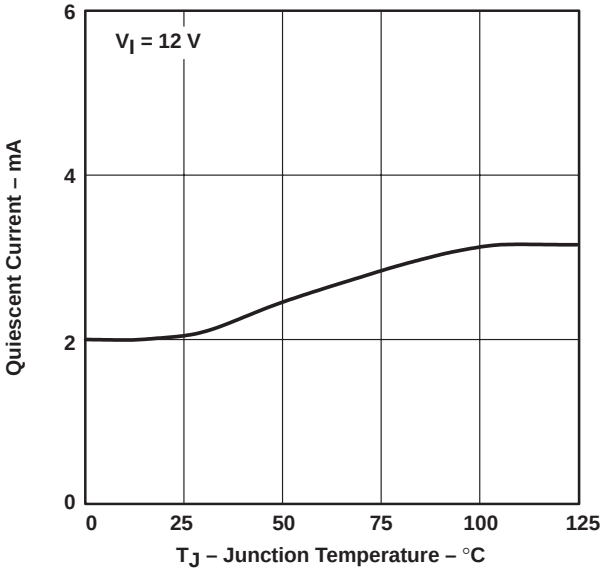



Figure 11

POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

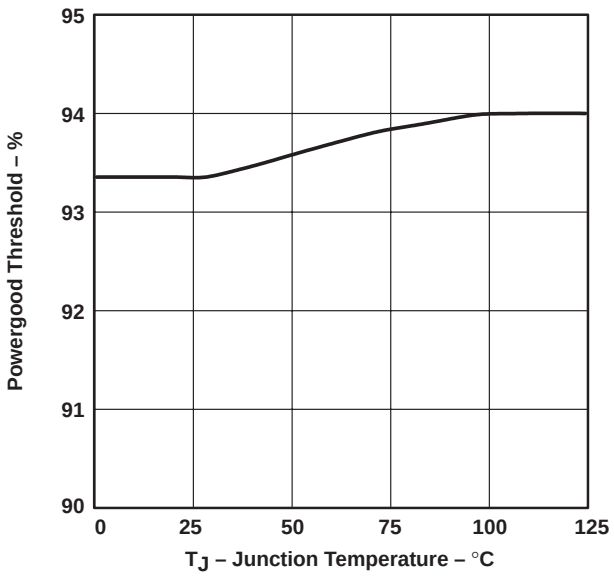



Figure 12

## TYPICAL CHARACTERISTICS

**SLOWSTART CHARGE CURRENT vs JUNCTION TEMPERATURE**

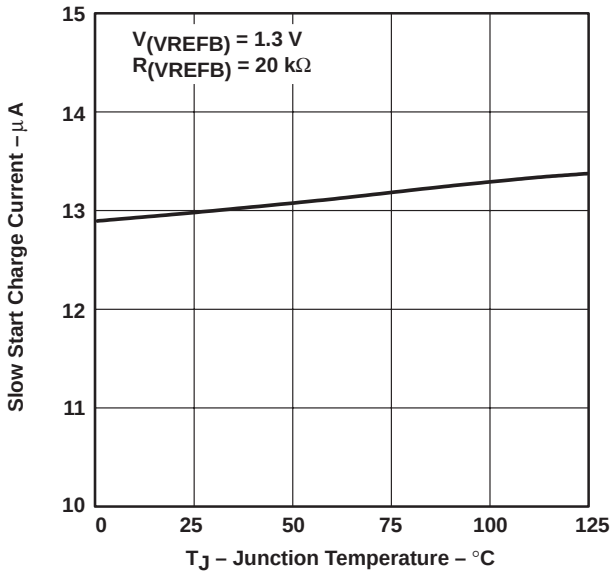



**Figure 13**

**DRIVER REGULATOR VOLTAGE vs JUNCTION TEMPERATURE**

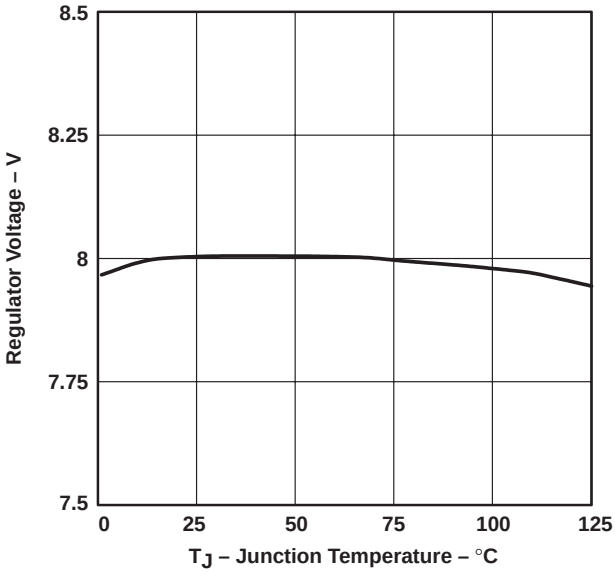



**Figure 14**

**DRIVER HIGH-SIDE OUTPUT RESISTANCE vs JUNCTION TEMPERATURE**

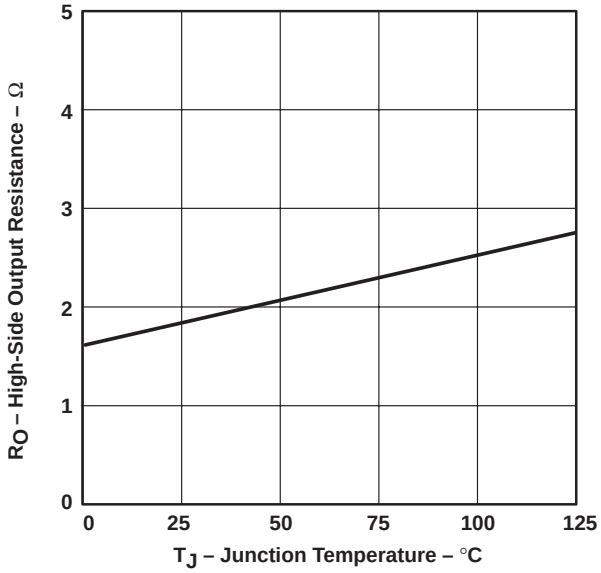



**Figure 15**

**DRIVER LOW-SIDE OUTPUT RESISTANCE vs JUNCTION TEMPERATURE**

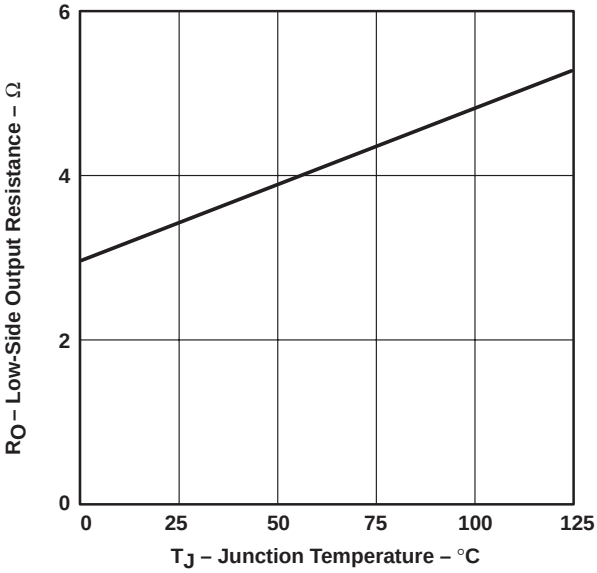



**Figure 16**

## TYPICAL CHARACTERISTICS

**SENSING SAMPLE/HOLD RESISTANCE
vs
JUNCTION TEMPERATURE**

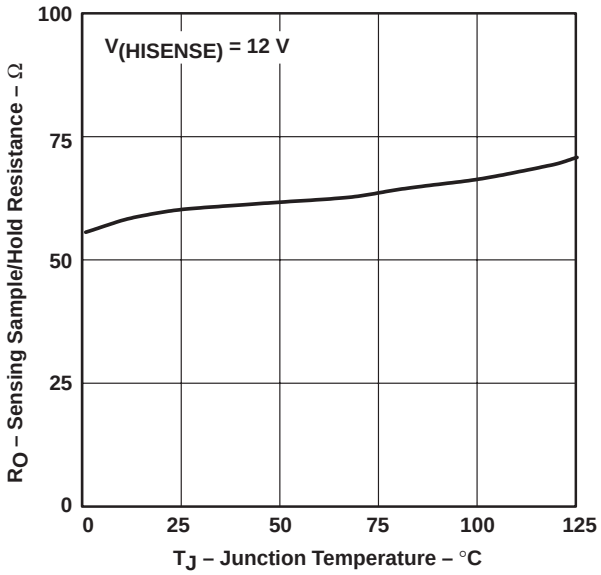
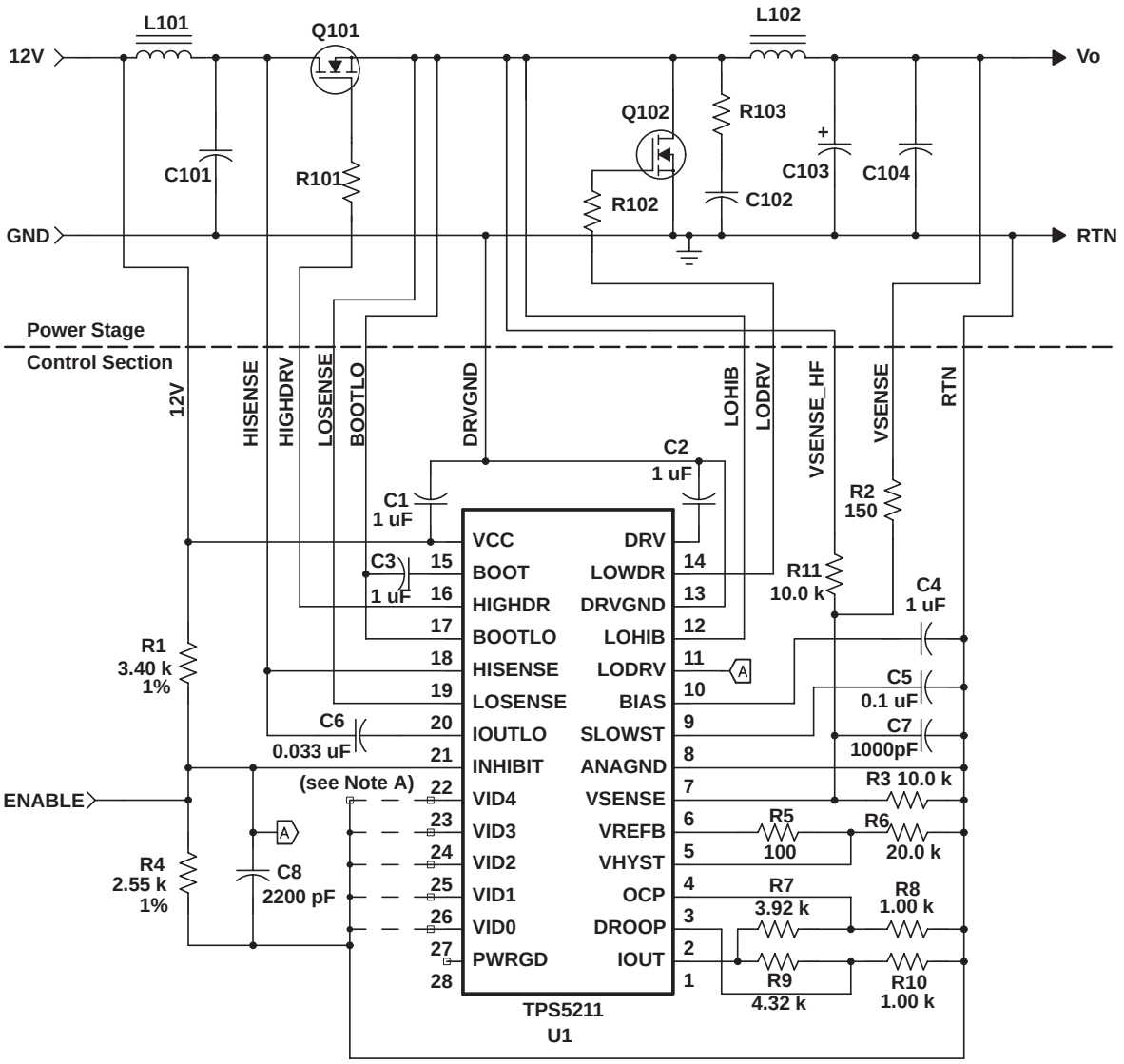



**Figure 17**

## APPLICATION INFORMATION

The following figure is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values. Table 2 shows the values of the power stage components for various output-current options.




NOTE A: VID0 – VID4 User – selected to set output voltage.

**Figure 18. Standard Application Schematic**

## APPLICATION INFORMATION

### Table 2. Power Stage Components

| Reference Designation | Function | 12-V–Input Power Stage Components | | | |
|---|---|---|---|---|---|
| | | 4–A Out | 8–A Out | 12–A Out | 20–A Out |
| C101 | Input capacitor | muRata, GRM235Y106Z016A, 2 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 4 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 6 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 10 x 10–uF, 16–V, Y5V |
| C102 | Snubber capacitor | muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R | muRata, GRM39X7R102K050A, 1000–pF, 50–V, X7R | muRata, GRM39X7R102K050A, 2 x 1000–pF, 50–V, X7R | muRata, GRM39X7R102K050A, 3 x 1000–pF, 50–V, X7R |
| C103 | Output bulk capacitor | Sanyo, 4TPC150M, 150–uF, 4–V, 20% | Sanyo, 4TPC150M, 2 x 150–uF, 4–V, 20% | Sanyo, 4TPC150M, 3 x 150–uF, 4–V, 20% | Sanyo, 4TPC150M, 4 x 150–uF, 4–V, 20% |
| C104 | Output hi–freq bypass capacitor | muRata, GRM235Y106Z016A, 2 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 4 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 6 x 10–uF, 16–V, Y5V | muRata, GRM235Y106Z016A, 8 x 10–uF, 16–V, Y5V |
| L101 | Input filter inductor | CoilCraft, DO1607C–152, 1.5–uH, 2.1–A | CoilCraft, DO1813HC–122, 1.2–uH, 4.4–A | CoilCraft, DO1813HC–122, 1.2–uH, 4.4–A | CoilCraft, DO3316P–152HC, 1.5–uH, 9.0–A |
| L102 | Output filter inductor | CoilCraft, DO1813HCP–561, 0.56–uH, 6–A | CoilCraft, DO3316P–681HC, 0.68–uH, 12–A | Vishay–Dale, IHLP–5050CE–XX, 0.82–uH, 16–A, New product | Vishay–Dale, IHLP–5050CE–XX, 0.5–uH, 25–A, New product |
| R101 | High–side gate resistor | 10.0–Ohm, 1/16–W, 5% | 10.0–Ohm, 1/16–W, 5% | 2 x 10.0–Ohm, 1/16–W, 5% | 2 x 10.0–Ohm, 1/16–W, 5% |
| R102 | Lo–side gate resistor | 3.3–Ohm, 1/16–W, 5% | 3.3–Ohm, 1/16–W, 5% | 2 x 3.3–Ohm, 1/16–W, 5% | 3 x 3.3–Ohm, 1/16–W, 5% |
| R103 | Snubber resistor | 2.7–Ohm, 1/10–W, 5% | 2.7–Ohm, 1/10–W, 5% | 2 x 2.7–Ohm, 1/10–W, 5% | 3 x 2.7–Ohm, 1/10–W, 5% |
| Q101 | Power switch | IR, IRF7811, NMOS, 11–mOhm | IR, IRF7811, NMOS, 11–mOhm | IR, 2 x IRF7811, NMOS, 11–mOhm | IR, 2 x IRF7811, NMOS, 11–mOhm |
| Q102 | Synchronous switch | IR, IRF7811, NMOS, 11–mOhm | IR, IRF7811, NMOS, 11–mOhm | IR, 2 x IRF7811, NMOS, 11–mOhm | IR, 2 x IRF7811, NMOS, 11–mOhm |
| Nominal frequency† | 700 KHz | | | | |
| Hysteresis window | 20 mV | | | | |

† Nominal frequency measured with Vo set to 2 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today's microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.

## APPLICATION INFORMATION

### frequency calculation

The simplified equation shown below can be used for a preliminary frequency calculation:

$$f_S \cong \frac{V_{REF} \times (V_I - V_{REF})}{V_I \times R11 \times C7 \times \text{Hysteresis Window}} \times 0.85 \quad (1)$$

High frequency operations require special attention not to exceed maxium current through the controller (120mA), and the maximum total power dissipation.

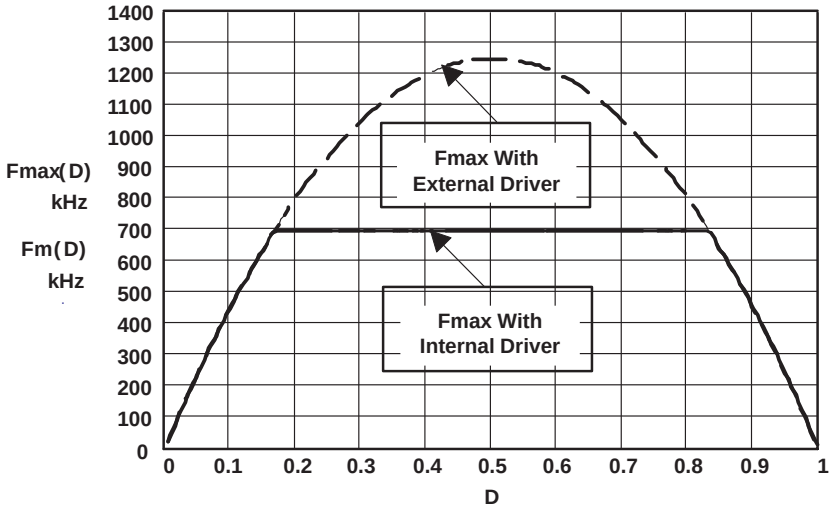



**Figure 19**

Another restriction relates to the maximum rms current through the output of the highside driver, (110mA.) The maximum allowable operating frequency can be defined by the following equation:

$$Fmax = \frac{(110mA)^2 \times 60ohm)}{Qg \times (V_I + Vdrv)} \quad (2)$$

Where Qg = Total gate charge of the upper FETs in the hysteretic converter (in nanocoulombs)
Vdrv = 8 V and is the drive regulator voltage of the TPS5211 controller
$V_I$ = Input voltage
Fmax = Maximum switching frequency in kHz

Figure 19 and equation (2) should be used to determine the maximum operating frequency of a converter. The operating frequency should not exceed the lower of the two values determined by Figure 19 and equation (2).

## APPLICATION INFORMATION

### Control Section

Below are the equations needed to select the various components within the control section.

### output voltage selection

The most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 3.5 V can be easily set by shorting the correct VID inputs to ground. Values above the maximum reference voltage (3.5 V) can be set by setting the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

R3 << than $V_{REF}/I_{BIAS(VSENSE)}$; a recommended value is 10 kΩ

Then, calculate R2 using:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right) \qquad \text{or} \qquad R2 = \frac{R3 \times \left(V_O - V_{REF}\right)}{V_{REF}}$$

These equations are accurate if R2<<R11. If this condition is not fullfilled, the following equation must be used:

$$V_O = V_{REF}\left(1 + \frac{R2 \text{ x } R11}{R3 \text{ x } (R2 + R11)}\right)$$

Another soultion is to use 0.1-µF DC decoupling capacitor in series with R11. In such a case, R11 does not influence the output voltage value.

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range and/or to adjust for load-current active droop compensation. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150 \text{ ns}}{(R2 \parallel R3)}$$

### slowstart timing

Slowstart reduces the startup stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R6) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R6:

R6 should be between 7 kΩ and 300 kΩ, a recommended value is 20 kΩ.

Set the slowstart timing using the formula:

$$C5 = \frac{t_{SS}}{\left(5 \times R_{VREFB}\right)} \cong \frac{t_{SS}}{(5 \times R6)}$$

Where C5 = Slowstart capacitance in µF
$t_{SS}$ = Slowstart timing in µs
$R_{VREFB}$ = Resistance from VREFB to GND in ohms (≈ R6)

## APPLICATION INFORMATION

### hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the VSENSE pin which the input comparator uses for sensing. Once selected, the TPS5211 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. Since the output current from VREFB should be less than 500 μA, the total divider resistance (R5 + R6) should be greater than 7 KΩ. The hysteresis voltage should be no greater than 60 mV so R6 will dominate the divider.

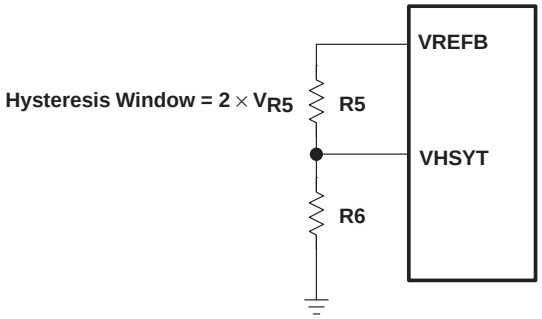



**Figure 20. Hysteresis Divider Circuit**

The upper divider resistor, R5, is calculated using:

$$R5 = \frac{Hysteresis\ Window}{(2 \times VREFB - Hysteresis\ Window)} \times R6 \cong \frac{V_{HYST}\ (\%)}{(2 \times 100)} \times R6$$

Where Hysteresis Window = The desired peak-to-peak hysteresis voltage
VREFB = Selected reference voltage
$V_{HYST}$ (%) = [(Hysteresis Window)/VREFB] * 100 < $V_{O(Ripple)(P–P)}$ (%)

### current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing elements. Select R8:

$$R8 << \frac{V_{OCP}}{I_{Bias(OCP)}} \leq \frac{0.1V}{(100 \times 100\,nA)} \leq 10\ k\Omega$$ (A recommended value is 1 kΩ)

The IOUT signal is used to drive the current limit and droop-circuit dividers. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Trip)}$$

Where NumFETS = Number of upper FETS in parallel
TF = $R_{DS(ON)}$ temperature correction factor
$I_{O(Trip)}$ = Desired output current trip level (A)

## APPLICATION INFORMATION

Calculate R7 using:

$$R7 = \left(\frac{V_{IOUT(Trip)}}{0.1\ V} - 1\right) \times R8$$

Note that since $R_{DS(ON)}$ of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than 1.5 x $I_O$) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

### droop compensation

Active voltage droop positioning is used to reduce the output voltage range during load transients by increasing the output voltage setpoint toward the upper tolerance limit during light loads and decreasing the voltage setpoint toward the lower tolerance limit during heavy loads. This allows the output voltage to swing a greater amount and still remain within the tolerance window. The maximum droop voltage is set with R9 and R10. Select R10:

$$R10 << \frac{V_{DROOP(Min)}}{I_{Bias(DROOP,Max)}} \leq \frac{0.01V}{(100 \times 100\ nA)} \leq 1\ k\Omega$$ (Again, a value of 1 kΩ is recommended)

The voltage at IOUT during normal operation (0 to 100% load) will vary from 0 V up to:

$$V_{IOUT(Max)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETs} \times I_{O(Max)}$$

Where $I_{O(Max)}$ = Maximum output load current (A).

### droop compensation (continued)

Then, calculate R9:

$$R9 = \left(\frac{V_{IOUT(Max)}}{V_{DROOP}} - 1\right) \times R10$$

Where $V_{DROOP}$ = Desired droop voltage

At full load, the output voltage will be:

$$V_O = V_{REF} \times \left(1 + \frac{R2}{R3}\right) - V_{DROOP}$$

## APPLICATION INFORMATION

### using the TPS5211 when both 12 V and 5 V are available

When both 12 V and 5 V are available, several components can be removed from the basic schematic shown in Figure 18. R1, R4, and C9 are no longer required if 5 V is brought in directly to INHIBIT and LODRV. However, if undervoltage lockout for the 5-V input is desired, R1 and R4 can be used to set the startup setpoint. The INHIBIT pin trip level is 2.1 V. Select R4:

$$R4 << \frac{V_{INH}}{I_{INH(Max)}} \leq \frac{2.1V}{(100 \times 100\,nA)} \leq 210\,k\Omega$$

Then, set the 5-V UVLO trip level with R1:

$$R1 = \frac{(5\,V_{Trip} - 2V)}{2V} \times R4$$

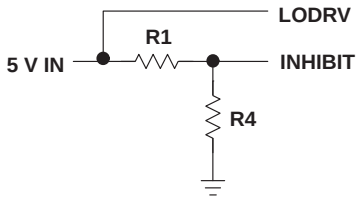
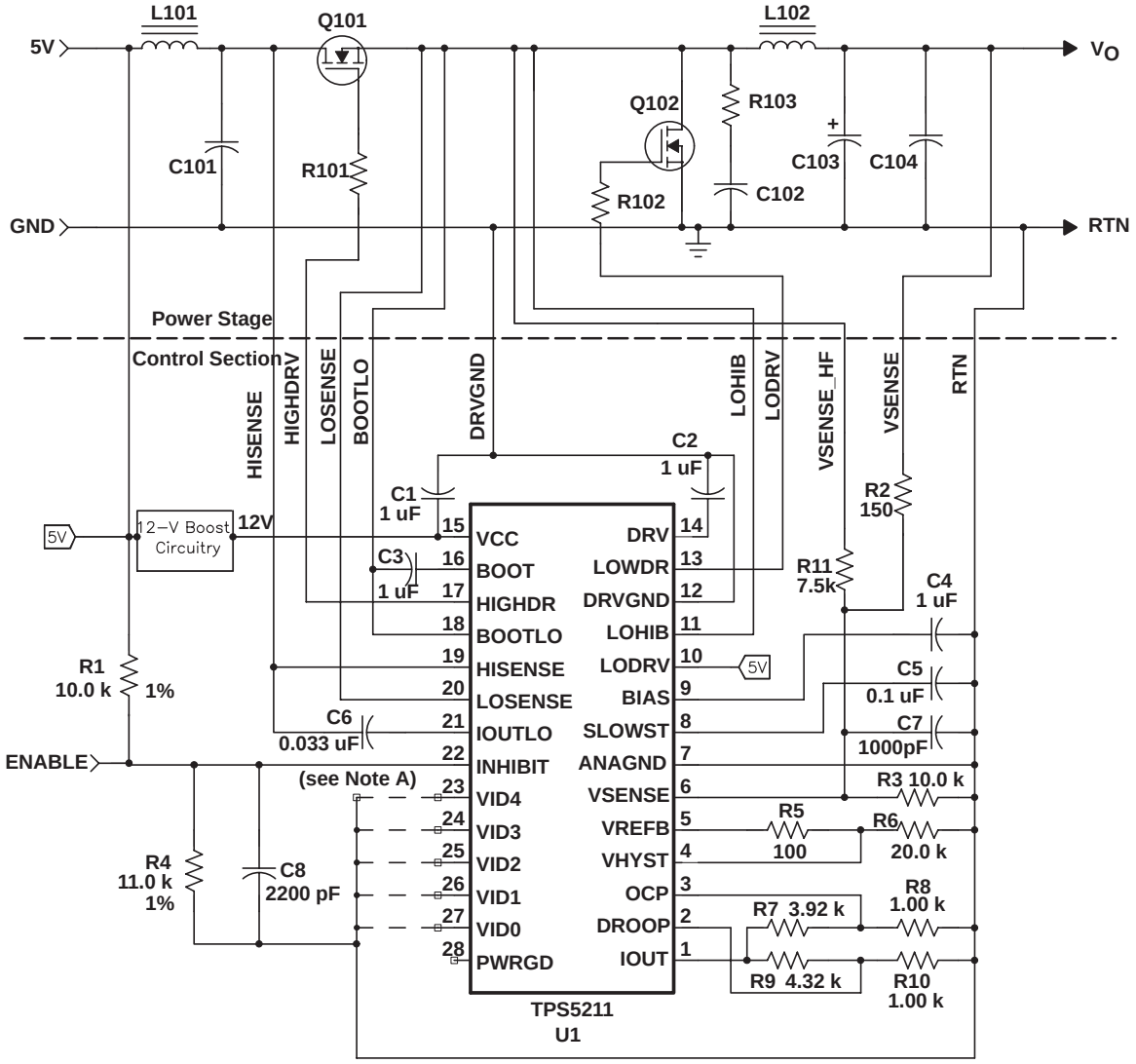



**Figure 21. 5-V Input With UVLO**

## APPLICATION INFORMATION

### using the TPS5211 when only 5 V is available

The TPS5211 controller requires 12 V for internal control of the device. If an external source for 12 V is not available, a small onboard source must be included in the design. A simple boost circuitry is described in TIs application report AN452 *Providing a DSP Power Solution from +5 V or +3.3 V only Systems.* Total 12-V current depends on switching frequency and power FETs gate charge characteristics. For reliable operation, this current should not exceed 120 mA. The power stage is not voltage dependent, but component values must be selected for 5-V inputs. The frequency of operation is dependent upon the power stage input voltage. A typical 5-V only application circuit is shown in Figure 22.




NOTE A: VID0 – VID4 User – selected to set output voltage.

**Figure 22. Typical 5-V-Only Application Circuit**

## APPLICATION INFORMATION

### controller operation

Operation of the TPS5211 controller differs from a regular hysteretic controller. The additional ramp signal through the input of the hysteretic comparator is formed by R11 and C7. The two signals are summed through the inputs of the comparator. The two signals are the ramp signal from R11 - C7 circuitry and the signal from the output converter. By proper selection of R11 and C7, one can get the amplitude of an additional ramp signal which is greater than the output ripple of the converter. As a result, the switching frequency is greater while the output ripple becomes lower. The additional ramp signal and output ripple waveforms are shown in Figure 23. The switching frequency now depends on R11 and C7 values and does not depend on the output filter characteristics including ESR, ESL, and C of the output capacitor (see frequency calculation section).

The dc feedback signal from the output of the converter through resistor R2 controls the dc level of the output voltage. Because the switching frequency of TPS5211 is high and it does not depend on output capacitor characteristics, low cost cermic or film capacitors can be used in a dc to dc converter while having the same load current transient response characteristics.

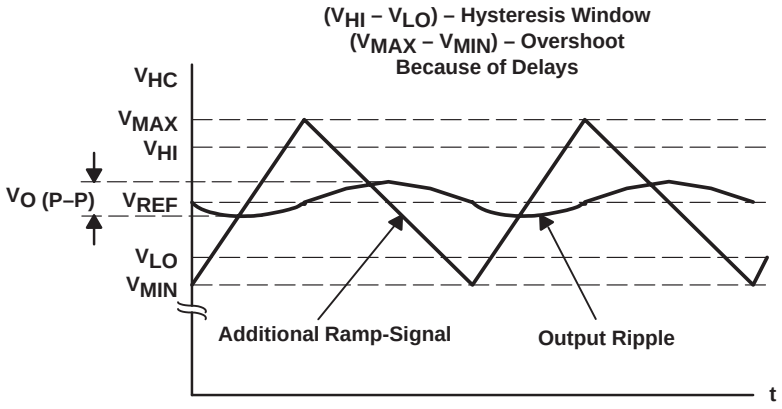



**Figure 23. The Additional Ramp-Signal and Output Voltage Ripple Waveforms**

## APPLICATION INFORMATION

### application examples

Below are waveforms and test results measured on the EVM for a 12-V input and a 2-V, 20-A output application. The output voltage ripple and power switches midpoints are shown in Figure 24. The converter operates at 450 kHz. The peak to peak output ripple is 9.6 mV, while the hysteresis window is set at 20 mV. Therefore, the output ripple for converter with TPS5211 is much lower than the hysteresis window.

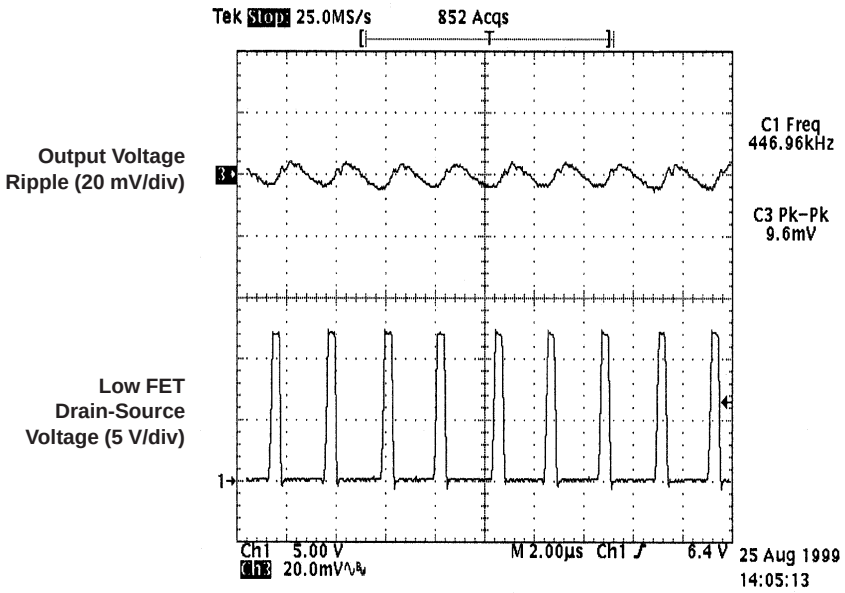



**Figure 24. The Output Voltage Ripple ans Low FET Drain-Source Voltage Waveforms**

## APPLICATION INFORMATION

The load current transient response waveforms are shown in Figure 25 to illustrate the excellent load current transient response characteristics of TPS5211.

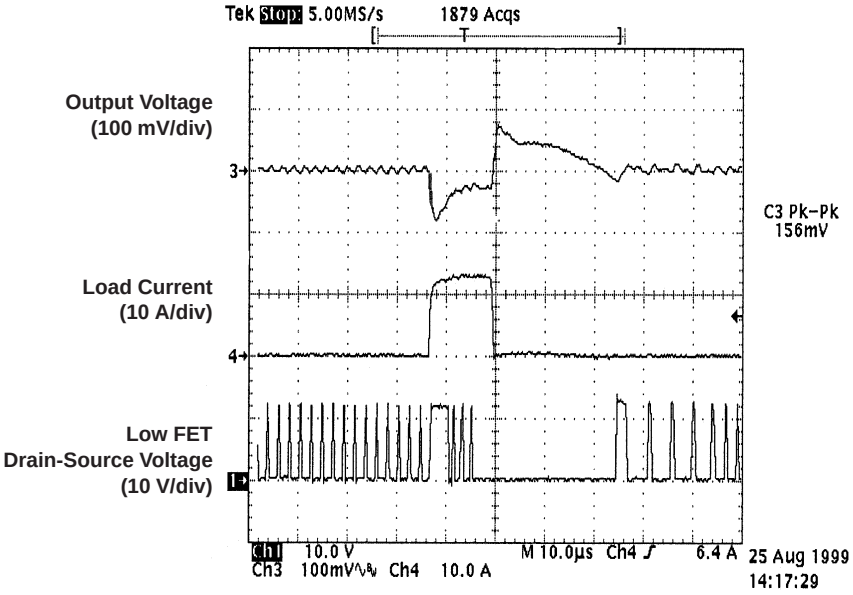



**Figure 25**

The output voltage transient response of the converter with TPS5211 controller. The load current has 14 A step with slew rate of 30 A/µS.

## APPLICATION INFORMATION

### Comparison of TPS5210 and TPS5211 controller applications

The TPS5210 and TPS5211 hysteretic controllers have excellent load current transient response characteristics, which is one of the most important advantages of hysteretic mode. There are specific application areas where one of the hysteretic controllers is preferable over the other. The table below gives a comparative view on application areas for the TPS5210 and TPS5211 controllers

| comparison of TPS5210 and TPS5211 applications | | |
|---|---|---|
| Controller | TPS5210 | TPS5211 |
| Switching frequency, kHz | 100 – 400 | 400 – 700 |
| Frequency variation | Depends on outout filter characteristics | Independent of output filter and easy to evaluate |
| Output current, A | up to 40 | up to 18 – 20 (can be increased in multi-phase configuration) |
| Efficiency, % (depends on frequency, output current, Vin, Vout, components, etc.) | 85 – 95 | 75 – 85 |
| Input and output filter | Requires bulk electrolytic capacitors especially if Iout > 12A and larger inductor | Surface-mount ceramic and POSCAP type capacitors and 40% – 65% smaller inductors. |
| Component Cost | 20% – 40% lower for TPS5211 | |
| System cost including reliability, power losses, cooling, etc. | Can be estimated only during design for a given specific application. | |
| Layout and design | Special attention to the noise sensitive places such as the hysteresis comparator and the sample hold circuitry. | Special attention not to exceed frequency and Icc limits. The high frequency dc – dc converter design rules should be used. |
| Compatibility with the whole system | For high current applications, it is difficult to meet high density minimum size requirements. | A dc – dc converter can be placed close to the microprocessor or DSP to decrease the number of decoupling capacitors. |

## APPLICATION INFORMATION

### layout guidelines

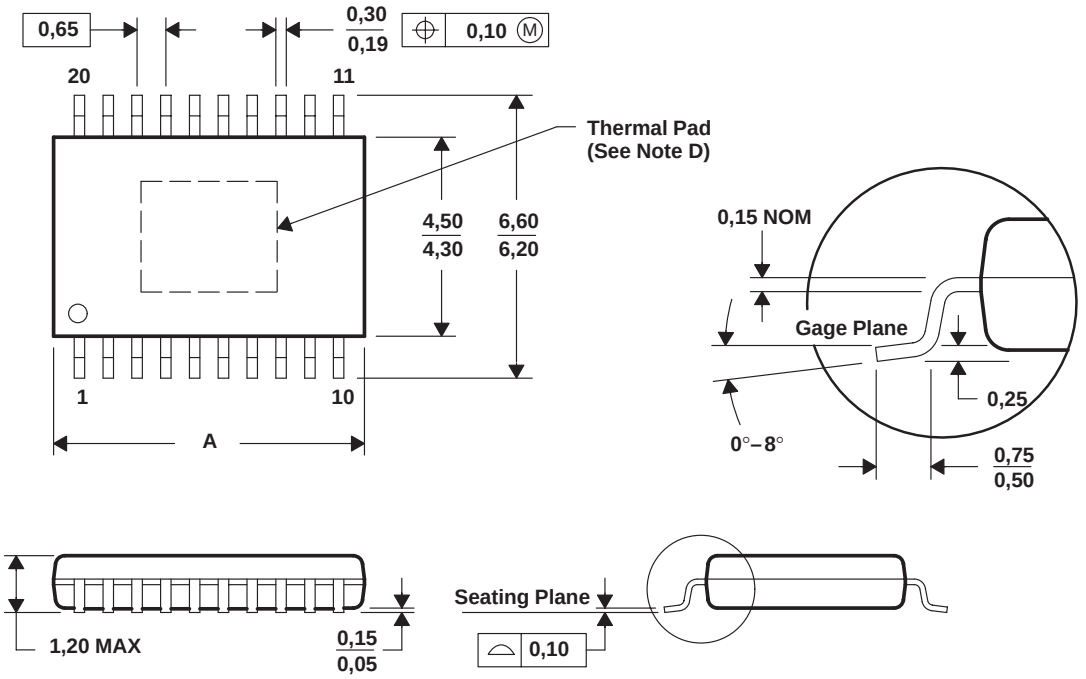
Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section, and, finally, to placing the low-level components. Below are several specific points to consider *before* layout of a TPS5211 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on $V_O$, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs, should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS5210 and be connected to DRVGND.
5. The bypass capacitor for $V_{CC}$ should be placed close to the TPS5210 and be connected to DRVGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETS since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS5210.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across $V_I$ should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on $V_O$.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

## MECHANICAL DATA

**PWP (R-PDSO-G**)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

**20-PIN SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|
| A MAX | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4073225/E 03/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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