



# High Speed Power Driver

## FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

## DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both  $V_s$  and  $V_c$  can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

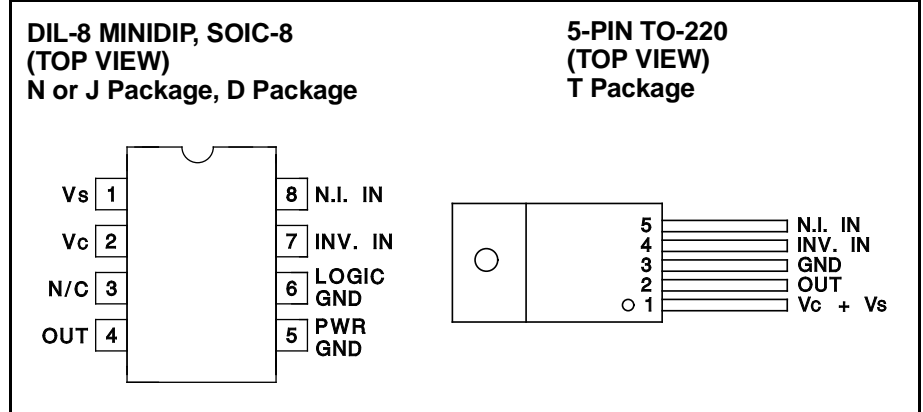
The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

## TRUTH TABLE

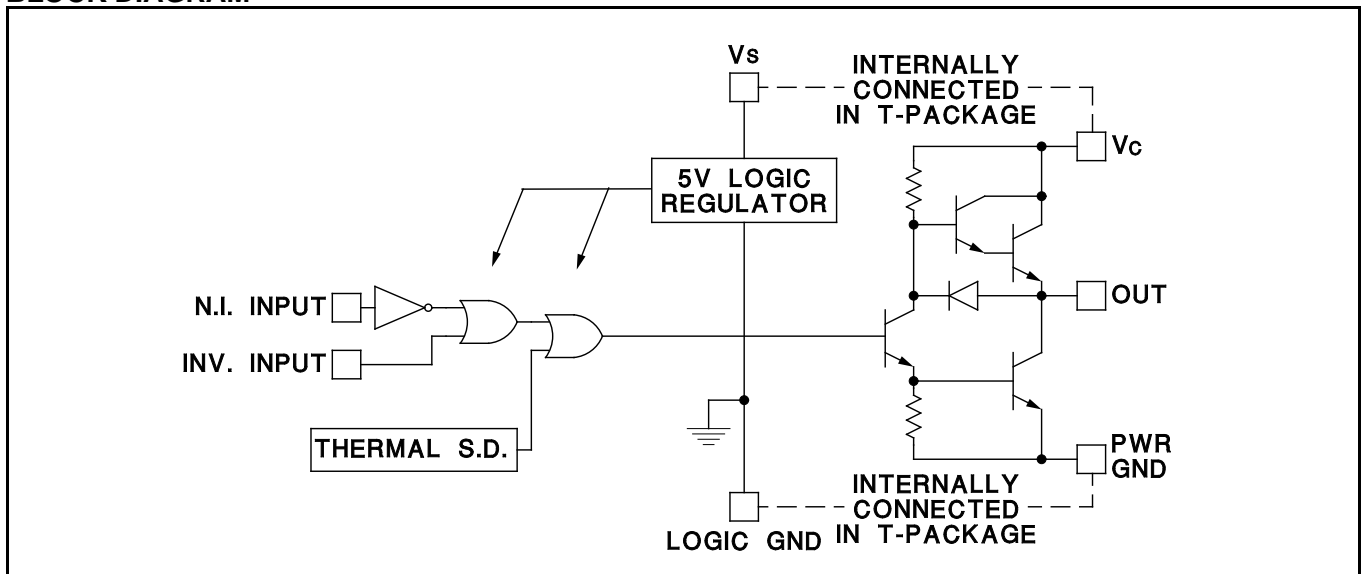
INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$\overline{OUT} = \overline{INV}$  and  $\overline{N.I.}$   
 $\overline{OUT} = INV$  or  $\overline{N.I.}$

## CONNECTION DIAGRAMS



## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

	<b>N-Pkg</b>	<b>J-Pkg</b>	<b>T-Pkg</b>
Supply Voltage, $V_{IN}$ .....	40V	40V	40V
Collector Supply Voltage, $V_C$ .....	40V	40V	40V
Output Current (Source or Sink)			
Steady-State .....	$\pm 500\text{mA}$	$\pm 500\text{mA}$	$\pm 1.0\text{A}$
Peak Transient .....	$\pm 1.5\text{A}$	$\pm 1.0\text{A}$	$\pm 2.0\text{A}$
Capacitive Discharge Energy .....	20 $\mu\text{J}$	15 $\mu\text{J}$	50 $\mu\text{J}$
Digital Inputs (See Note) .....	5.5V	5.5V	5.5V
Power Dissipation at $T_A = 25^\circ\text{C}$ (See Note) .....	1W	1W	3W
Power Dissipation at $T_A$ (Leads/Case) = $25^\circ\text{C}$ (See Note) .....	3W	2W	25W
Operating Temperature Range .....	$0^\circ\text{C}$ to $+70^\circ\text{C}$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	$0^\circ\text{C}$ to $+70^\circ\text{C}$
Storage Temperature Range .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 seconds) .....	$300^\circ\text{C}$	$300^\circ\text{C}$	$300^\circ\text{C}$

*Note: All currents are positive into, negative out of the specified terminal.*

*Digital Drive can exceed 5.5V if input current is limited to 10mA*

*Consult Packaging Section of Databook for thermal limitations and considerations of package.*

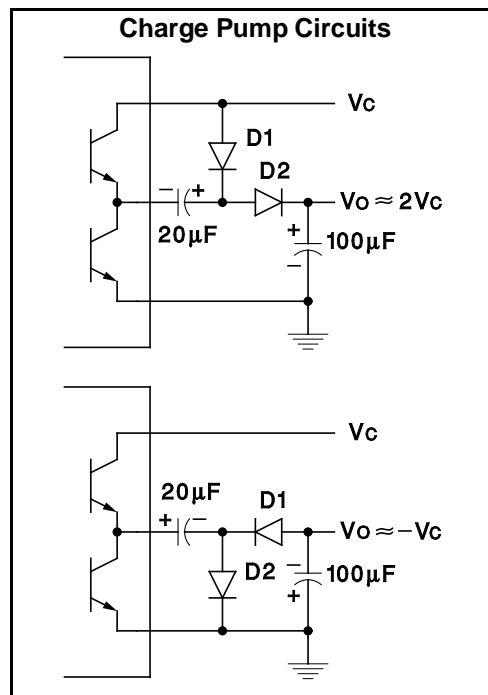
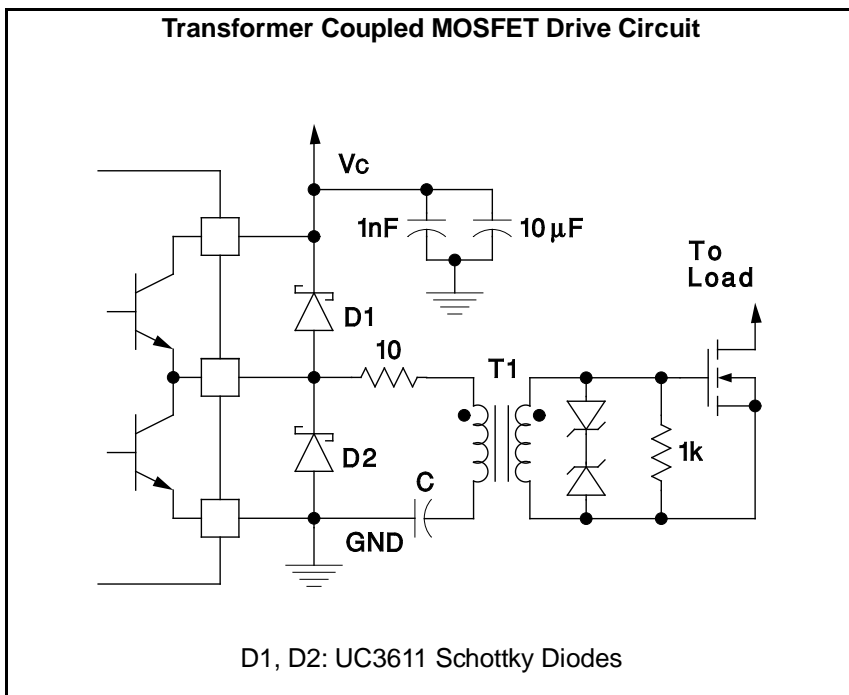
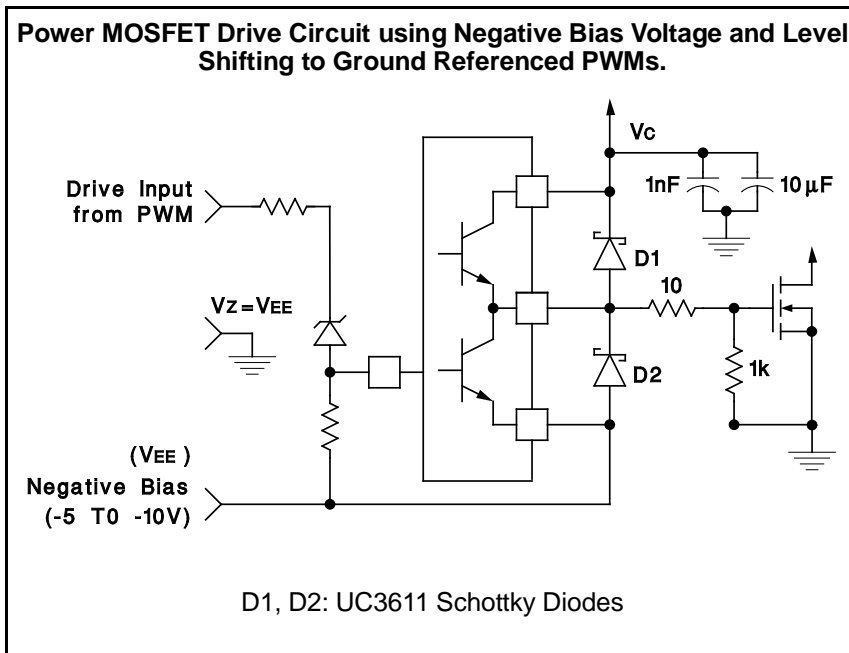
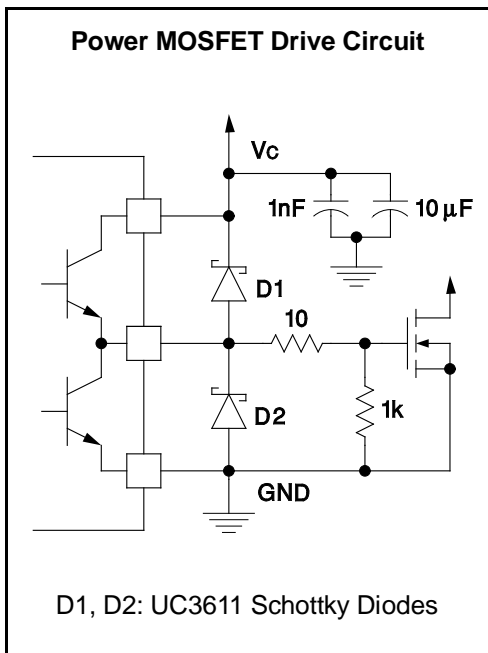
**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1705,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2705, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3705;  $V_S = V_C = 20\text{V}$ ,  $T_A = T_J$ .

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_S$ Supply Current	$V_S = 40\text{V}$ , (Outputs High, T Pkg)		6	8	mA
	$V_S = 40\text{V}$ , (Outputs Low, T Pkg)		8	12	mA
$V_C$ Supply Current (N, J Only)	$V_C = 40\text{V}$ , Outputs Low		2	4	mA
$V_C$ Leakage Current (N, J Only)	$V_S = 0$ , $V_C = 30\text{V}$		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	$V_I = 0$		-0.6	-1.0	mA
Input Leakage	$V_I = 5\text{V}$		0.5	0.1	mA
Output High Sat., $V_C - V_O$	$I_O = -50\text{mA}$			2.0	V
	$I_O = -500\text{mA}$			2.5	V
Output Low Sat., $V_O$	$I_O = 50\text{mA}$			0.4	V
	$I_O = 500\text{mA}$			2.5	V
Thermal Shutdown			155		$^\circ\text{C}$

**TYPICAL SWITCHING CHARACTERISTICS:**  $V_S = V_C = 20\text{V}$ ,  $T_A = 25^\circ\text{C}$ . Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT $C_L =$			UNIT
		open	1.0	2.2	
From Inv. Input to Output:					nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
$V_C$ Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns

APPLICATIONS



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