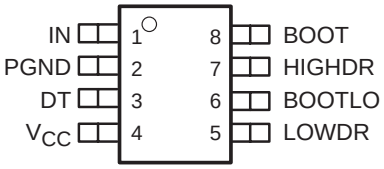
- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Active Deadtime Control**
- **50-ns Max Rise/Fall Times and 100-ns Max Propagation Delay — 3-nF Load**
- **Ideal for High-Current Single or Mutiphase Applications**
- **2.4-A Typ Peak Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **Internal Schottky Bootstrap Diode**
- **Low Supply Current . . . 3–mA Typ**
- **–40°C to 125°C Junction-Temperature Operating Range**

**D PACKAGE**
**(TOP VIEW)**




## description

The TPS2832 and TPS2833 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using a switching controller that does not include suitable MOSFET drivers on the chip. The drivers are designed to deliver 2.4-A peak currents into large capacitive loads. Higher currents can be controlled by using multiple drivers in a multiphase configuration. The high-side driver can be configured as a ground-reference driver or as a floating bootstrap driver. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions and provides high efficiency for the buck regulator.

The TPS2832 has a noninverting input. The TPS2833 has an inverting input. The TPS2832/33 drivers, available in 8-terminal SOIC packages, operate over a junction temperature range of –40°C to 125°C.

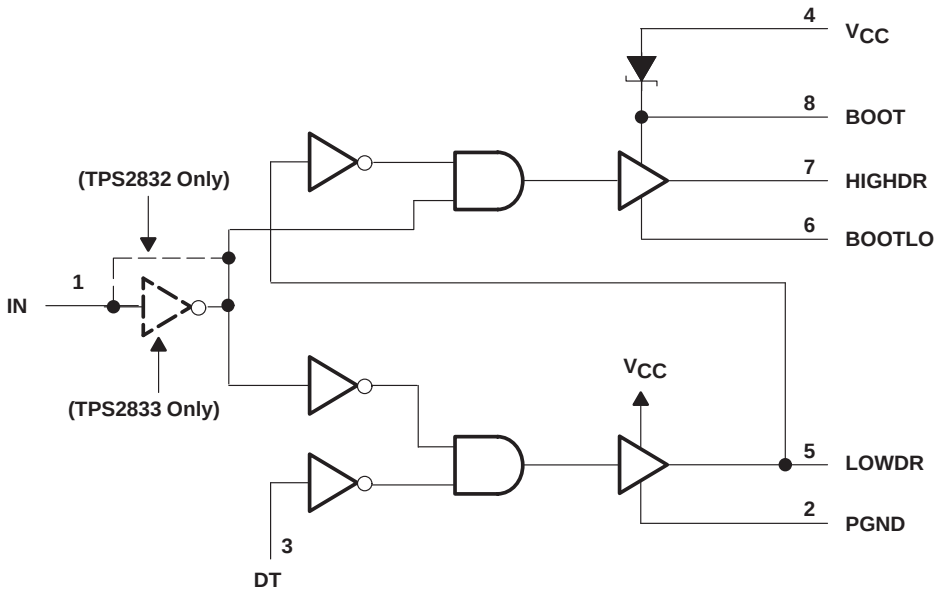
**AVAILABLE OPTIONS**

| $T_J$ | PACKAGED DEVICES |
|---|---|
| | SOIC (D) |
| –40°C to 125°C | TPS2832D<br>TPS2833D |

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2830DR)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## functional block diagram




## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BOOT | 8 | I | Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO terminals to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μF and 1 μF. A 1-MΩ resistor should be connected across the bootstrap capacitor to provide a discharge path when the driver has been powered down. |
| BOOTLO | 6 | O | This terminal connects to the junction of the high-side and low-side MOSFETs. |
| DT | 3 | I | Deadtime control terminal. Connect DT to the junction of the high-side and low-side MOSFETs |
| HIGHDR | 7 | O | Output drive for the high-side power MOSFET |
| IN | 1 | I | Input signal to the MOSFET drivers (noninverting input for the TPS2832; inverting input for the TPS2833). |
| LOWDR | 5 | O | Output drive for the low-side power MOSFET |
| PGND | 2 | | Power ground. Connect to the FET power ground. |
| $V_{CC}$ | 4 | I | Input supply. Recommended that a 1 μF capacitor be connected from $V_{CC}$ to PGND. |

## detailed description

### low-side driver

The low-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

### high-side driver

The high-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a ground-reference driver or a floating bootstrap driver. The internal bootstrap diode, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between the BOOT terminal and ground is 30 V.

### deadtime (DT) control†

Deadtime control prevents shoot through current from flowing through the main power FETs during switching transitions by controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrn) is low; the DT terminal connects to the junction of the power FETs.

### IN†

The IN terminal is a digital terminal that is the input control signal for the drivers. The TPS2832 has a noninverting input; the TPS2833 has an inverting input.

†High-level input voltages on IN and DT must be greater than or equal to $V_{CC}$.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON) . . . . . –0.3 V to 30 V
BOOTLO to PGND . . . . . –0.3 V to 16 V
BOOT to BOOTLO . . . . . –0.3 V to 16 V
IN (see Note 2) . . . . . –0.3 V to 16 V
DT (see Note 2) . . . . . –0.3 V to 30 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, all voltages are with respect to PGND.
2. High-level input voltages on the IN and DT terminals must be greater than or equal to $V_{CC}$.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D | 580 mW | 5.8 mW/°C | 320 mW | 232 mW |

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.5 | | 15 | V |
| Input voltage | BOOT to PGND | 4.5 | | 28 | V |

### electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 6.5 V, $C_L$ = 3.3 nF (unless otherwise noted)

#### supply current

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | | 4.5 | | 15 | V |
| $V_{CC}$ | Quiescent current | $V_{CC}$ =15 V | | | | 100 | µA |
| | | $V_{CC}$ =12 V, $f_{SWX}$ = 200 kHz, $C_{HIGHDR}$ = 50 pF, | BOOTLO grounded, $C_{LOWDR}$ = 50 pF, See Note 3 | | 3 | | mA |

NOTE 3: Ensured by design, not production tested.

## electrical characteristics over recommended operating virtual junction temperature range, $V_{CC}$ = 6.5 V, $C_L$ = 3.3 nF (unless otherwise noted) (continued)

### output drivers

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Peak output-current | High-side sink (see Note 4) | Duty cycle < 2%, $t_{pw}$ < 100 µs (see Note 3) | $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, $V_{HIGHDR}$ = 4 V | 0.7 | 1.1 | | A |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 5 V | 1.1 | 1.5 | | |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 12 V, $V_{HIGHDR}$ = 10.5 V | 2 | 2.4 | | |
| | High-side source (see Note 4) | Duty cycle < 2%, $t_{pw}$ < 100 µs (see Note 3) | $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, $V_{HIGHDR}$ = 0.5V | 1.2 | 1.4 | | A |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 1.5 V | 1.3 | 1.6 | | |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 12 V, $V_{HIGHDR}$ = 1.5 V | 2.3 | 2.7 | | |
| | Low-side sink (see Note 4) | Duty cycle < 2%, $t_{pw}$ < 100 µs (see Note 3) | $V_{CC}$ = 4.5 V, $V_{LOWDR}$ = 4 V | 1.3 | 1.8 | | A |
| | | | $V_{CC}$ = 6.5 V, $V_{LOWDR}$ = 5 V | 2 | 2.5 | | |
| | | | $V_{CC}$ = 12 V, $V_{LOWDR}$ = 10.5 V | 3 | 3.5 | | |
| | Low-side source (see Note 4) | Duty cycle < 2%, $t_{pw}$ < 100 µs (see Note 3) | $V_{CC}$ = 4.5 V, $V_{LOWDR}$ = 0.5V | 1.4 | 1.7 | | A |
| | | | $V_{CC}$ = 6.5 V, $V_{LOWDR}$ = 1.5 V | 2 | 2.4 | | |
| | | | $V_{CC}$ = 12 V, $V_{LOWDR}$ = 1.5 V | 2.5 | 3 | | |
| Output resistance | High-side sink (see Note 4) | | $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, $V_{HIGHDR}$ = 0.5 V | | | 5 | Ω |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 0.5 V | | | 5 | |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 12 V, $V_{HIGHDR}$ = 0.5 V | | | 5 | |
| | High-side source (see Note 4) | | $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, $V_{HIGHDR}$ = 4 V | | | 45 | Ω |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, $V_{HIGHDR}$ = 6 V | | | 45 | |
| | | | $V_{BOOT} - V_{BOOTLO}$ = 12 V, $V_{HIGHDR}$ =11.5 V | | | 45 | |
| | Low-side sink (see Note 4) | | $V_{DRV}$ = 4.5 V, $V_{LOWDR}$ = 0.5 V | | | 9 | Ω |
| | | | $V_{DRV}$ = 6.5 V $V_{LOWDR}$ = 0.5 V | | | 7.5 | |
| | | | $V_{DRV}$ = 12 V, $V_{LOWDR}$ = 0.5 V | | | 6 | |
| | Low-side source (see Note 4) | | $V_{DRV}$ = 4.5 V, $V_{LOWDR}$ = 4 V | | | 45 | Ω |
| | | | $V_{DRV}$ = 6.5 V, $V_{LOWDR}$ = 6 V | | | 45 | |
| | | | $V_{DRV}$ = 12 V, $V_{LOWDR}$ = 11.5 V | | | 45 | |

NOTES: 3. Ensured by design, not production tested.
4. The pull-up/pull-down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

### deadtime

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| LOWDR | High-level input voltage | Over the $V_{CC}$ range (see Note 3) | 2 | | | V |
| | Low-level input voltage | | | | 1 | V |
| DT | High-level input voltage | Over the $V_{CC}$ range | 2 | | | V |
| | Low-level input voltage | | | | 1 | V |

NOTE 3: Ensured by design, not production tested.

### digital control terminals

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| High-level input voltage | Over the $V_{CC}$ range | 2 | | | V |
| Low-level input voltage | | | | 1 | V |

**switching characteristics over recommended operating virtual junction temperature range, $C_L$ = 3.3 nF (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Rise time | HIGHDR output (see Note 3) | $V_{BOOT}$ = 4.5 V, | $V_{BOOTLO}$ = 0 V | | | 60 | ns |
| | | $V_{BOOT}$ = 6.5 V, | $V_{BOOTLO}$ = 0 V | | | 50 | |
| | | $V_{BOOT}$ = 12 V, | $V_{BOOTLO}$ = 0 V | | | 50 | |
| | LOWDR output (see Note 3) | $V_{CC}$ = 4.5 V | | | | 40 | ns |
| | | $V_{CC}$ = 6.5 V | | | | 30 | |
| | | $V_{CC}$ = 12 V | | | | 30 | |
| Fall time | HIGHDR output (see Note 3) | $V_{BOOT}$ = 4.5 V, | $V_{BOOTLO}$ = 0 V | | | 60 | ns |
| | | $V_{BOOT}$ = 6.5 V, | $V_{BOOTLO}$ = 0 V | | | 50 | |
| | | $V_{BOOT}$ = 12 V, | $V_{BOOTLO}$ = 0 V | | | 50 | |
| | LOWDR output (see Note 3) | $V_{CC}$ = 4.5 V | | | | 40 | ns |
| | | $V_{CC}$ = 6.5 V | | | | 30 | |
| | | $V_{CC}$ = 12 V | | | | 30 | |
| Propagation delay time | HIGHDR going low (excluding deadtime) (see Note 3) | $V_{BOOT}$ = 4.5 V, | $V_{BOOTLO}$ = 0 V | | | 130 | ns |
| | | $V_{BOOT}$ = 6.5 V, | $V_{BOOTLO}$ = 0 V | | | 100 | |
| | | $V_{BOOT}$ = 12 V, | $V_{BOOTLO}$ = 0 V | | | 75 | |
| | LOWDR going high (excluding deadtime) (see Note 3) | $V_{BOOT}$ = 4.5 V, | $V_{BOOTLO}$ = 0 V | | | 80 | ns |
| | | $V_{BOOT}$ = 6.5 V, | $V_{BOOTLO}$ = 0 V | | | 70 | |
| | | $V_{BOOT}$ = 12 V, | $V_{BOOTLO}$ = 0 V | | | 60 | |
| Propagation delay time | LOWDR going low (excluding deadtime) (see Note 3) | $V_{CC}$ = 4.5 V | | | | 80 | ns |
| | | $V_{CC}$ = 6.5 V | | | | 70 | |
| | | $V_{CC}$ = 12 V | | | | 60 | |
| Driver nonoverlap time | DT to LOWDR and LOWDR to HIGHDR (see Note 3) | $V_{CC}$ = 4.5 V | | 40 | | 170 | ns |
| | | $V_{CC}$ = 6.5 V | | 25 | | 135 | |
| | | $V_{CC}$ = 12 V | | 15 | | 85 | |

NOTE 3: Ensured by design, not production tested.

## TYPICAL CHARACTERISTICS

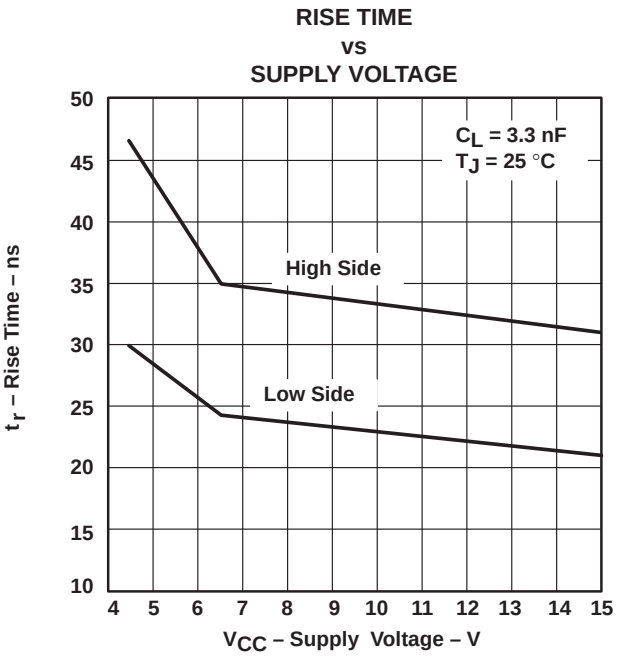



Figure 1

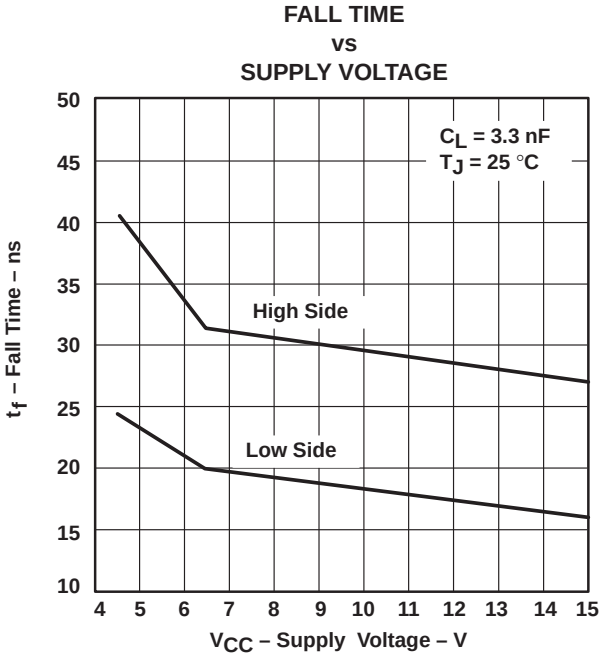



Figure 2

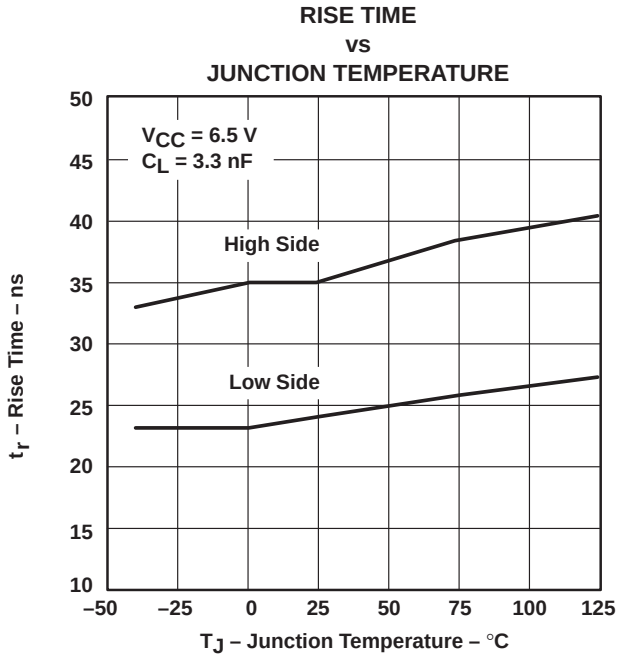



Figure 3

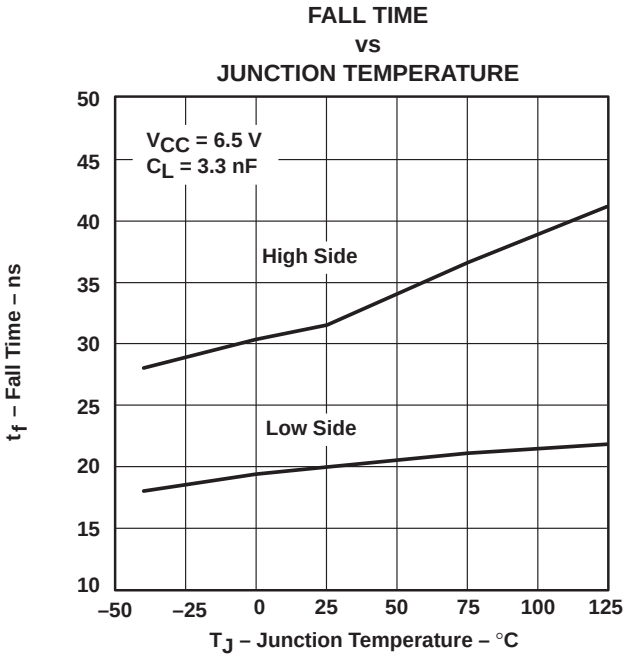



Figure 4

## TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, LOW TO HIGH LEVEL

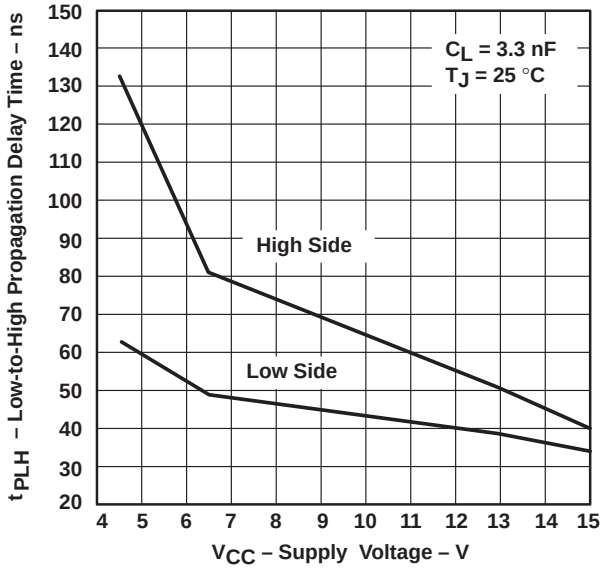



Figure 5

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE, HIGH TO LOW LEVEL

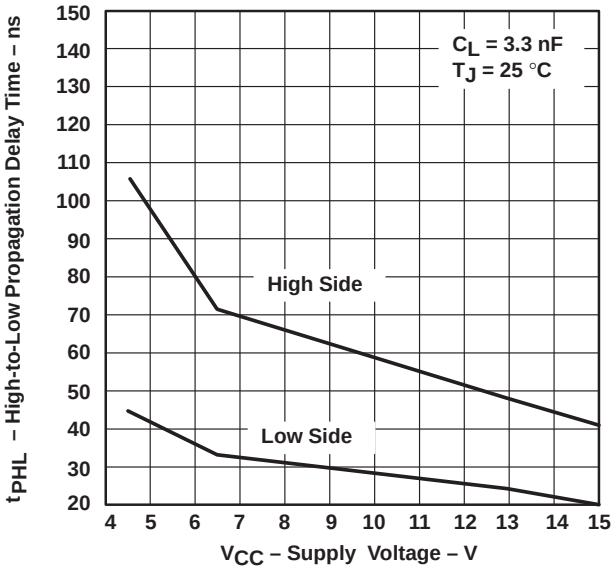



Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

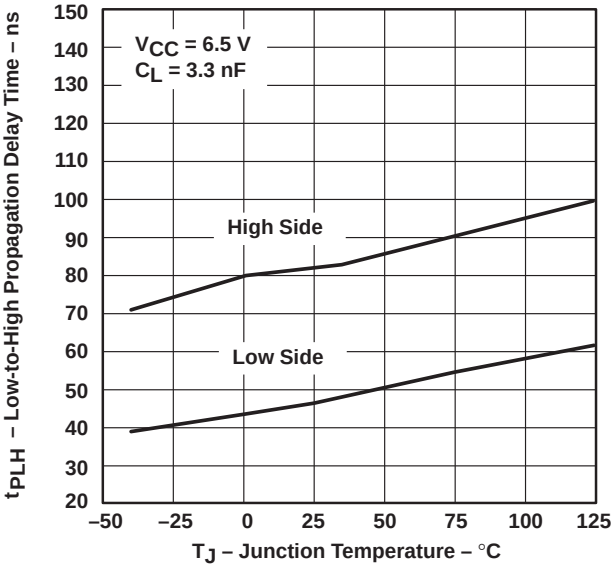



Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
JUNCTION TEMPERATURE

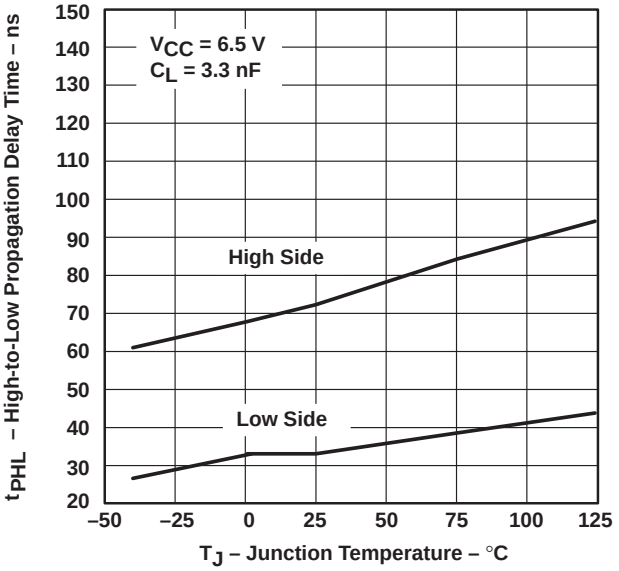



Figure 8

## TYPICAL CHARACTERISTICS

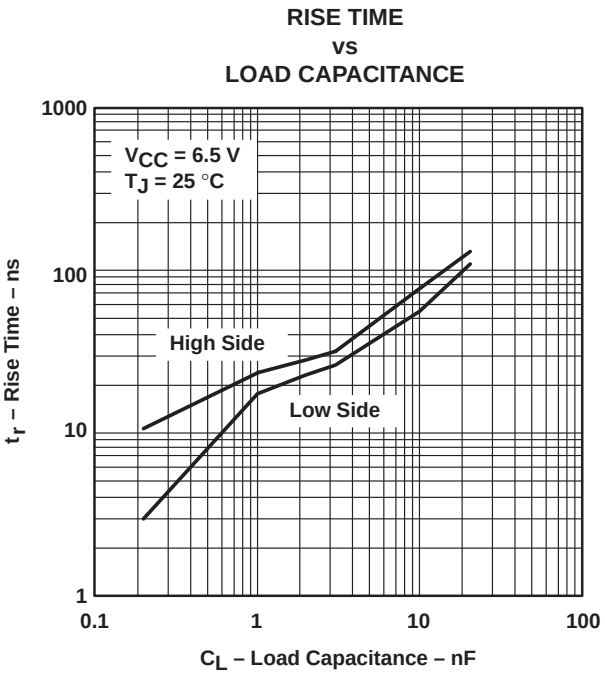



Figure 9

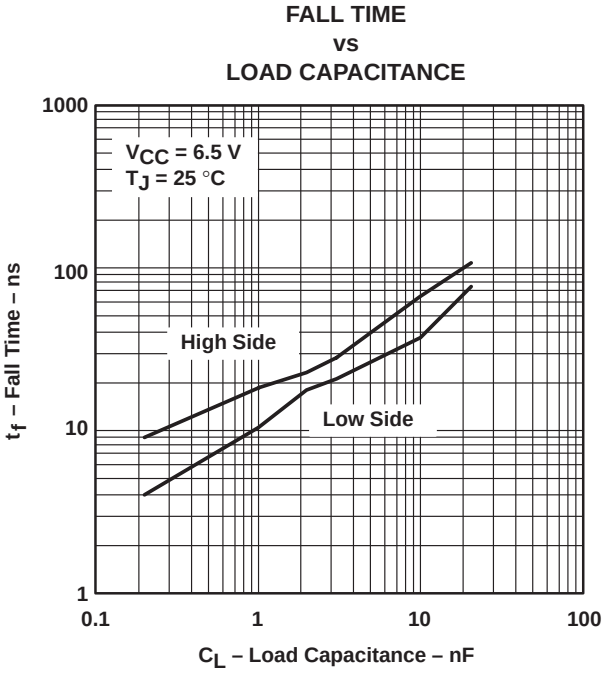



Figure 10

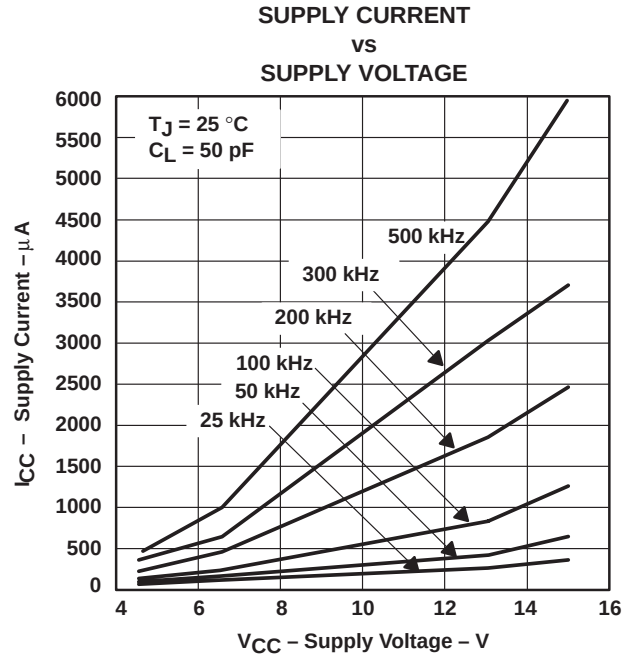



Figure 11

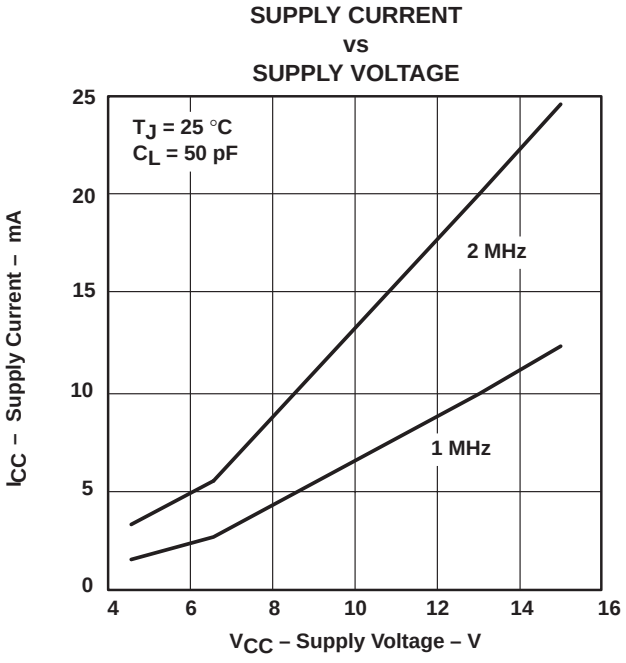



Figure 12

## TYPICAL CHARACTERISTICS

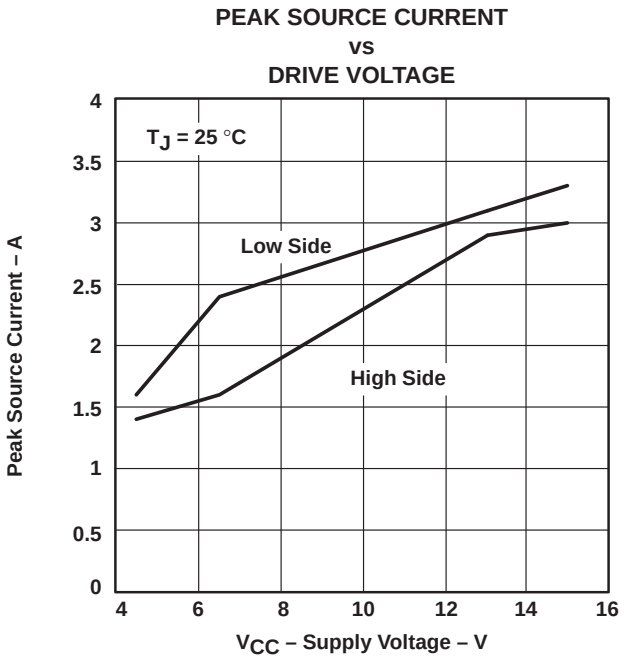



Figure 13

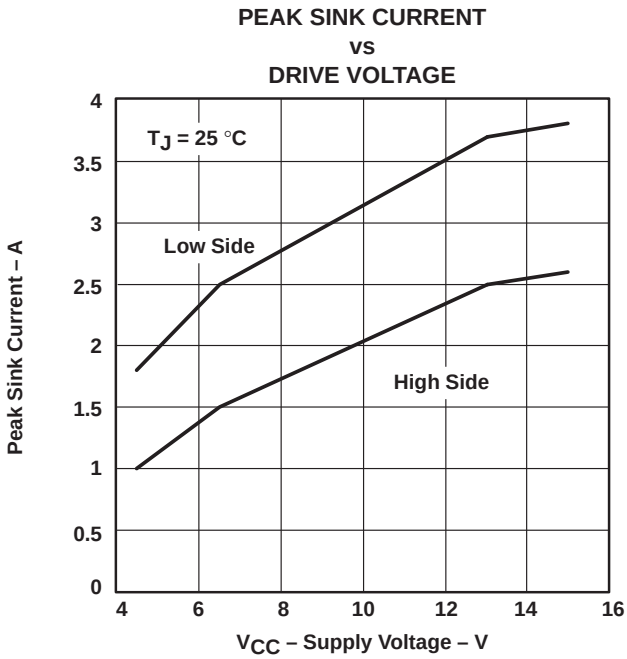



Figure 14

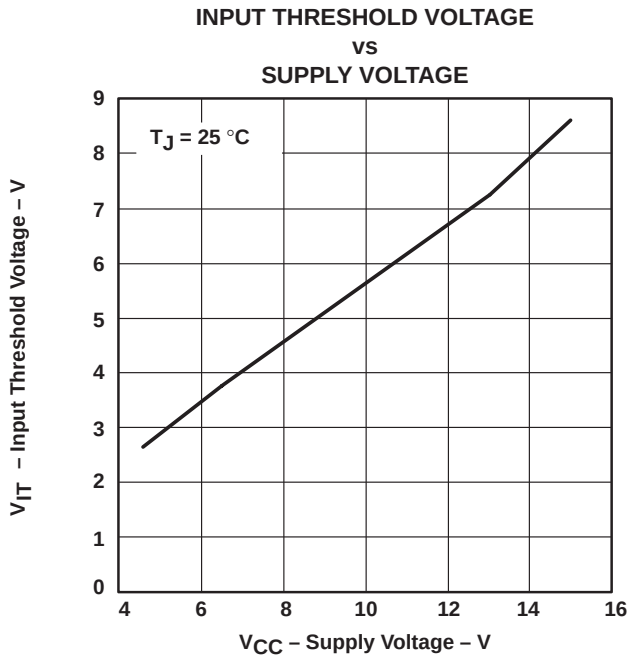



Figure 15

## APPLICATION INFORMATION

Figure 15 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2833 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3 V output. The circuit can supply 3 A continuous load and the transient load is 5 A. The converter achieves an efficiency of 94% for $V_{IN}$ = 5 V, $I_{load}$=1 A, and 93% for $V_{in}$ = 5 V, $I_{load}$ = 3 A.

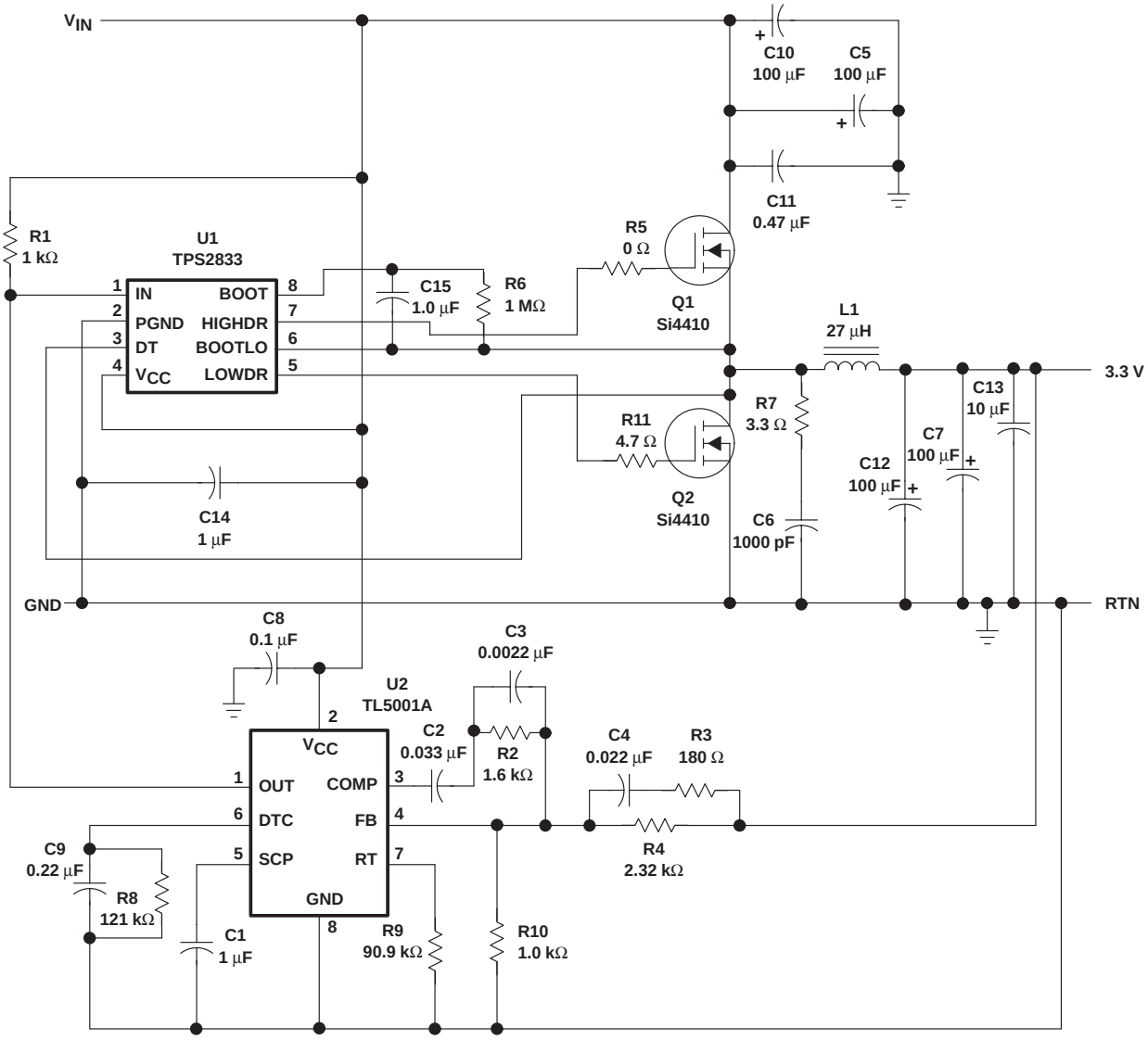



**Figure 16. 3.3 V 3 A Synchronous-Buck Converter Circuit**

## APPLICATION INFORMATION

Great care should be taken when laying out the pc board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

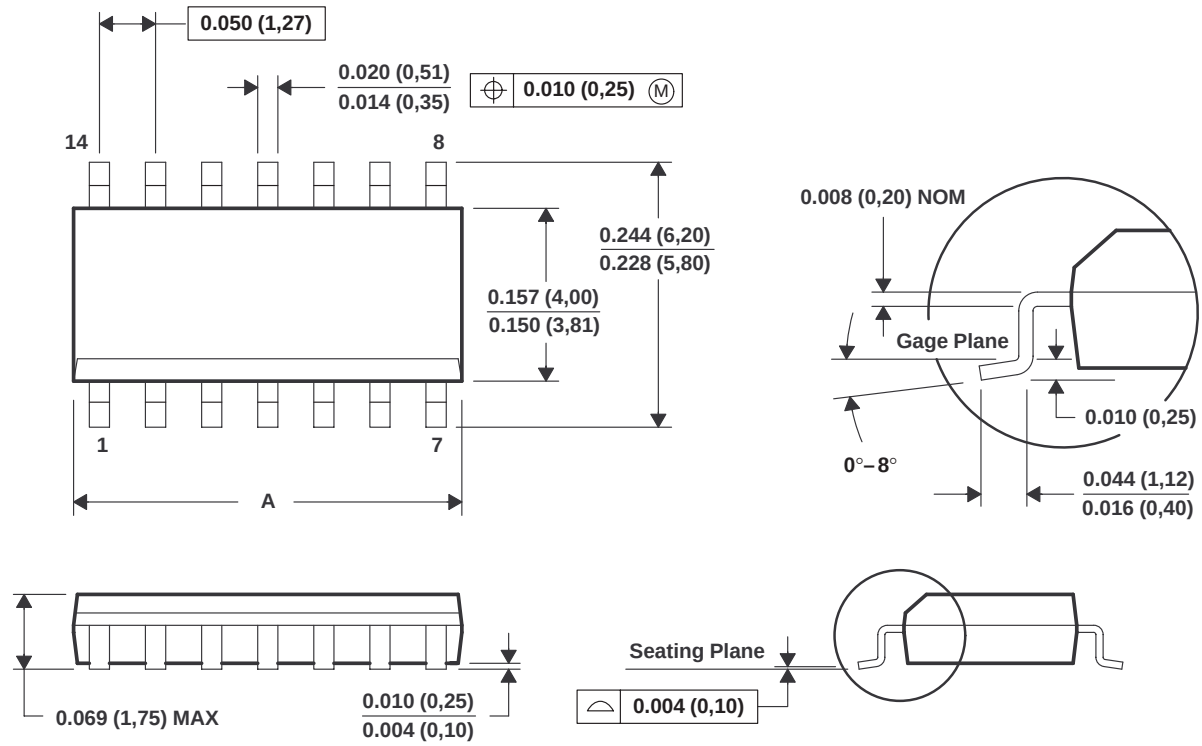
Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across $V_{CC}$ and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A) This node is very sensitive to noise pick up and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have any other EMI problems and the power supply will be relatively free of noise.

## MECHANICAL DATA

**D (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PIN SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

**4040047/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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