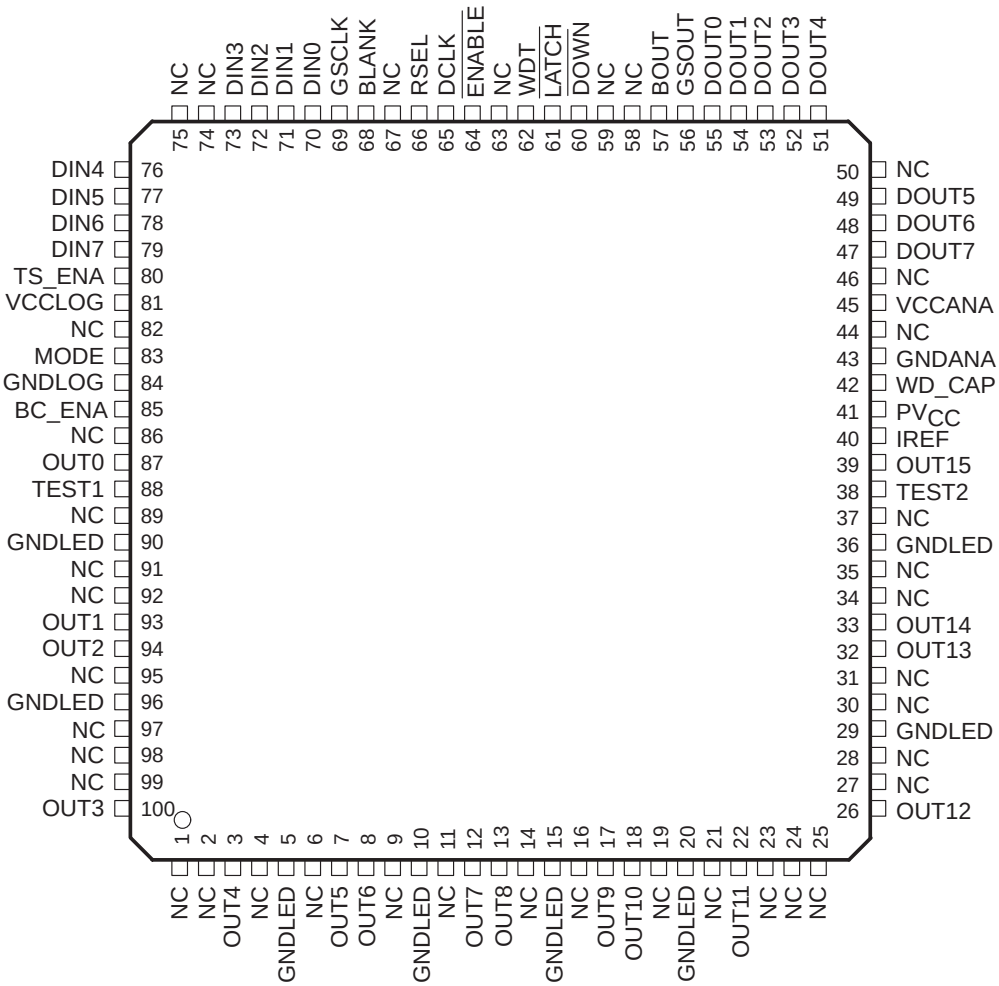
- **80 mA × 16 Bits and 120 mA × 8 Bits Drive Capability and Output Counts**
- **5 mA to 80 mA/10 mA to 120 mA Constant Current Output Range**
- **Constant Currency Accuracy of ±4% (Maximum Error Between Bits)**
- **Constant Current Output Terminals**
  - **0.4 V (Output Current 0 to 40 mA)**
  - **0.7 V (Output Current 40 to 80 mA)**
- **256 Gray Scale Display With Pulse Width Control 256 Steps**
- **Brightness Adjustment**
  - **Output Current Adjustment for 32 Steps (Adjustment for Brightness Deviation Between LEDs)**
  - **8 Steps Brightness Control by 8 Times Speed Gray Scale Control Clock (Brightness Adjustment for Panel)**
- **Protection**
  - **WDT Function**
  - **TSD Function**
- **Clock Synchronized 8-Bit Parallel Input**
- **Anode Common LED Type Applied**
- **CMOS Input Signal Level (Schmitt-Triggered Input for All Input Terminals)**
- **4.5 V to 5.5 V Power Supply Voltage**
- **15 V Maximum Output Voltage**
- **15 MHz Maximum Data Transfer Rate**
- **4 MHz Maximum Gray Scale Clock Frequency**
- **–20°C to 85°C Operating Free-Air Temperature Range**
- **100-Pin HTQFP Package (PD = 4.7 W, T_A = 25°C)**

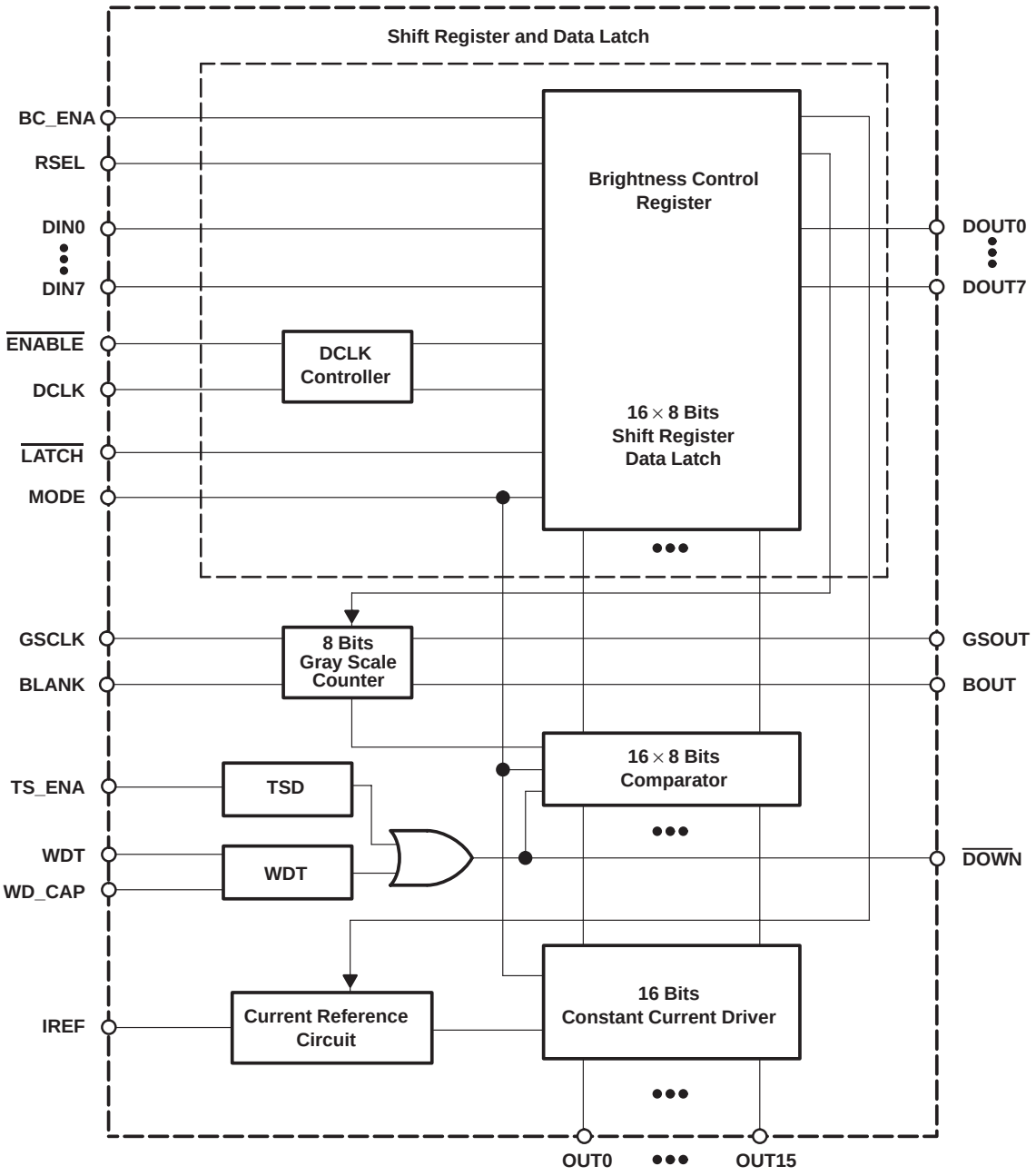
description

The TLC5902 is a constant current driver that incorporates shift register, data latch, and constant current circuitry with a current value adjustable and 256 gray-scale display that uses pulse width control. The output current can be selected as maximum 80 mA with 16 bits or 120 mA with 8 bits. The current value of the constant current output is set by one external resister. After this device is mounted on a printed-circuit board (PCB), the brightness deviation between LEDs (ICs) can be adjusted using an external data input, and the brightness control for the panel can be adjusted using the brightness adjustment circuitry. Moreover, the device incorporates watchdog timer (WDT) circuitry, which turns the constant current output off when the scan signal is stopped during dynamic scanning operation, and thermal shutdown (TSD) circuitry, which turns constant current output off when the junction temperature exceeds the limit.

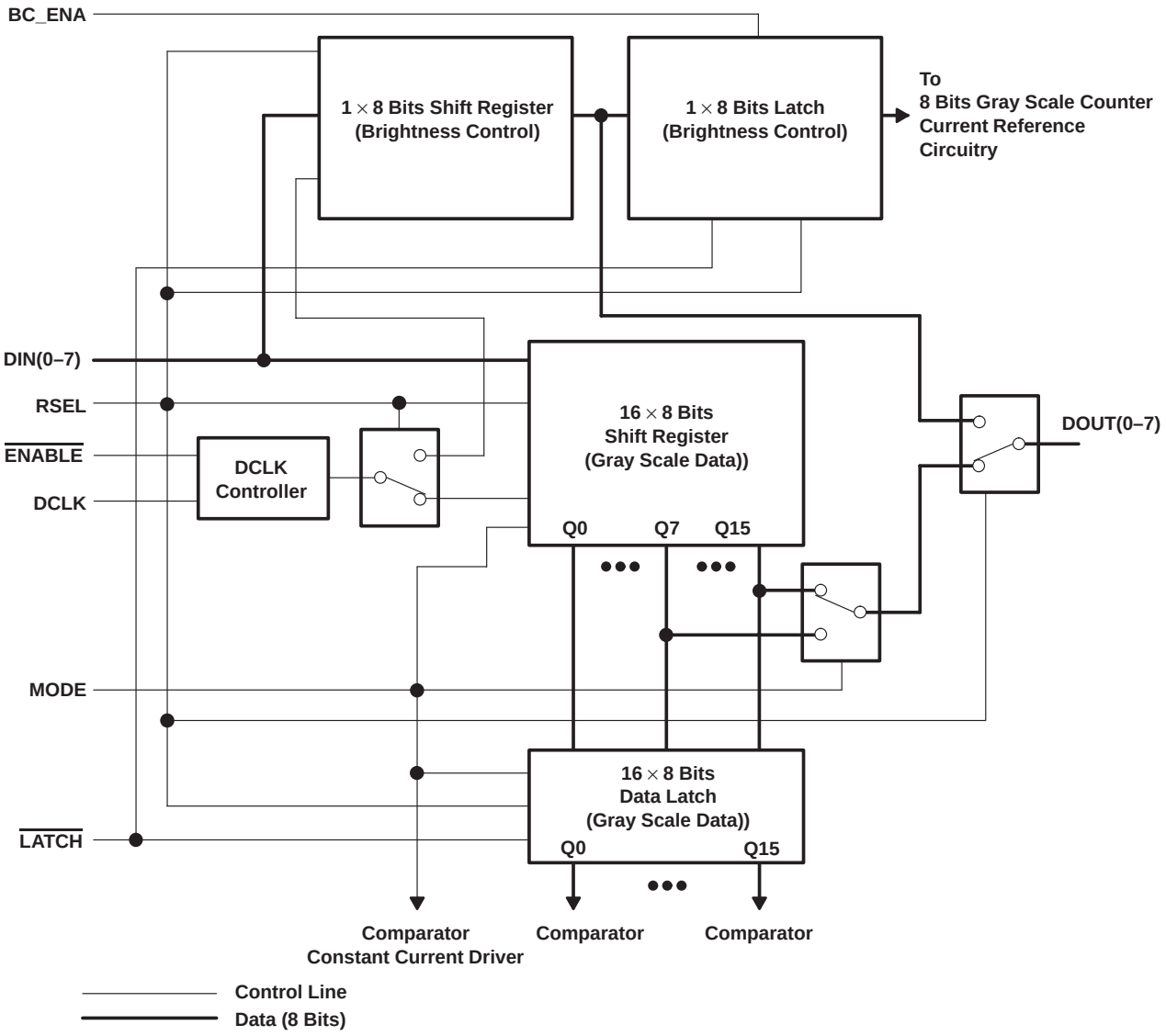
HTQFP PACKAGE
(TOP VIEW)



functional block diagram

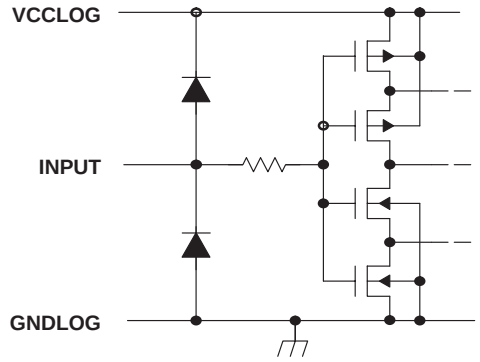


functional block diagram for shift register and data latch

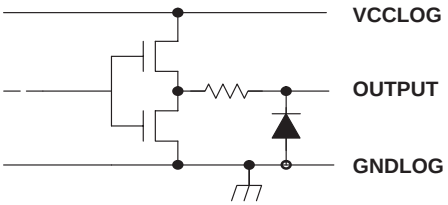


equivalent input and output schematic diagrams

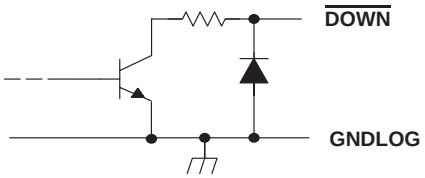
Input



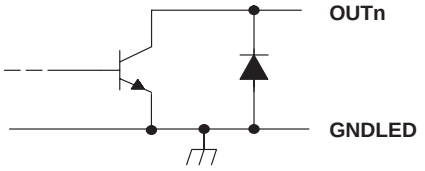
DOUT (0–7), GSOUT, BOUT



$\overline{\text{DOWN}}$



OUTn



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BC_ENA	85	I	Brightness control enable. When BC_ENA is low, the brightness control function is disabled. At this time, the brightness control latch is reset to 1Fh. Output current value is 100% of setting value by an external resistor and the frequency division ratio of GSCLK is 1/1.
BLANK	68	I	Blank (Light off). When BLANK is high, all the output of the constant current driver is turned off. All the output is turned on (LED on) synchronizing to the falling edge of GCLK after next rising edge of GCLK when BLANK goes from high to low.
BOUT	57	O	Blank signal delay. BOUT is output with the addition of delay time to BLANK.
CONDUCTIVE PAD	package surface		Heat sink pad
DCLK	65	I	Clock input for data transfer. The input data of DIN is synchronized to the rising edge of DCLK, and transferred to DOUT. DCLK is valid at the rising edge after ENABLE goes low.
DIN7–DIN0	70,71,72,73, 76,77,78,79	I	Input for shift register for both gray scale data and brightness control. It is 8 bits parallel data.
DOUT7–DOUT0	47,48,49,51, 52,53,54,55	O	Output for shift register for both gray scale data and brightness control.
$\overline{\text{DOWN}}$	60	O	Shutdown. $\overline{\text{DOWN}}$ is configured as an open collector. It goes low when the constant current output is shut down by the WDT or TSD function.
$\overline{\text{ENABLE}}$	64	I	Data transfer enable. When $\overline{\text{ENABLE}}$ is high, data is not transferred.
GNDANA	43		Analog ground. (Internally connected to GNDLOG and GNDLED)
GNDLED	5,10,15,20,29, 36,90,96		LED driver ground (Internally connected to GNDANA and GNDLOG)
GNDLOG	84		Logic ground. (Internally connected to GNDANA and GNDLED)
GSCLK	69	I	Clock input for gray scale. The gray scale display is accomplished by lighting the LED until the number of GSCLK counted is equal to the data latched.
GSOUT	56	O	Clock delay for gray scale. GSOUT is output with addition of delay time to GSCLK
IREF	40	I	Constant current control setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 38 times current is compared to current across external resistor sink on output terminal.
$\overline{\text{LATCH}}$	61	I	Latch. When $\overline{\text{LATCH}}$ is high, data on shift register goes through the latch. When $\overline{\text{LATCH}}$ is low, data is latched. Accordingly, if data on the shift register is changed during $\overline{\text{LATCH}}$ high, this new value is latched.
MODE	83	I	8/16 bits select. When the MODE is high, the 16 bits output is selected. When the MODE is low, the 8 bits output is selected.
OUT0–OUT15	87,93,94,100, 3,7,8,12,13,17, 18,22,26,32, 33,39	O	Constant current output
PV_{CC}	41		LED driver power supply voltage
RSEL	66	I	Shift register latch switching. When RSEL is low, the shift register and latch for gray scale are selected. When RSEL is high, the shift register and latch for brightness control are selected.
TEST1, TEST2	88,38	I	TEST. Factory test terminal. TEST should be connected to GND for normal operation.
TS_ENA	80	I	TSD (Thermal shutdown) enable. When TS_ENA is high, TSD is enabled. When TS_ENA is low, TSD is disabled.
VCCANA	45		Analog power supply voltage
VCCLOG	81		Logic power supply voltage
WD_CAP	42	I	WDT detection time adjustment. The capacitor for WDT detection time adjustment is connected between WD_CAP and GND. When WD_CAP is directly connected to GND, the WDT function is disabled.
WD	62	I	WDT scan input. By applying a scan signal to this terminal, the scan signal can be monitored and constant current output can be turned off. LED is protected from damage from burning when the scan signal is stopped during the constant period. The scan signal should be applied to this terminal by connecting W_CAP to GND even though no WDT function is used.

Function Tables

Truth Table (Data)

BC_ENA	$\overline{\text{ENABLE}}$	DCLK	RSEL	$\overline{\text{LATCH}}$	MODE	DOUT0 – DOUT7	OPERATION/FUNCTION
L	X	X	X	X	X	No change	Data latch for brightness control is set to 1Fh.
X	H	X	X	X	X	No change	Data transfer for gray scale and brightness control does not occur.
X	L	↑	H	X	X	Shift register for brightness control	Data of DIN0 to DIN7 is clocked into the shift register for brightness control.
X	L	↑	L	X	H	Data for shift register before 16 bytes (written before 16 times)	Data of DIN0 to DIN7 is clocked into the first byte of the shift register for gray scale data.
X	L	↑	L	X	L	Shift register for gray scale before 8 bytes (written before 8 times)	Data of DIN0 to DIN7 is clocked into the first byte of the shift register for gray scale data.
H	X	X	H	H	X	No change	Shift register for brightness control goes through data latch for brightness control.
X	X	X	L	H	X	No change	Shift register for gray scale goes through data latch for gray scale.
H	X	X	X	L	X	No change	The value for the shift register selected by RSEL is latched.

Truth Table (Display/Protection)

BLANK	GSCLK	MODE	WDT	WD_CAP	TS_ENA	OUT0~15	$\overline{\text{DOWN}}$	OPERATION/ FUNCTION
H	X	X	X	X	X	Off	Hi–Z	
L	↓	H	X	X	X	16 bits operation mode. The output is turned on if all the gray scale data is not zero on the falling edge of GCLK after the next rising edge of GCLK when BLANK goes from high to low. Each output turns off on the falling edge of GSCLK, corresponding to each gray scale data.	Hi–Z	
L	↓	L	X	X	X	8 bits operation mode. The output is turned on if all the gray scale data is not zero on the falling edge of GCLK after the next rising edge of GCLK when BLANK goes from high to low. Each output turns off on the falling edge of GSCLK corresponding to each gray scale data.	Hi–Z	
L	X	X	CLK	capacitor	X	Turn off if the level of WDT is not changed within time set by capacitor connected to WD_CAP.	L	Recover when the level of WDT changes.
L	X	X	CLK	L	X	WDT function is disabled.	Hi–Z	
L	X	X	CLK	H	X	WDT function is disabled.	Hi–Z	
L	X	X	X	X	H	Turn off if junction temperature exceeds the limit.	L	Set TS_ENA to low for recovery

absolute maximum ratings (see Note 1)†

Logic supply voltage, $V_{CC(LOG)}$ . . . . . –0.3 V to 7 V
Supply voltage for constant current circuit, PV_{CC} . . . . . –0.3 V to 7 V
Analog supply voltage, $V_{CC(ANA)}$ . . . . . –0.3 V to 7 V
Output current (DC), $I_{OL(C)}$ . . . . . 90 mA
Input voltage range . . . . . –0.3 V to $V_{CC(LOG)}$ 0.3 V
Output voltage range, $V_{(OUTn)}$, $V_{(BOUT)}$ and $V_{(GSOUT)}$ . . . . . –0.3 V to $V_{CC(LOG)}$ 0.3 V
Output voltage range, $V_{(OUTn)}$ and $V_{(DOWN)}$ . . . . . –0.3 V to 0.3 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2) . . . . . 4.7 W
Operating free air temperature range, T_A . . . . . –20°C to 85°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GNDLOG terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 38.2 mW/°C.

recommended operating conditions

dc characteristics over recommended ranges of operating free-air temperature, $V_{CC(LOG)} = V_{CC(ANA)} = PV_{CC}$ = 4.5 V to 5.5 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Logic supply voltage, $V_{CC(LOG)}$		4.5	5	5.5	V
Supply voltage for constant current circuit, PV_{CC}		4.5	5	5.5	V
Analog power supply, $V_{CC(ANA)}$		4.5	5	5.5	V
Voltage between V_{CC}, $V_{(DEF1)}$ (see Note 3)	$V_{DEF1} = V_{CC(LOG)} - V_{CC(ANA)}$ $V_{CC(LOG)} - PV_{CC}$, $V_{CC(ANA)} - PV_{CC}$	–0.3	0	0.3	V
Voltage between GND, $V_{(DEF2)}$ (see Note 3)	$V_{(DEF2)}$ = GND(LOG) – GND(ANA) GND(LOG) – GND(LED), GND(ANA) – GND(LED)	–0.3	0	0.3	V
High-level input voltage, V_{IH}		0.8 $V_{CC(LOG)}$		$V_{CC(LOG)}$	V
Low-level input voltage, V_{IL}		GND(LOG)		0.2 $V_{CC(LOG)}$	V
High-level output current, $I_{O(H)}$	$V_{CC(LOG)}$ = 4.5 V, DOUT0 to DOUT7, BOUT, GSOUT			–1	mA
Low-level output current, $I_{O(L)}$	V_{CCLOG} = 4.5 V, DOUT0 to DOUT7, BOUT, GSOUT			1	mA
	$V_{CC(LOG)}$ = 4.5 V, $\overline{DOWN}$			5	mA
Constant output current, $I_{OL(C)}$	OUT0 to OUT15	5		80	mA

NOTE 3: Each voltage is supplied by single power supply, not a separated power supply.

recommended operating conditions (continued)

ac characteristics over recommended ranges of operating free-air temperature, $V_{CC(LOG)} = V_{CC(ANA)} = PV_{CC}$ = 4.5 V to 5.5 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
DCLK clock frequency, $f_{(DCLK)}$	At single operation			15	MHz
	At cascade operation			10	
DCLK pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$		20			ns
GSCLK clock frequency, $f_{(GSCLK)}$	Frequency division ratio 1/1			4	MHz
	Frequency division ratio 1/1, T_A = 25°C, $V_{CCLOG} = V_{CCANA} = PV_{CC}$ = 5 V		8		MHz
GSCLK pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$		75			ns
WDT clock frequency, $f_{(WDT)}$				5	MHz
WDT pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$		50			ns
LAT pulse duration (high or low level), $t_{w(h)}$	LATCH	50			ns
Rise/fall time, t_r/t_f				100	ns
Setup time, t_{su}	DINn – DCLK	10			ns
	$\overline{\text{LATCH}}$ – DCLK	15			
	BLANK – GSCLK	20			
	$\overline{\text{ENABLE}}$ – DCLK	15			
	$\overline{\text{LATCH}}$ – GSCLK	10			
	RSEL – DCLK	10			
	RSEL – LATCH	20			
Hold time, t_h	DINn – DCLK	15			ns
	$\overline{\text{LATCH}}$ – DCLK	30			
	$\overline{\text{ENABLE}}$ – DCLK	20			
	RSEL – DCLK	20			
	RSEL – LATCH	20			

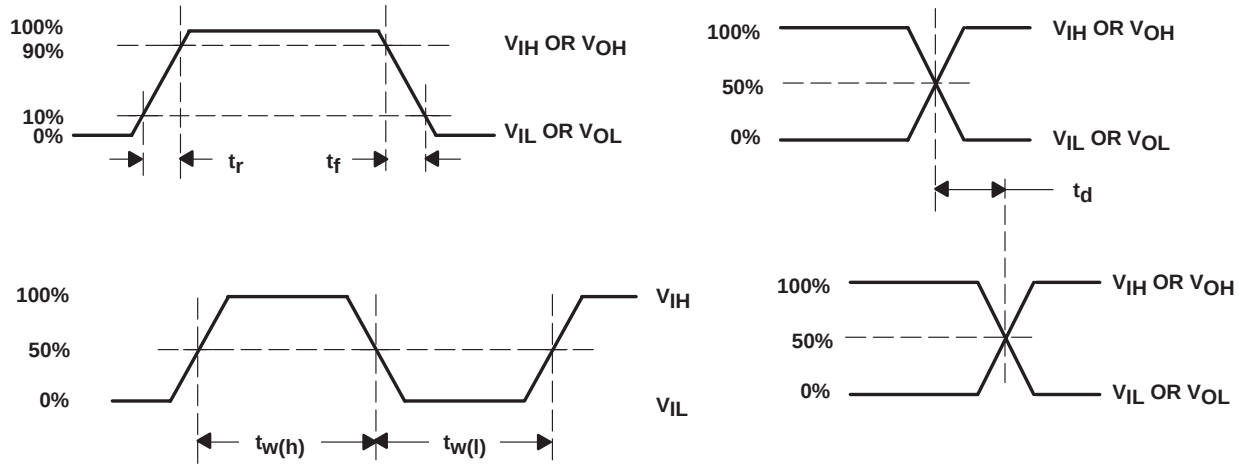
electrical characteristics, MIN/MAX: $V_{CC(LOG)} = V_{CCANA} = PV_{CC} = 4.5$ V to 5.5 V, $T_A = –20°C$ to 85°C TYP: $V_{CC(LOG)} = V_{CC(ANA)} = PV_{CC} = 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High–level output voltage	I_{OH} = –1 mA, DOUT0 to DOUT7, GSOUT, BOUT	$V_{CC(LOG)}$ –0.5V			V
V_{OL}	Low–level output voltage	I_{OL} = 1 mA, DOUT0 to DOUT7, GSOUT, BOUT			0.5	V
		I_{OL} = 5 mA $\overline{DOWN}$			0.5	
I_I	Input current	$V_I = V_{CC(LOG)}$ or GND(LOG)			±1	µA
$I_{(OG)}$	Supply current (logic)	Input signal is static, TS_ENA = H, WD_CAP = OPEN			1	mA
$I_{(LOG)}$		Data transfer, DCLK = 15 MHz, GSCLK = 1 MHz		18	30	
$I_{(ANA)}$	Supply current (analog)	LED turns on, $R_{(IREF)}$ = 590 Ω		3	5	mA
		LED turns off, $R_{(IREF)}$ = 590 Ω		3	5	
$I_{(PVCC)}$	Supply current (constant current driver)	$R_{(IREF)}$ = 1180 Ω, LED turns off		15	20	mA
		$R_{(IREF)}$ = 590 Ω, LED turns off		30	40	
		V_O = 1 V, $R_{(IREF)}$ = 1180 Ω, 16 bits output turns on		25	35	
		V_O = 1 V, $R_{(IREF)}$ = 590 Ω, 16 bits output turns on		50	70	
$I_{OL(C1)}$	Constant output current	V_O = 1 V, $V_{(IREF)}$ = 1.24 V, $R_{(IREF)}$ = 1180 Ω	35	40	45	mA
$I_{OL(C2)}$		V_O = 1 V, $V_{(IREF)}$ = 1.24 V, $R_{(IREF)}$ = 590 Ω	70	80	90	mA
I_{lkg}	Constant output leakage current	V_O = 15 V, $R_{(IREF)}$ = 590 Ω, LED turn off			10	µA
$\Delta I_{OL(C)}$	Constant output current error between bit	$V_{CC(LOG)} = V_{CC(ANA)} = PV_{CC}$ = 5 V, $V_{(IREF)}$ = 1.24 V, $R_{(IREF)}$ = 590 Ω, All bits turns on, V_O = 1 V		±1%	±4%	
$I\Delta_{OL(C1)}$	Changes in constant output current depend on supply voltage	$V_{(IREF)}$ = 1.24 V		±1%	±4%	V
$I\Delta_{OL(C2)}$	Changes in constant output current depend on output voltage	$V_{(IREF)}$ = 1.24 V, $R_{(IREF)}$ = 1180 Ω, 1 bit output turns on, V_O = 1 V to 3 V		±1%	±2%	V
$T_{(tsd)}$	TSD detection temperature (thermal shutdown circuit)	Junction temperature	150	160	170	°C
$T_{(wdt)}$	WDT detection time (watch–dog timer circuit)	No external capacitor	1	3	8	ms
$V_{(IREF)}$	Voltage reference	BC_ENA = L, $R_{(IREF)}$ = 590 Ω		1.24		V

switching characteristics, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	DOUT		12	30	ns
		OUT		250		
		GSOUT		13	30	
		BOUT		13	30	
t_f	Fall time	DOUT		8	20	ns
		OUT		150		
		GSOUT		10	25	
		BOUT		10	25	
t_d	Propagation delay time	OUTn+1 – OUTn		8	15	ns
		BLANK ↑ – OUT0		350	500	
		GSCLK ↓ – OUT0		350	500	
		DCLK ↑ – DOUT	15	30	50	
		GSCLK – GSOUT	10	25	50	
		BLANK – BOUT	10	25	50	

timing requirements



PRINCIPLES OF OPERATION

constant current output selection by user (80 mA × 16 bits or 120 mA × 8 bits)

When MODE terminal is set to high, output is selected as 80 mA × 16 bits. When MODE terminal is set to low, output is selected as 120 mA × 8 bits. By this setting, the internal shift register and latch are changed. Note that two constant output terminals should be tied, such as OUT0 to OUT1 and OUT2 to OUT3 when 8-bit output is selected.

MODE	OUTPUT
H	80 mA x 16 bits
L	120 mA x 8 bits

setting for constant current value

On the constant current output terminals (OUT0 to OUT15), approximately 38 times the current that flows through the external resistor, $R_{(IREF)}$ (connected between IREF and GND), can flow. The external resistor value is calculated using the following equation.

$$\frac{I_{(OUTn)}(mA) \cong 38 \times 1.24(V)}{R_{(IREF)}(k\Omega)} \quad (1)$$

More current flows if IREF is connected to GND directly.

shift register latch for gray scale data

The shift register latch for gray scale data is set as 8 × 8 bits configuration each at 8 bit mode, and as 16 x 8 bits configuration each at 16-bit mode. By setting RSEL to low, the shift register latch for gray scale data is selected. Data structure shows that DIN0 corresponds to LSB, and DIN7 to MSB. This results in 2^8 = 256 steps gray scale. The latched data is compared to GSCLK (clock for gray scale) counts, and constant current output continues to turn on until these values are equal.

shift register latch for brightness control

The shift register latch for brightness control is configured with 1 × 8 bits each. The data input terminal and latch terminal are common to shift register latch for gray scale data. By setting RSEL to low, the shift register latch for gray scale data is selected, and by setting RSEL to high, the shift register latch for brightness control is selected. If the brightness control function is not used, BC_ENA terminal should be pulled low. Since the brightness control latch is reset to initial value of 00011111h, it is not necessary to write data to shift register latch for brightness control. When power is up, latch data is undetermined. Data should be written to shift register latch when the brightness control function is used. Also, rewriting the latch value for brightness control is inhibited when the LED is turned on.

RSEL	SHIFT REGISTER LATCH SELECTED
L	Shift register latch for gray scale data
H	Shift register latch for brightness control

PRINCIPLES OF OPERATION

write data to both shift register latches

The shift register latch is selected using the RSEL terminal. The data input method is the same for both shift register latches. The data is applied to DIN0 to DIN7 of 8-bits data input terminal, and transferred synchronizing to DCLK. The data of DIN0 to DIN7 is transferred to the direction from OUT0 to OUT15 synchronizing to DCLK. The shift register for brightness control is 1-bit length resulting in one time of DCLK input. The shift register for gray scale data is 8-bits length at 8-bit mode resulting in eight times of DCLK, and 16-bit length at 16-bit mode resulting in 16 times of DCLK input. At the number of DCLK input for each case, output data appear on DOUT0 to DOUT7. When $\overline{\text{LATCH}}$ goes from low to high, data is latched internally. Then, when $\overline{\text{LATCH}}$ goes low, data is held. RSEL switching should be done when DCLK and $\overline{\text{LATCH}}$ are low.

brightness control latch configuration

The brightness control latch is configured as DIN0 corresponds to LSB, and DIN7 to MSB. The lower 5 bits are assigned for output current adjustment, and the upper 3 bits are for a frequency division ratio setting of GSCLK.

DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
MSB	. . . .	. . . .	. . . .	. . . .	. . . .	. . . .	LSB
0†	0	0	1	1	1	1	1
Frequency division ratio setting of GSCLK			Output current setting				

† BC_ENA is low.

output current adjustment – brightness adjustment between ICs

By using the lower 5 bits of the brightness control latch, output current can be adjusted to 32 steps. When output current is set to 100% by the external resistor at 11111h of the latched value, it is adjusted as 1 step or 32 steps of 1.6% current ratio between 100 and 51.6%. By using this function, the brightness control between modules (ICs) can be adjusted, sending the desired data externally even if ICs are mounted on PCB. When BC_ENA is pulled low, the latch is reset to the initial value of 00011111h, and the output current is set to 100%.

CODE	CURRENT RATIO (%)	20 (mA)	80 (mA)	V_{IREF} (TYP)
MSB 00000 LSB	51.6	10.3	41.3	0.64
. . . .	. . . .	. . . .	. . . .	. . . .
11110	98.4	19.7	78.7	1.22
11111†	100	20.0	80.0	1.24

† BC_ENA is low.

PRINCIPLES OF OPERATION

frequency division ratio setting for GSCLK(clock for gray scale) – panel brightness adjustment

By using the upper 3 bits of the brightness control latch, GSCLK can be divided into 1/1 to 1/8. If GSCLK is set to 8 times the speed ($256 \times 8 = 2048$) of the frequency during the horizontal scanning time, the brightness can be adjusted to 8 steps by selecting the frequency division ratio. Thus, the total panel brightness can be adjusted at once and applied to the brightness of day or night. When BC_ENA is pulled low, GSCLK is not divided. When BC_ENA is pulled high, the brightness can be adjusted as shown in the following table.

CODE	FREQUENCY DIVISION RATIO	RELATIVE BRIGHTNESS RATIO (%)
MSB 000 LSB†	1/1	12.5
001	1/2	25.0
010	1/3	37.5
011	1/4	50.0
100	1/5	62.5
101	1/6	75.0
110	1/7	87.5
111	1/8	100

† BC_ENA is low.

constant output current operation

The constant current output turns on (sink constant current) if all the gray-scale data latched into the gray-scale latch is not zero on the falling edge of GCLK, after the next rising edge of GCLK when BLANK goes from high to low. After that, the number of the falling edge is counted by the 8-bit gray scale counter. Output counted that corresponds to gray-scale data is turned off (stop to sink constant current). If the shift register for gray scale is updated during $\overline{\text{LATCH}}$ high, data on the gray-scale data latch is also updated, affecting the number of gray scale of constant current output. Accordingly, during the on state of constant current output, $\overline{\text{LATCH}}$ is kept to low and the gray-scale data latch is held. When unconnected constant current output terminals exist, operation is complete after writing zero (data for LED turn off) to the corresponding gray-scale data latch. If this action is not completed, the supply current (I_{PVCC}) in the constant current driver portion increases.

protection

This device incorporates WDT and TSD functions. In WDT or TSD functions, the current output is stopped (Logic portion is still operating). By monitoring the $\overline{\text{DOWN}}$ terminal, these failures are detected immediately. Since $\overline{\text{DOWN}}$ output is configured as an open collector, outputs of multiple ICs are brought together.

WDT

When the scan signal is stopped during a fixed period in dynamic scanning operation, the constant current output is turned off, preventing the LED from burning damage. The time detected can be set using the external capacitor (C1). The typical value is approximately 3 ms without a capacitor, 33 ms with a 1000 pF capacitor, and 300 ms with a 0.01 μF capacitor. Once the scan signal is applied again, the abnormal status is released and normal operation is resumed. During static operation, the WDT function is disabled, connecting WD_CAP to GND. The scan signal should be applied to the WDT terminal even though the WDT function is not used.

PRINCIPLES OF OPERATION

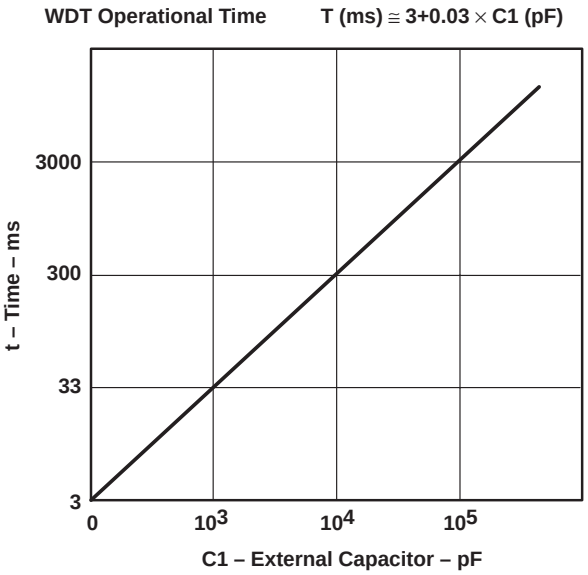


Figure 1. WDT Operational Time

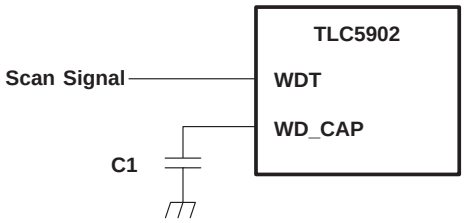


Figure 2. WDT Usage Example

TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD functions and turns the constant current output off. When TSD is used, TS_ENA is pulled high. When TSD is not used, TS_ENA is pulled low. To recover to normal operation, the power supply is turned off or TS_ENA is pulled low.

noise reduction

concurrent switching noise reduction

The concurrent switching noise has a potential to occur when multiple outputs turn on or off at the same time. To prevent this noise, the device has delay output terminals such as GSOUT and BOUT for GSCLK and BLANK respectively. Connecting these outputs to GSCLK and BLANK terminals of the next stage IC allows differences in the switching time between ICs to be made. When GSCLK is output to GSOUT through the device, duty is changed, so that the number of stages to be connected will be limited to a maximum of 10 at GSCLK = 4 MHz.

output slope

The on and off time of constant current output at an output current of 80 mA is approximately 150 ns and 250 ns respectively. It is effective in reducing concurrent switching noise that occurs when multiple outputs turn on or off at the same time.

delay between constant current output

The constant current output has a delay time of approximately 8 ns between output. It means approximately 120 ns delay time exists between OUT0 and OUT15. This time difference by delay is effective for reduction of concurrent switching noise as well as output slope. This delay time has the same value at 8-bits or 16-bits operation mode.

PRINCIPLES OF OPERATION

noise reduction (continued)

power supply

VCCLOG, VCCANA, and PVCC are supplied by a single power supply to minimize voltage differences between these terminals.

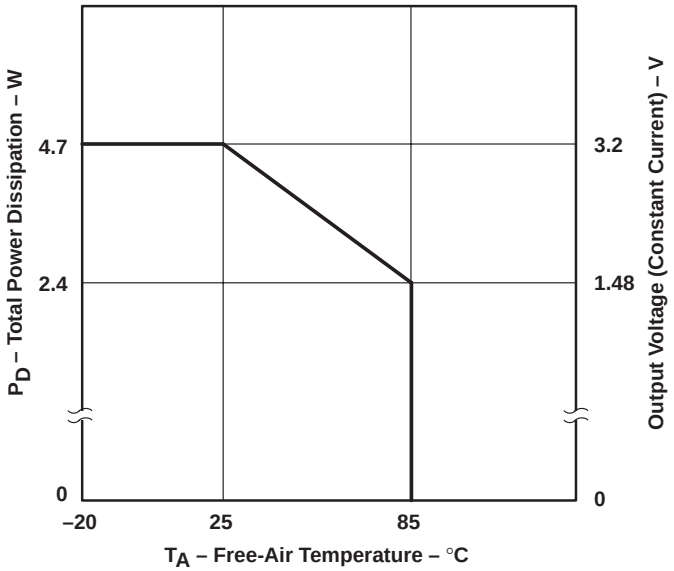
The bypass capacitor is located between power supply and GND to eliminate the variation of power supply voltage.

GND

Although GNDLOG, GNDANA, and GNDLED are internally tied together, these terminals should be externally connected to reduce noise influence.

heat sink pad

The heat sink pad should be connected to GND to eliminate the noise influence since it is connected to the bottom side of the IC chip. Also, the desired thermal effect is obtained by connecting this pad to the PCB pattern with better thermal conductivity.



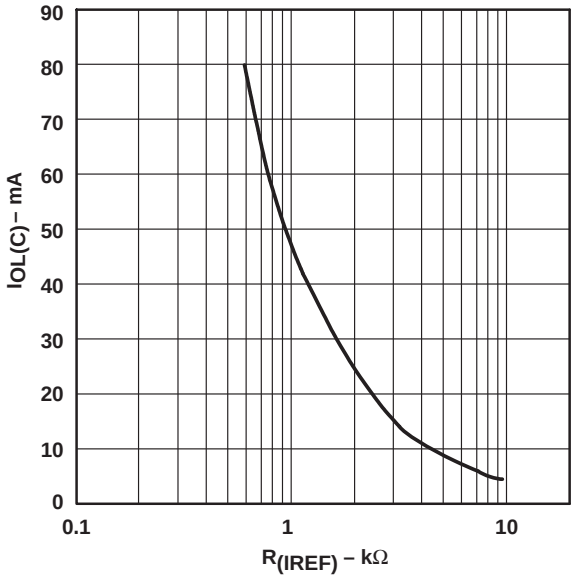
NOTES: A. IC is mounted on PCB. PCB size: $102 \times 76 \times 1.6$ [mm^3], four layers with internal two layer having plane. The thermal pad is soldered to PCB pattern of 10 mm^2. For operation above 25°C free-air temperature, derate linearly at the rate of 38.2 mW/°C.

VCCLOG = VCCANA = PVCC = 5 V, $I_{OL(C)}$ = 80 mA, I_{CC} is typical value

B. Consider thermal characteristics when selecting the material for the PCB, since the temperature will rise around the thermal pad.

Figure 3. Power Rating

PRINCIPLES OF OPERATION



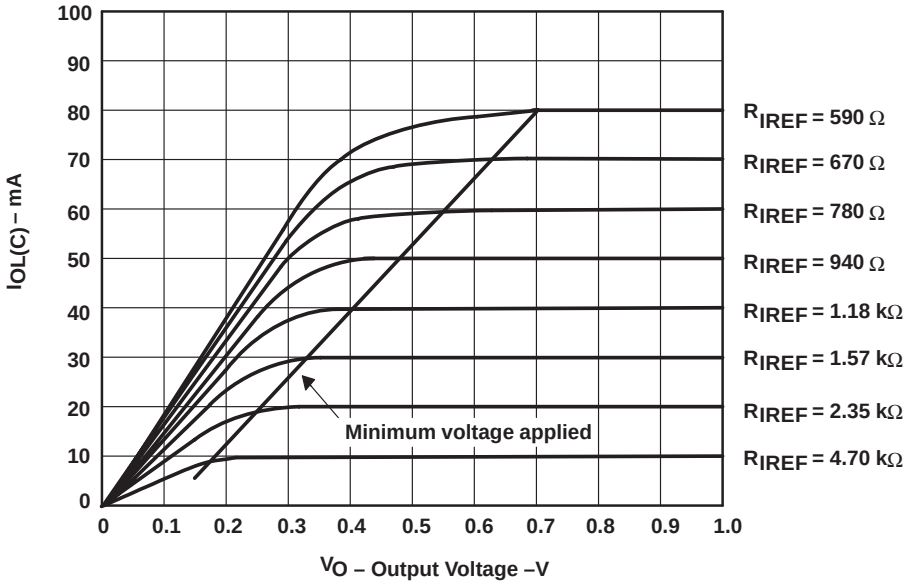
Conditions : V_O = 1 V, $V_{(IREF)}$ = 1.24 V

$$I_{OL(C)}(mA) \approx \frac{V_{(IREF)}(V)}{R_{(IREF)}(k\Omega)} \times 38$$

$$R_{(IREF)}(k\Omega) \approx \frac{47}{I_{OL(C)}(mA)}$$

NOTE: The output current is at 16 bit output.
When 8-bit output, it will be the current of sum of two outputs. This sum current should be set up with the range of 10 mA to 120 mA. The resistor, R_{IRF}, should be located as close as possible to IREF terminal to eliminate the noise influence.

Figure 4. Current on Constant Current Output vs External Resistor



NOTE: VCCLOG = VCCANA = PVCC = 5 V, T_A = 25°C.

Figure 5. Current on Constant Current Output vs Voltage Applied To Constant Current Output Terminal

PRINCIPLES OF OPERATION

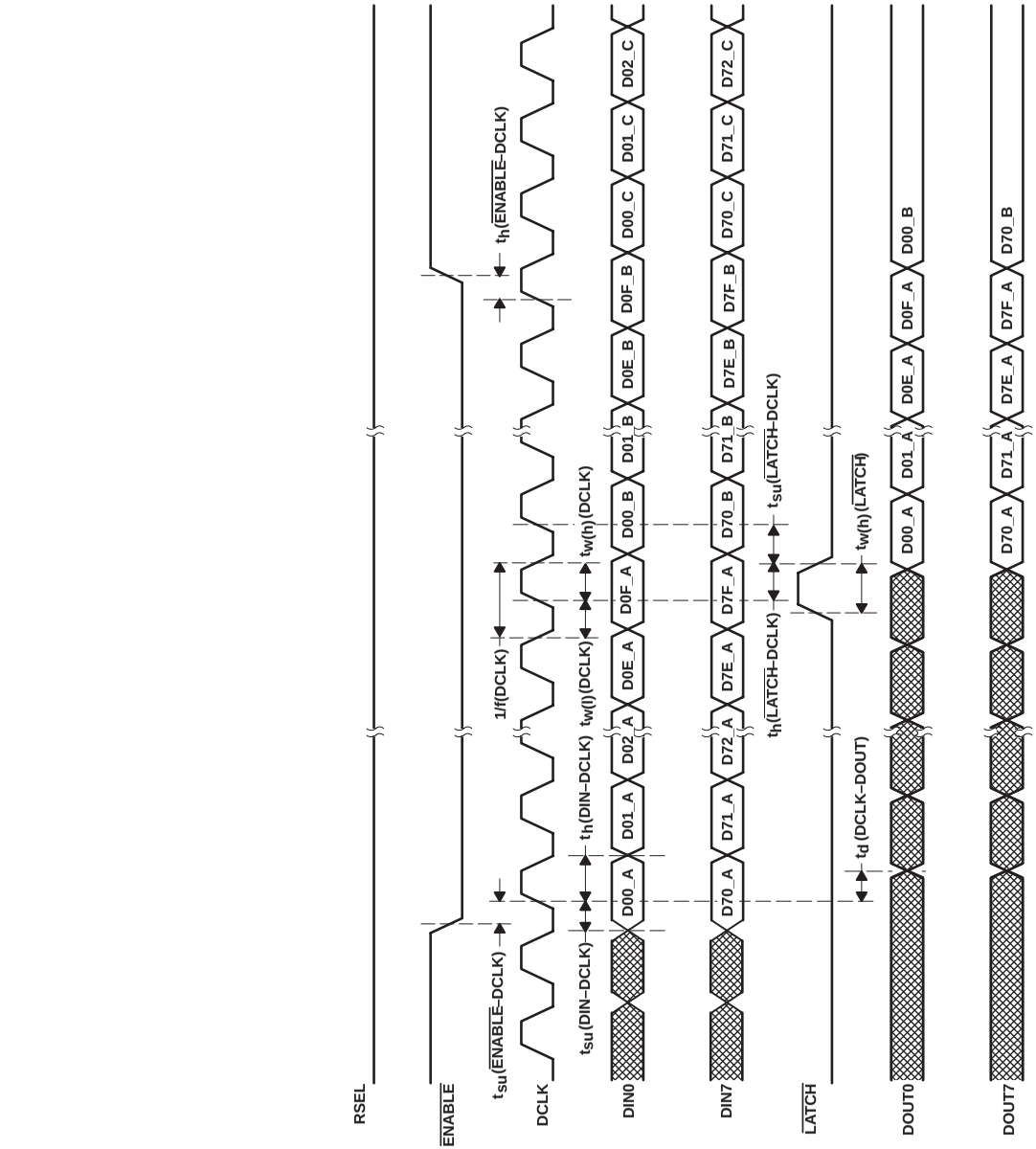
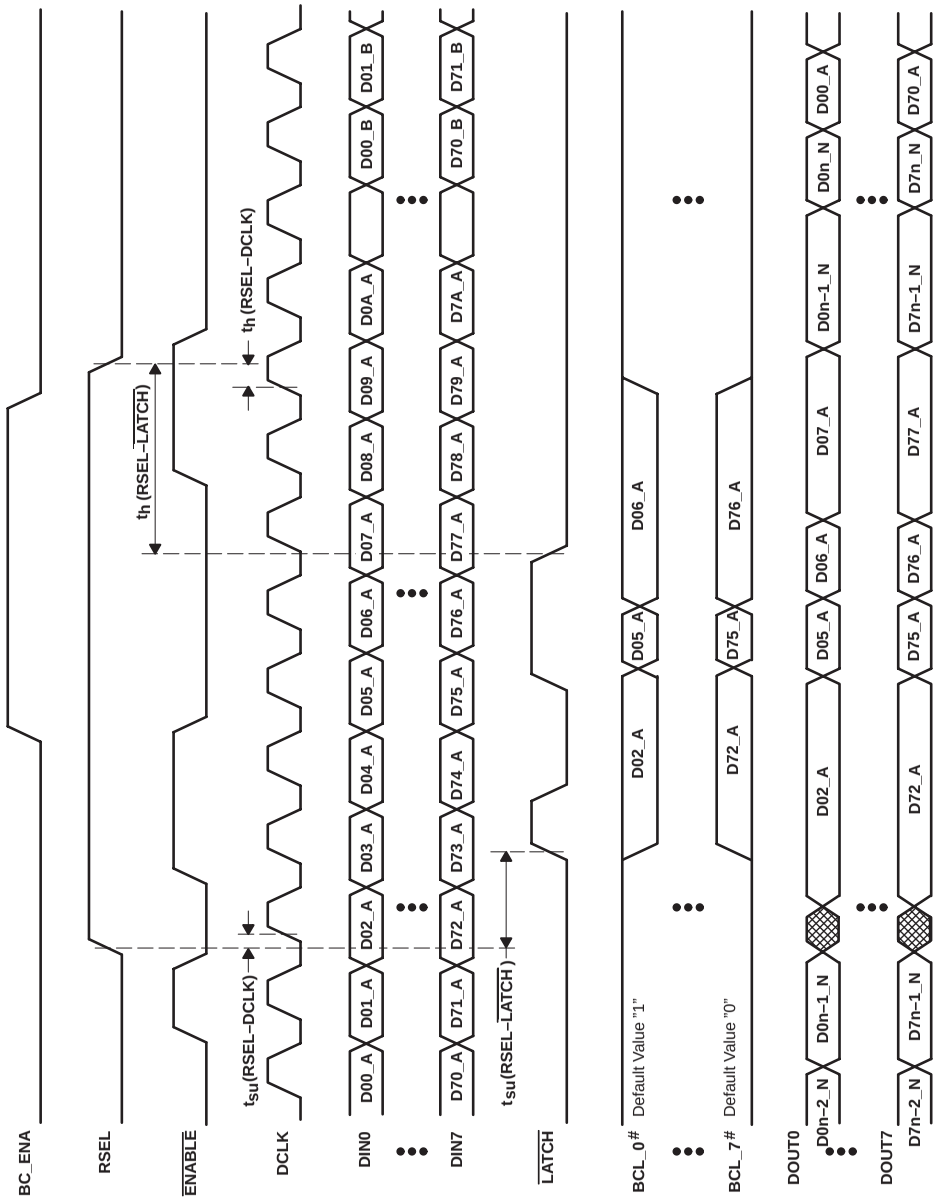


Figure 6. Timing Diagram (Shift Register for Gray Scale Data)

PRINCIPLES OF OPERATION



#Internal brightness control latch

Figure 7. Timing Diagram (Brightness Control Register)

PRINCIPLES OF OPERATION

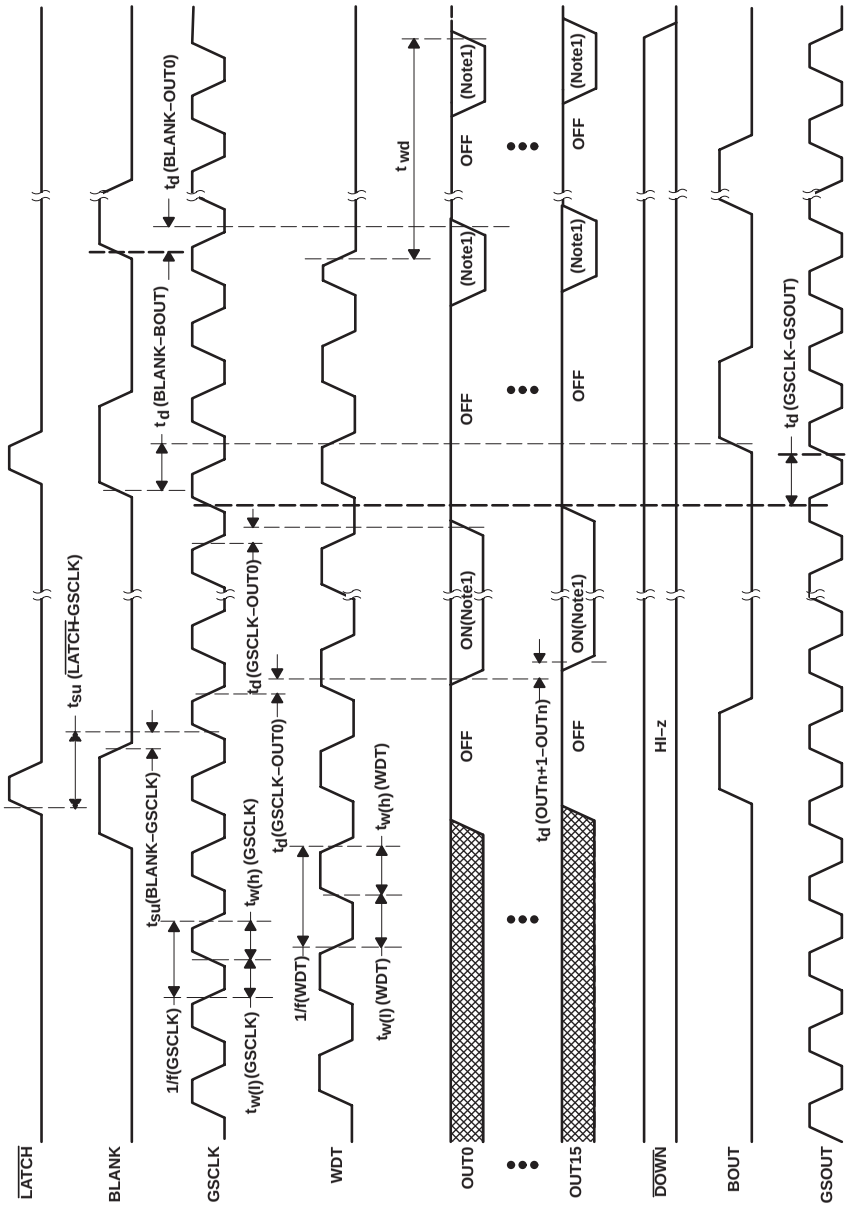
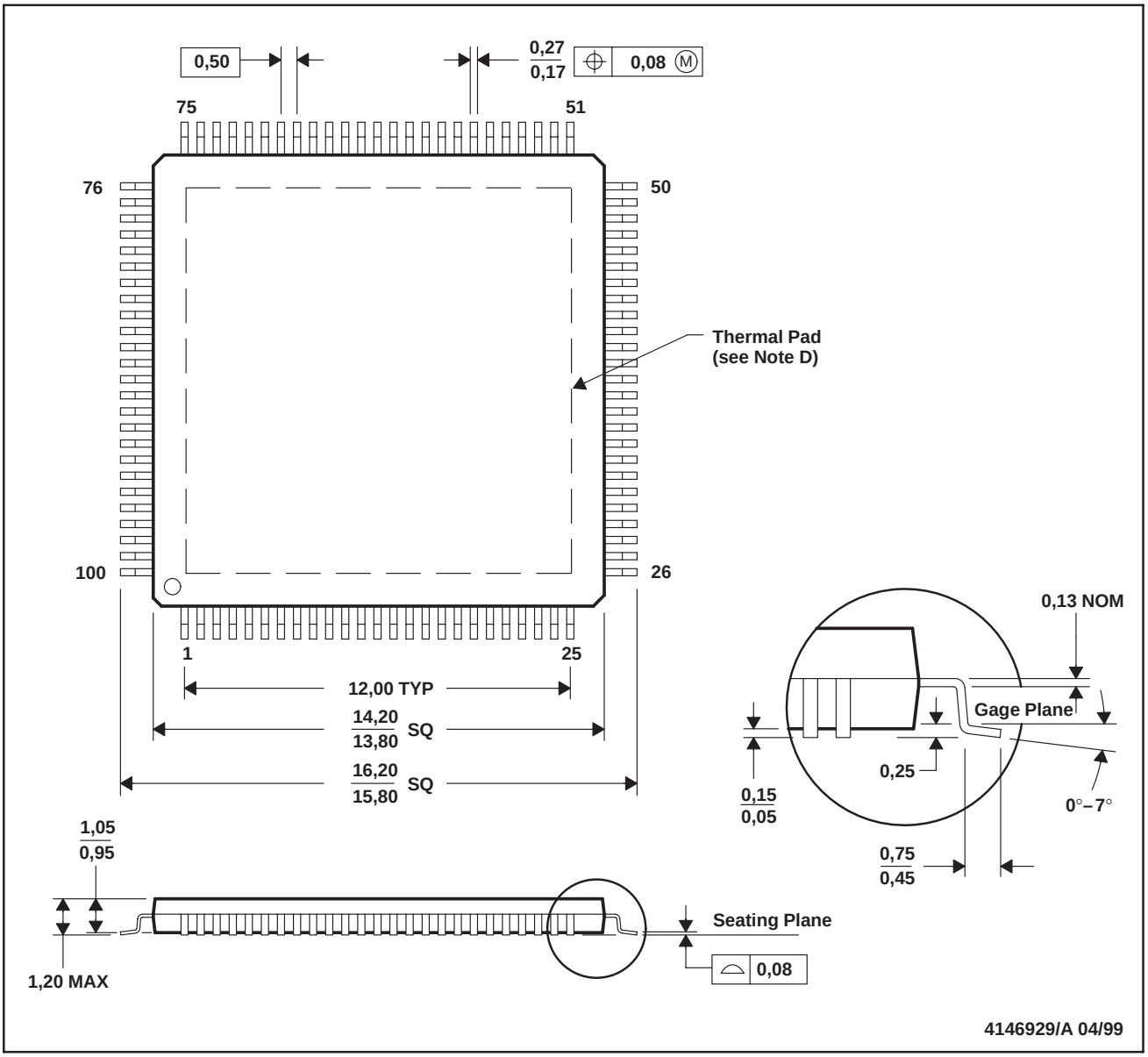


Figure 8. Timing Diagram (Constant Current Output)

NOTE 1: ON or OFF, or ON time is varied depending on the gray scale data and BLANK.

MECHANICAL DATA

PZP (S-PQFP-G100) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimensions of the thermal pad are 2 mm × 2 mm (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MS-026

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