- **Member of the Texas Instruments *Widebus*™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **1024 Words × 18 Bits**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 20 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Package Options Include 68-Pin Ceramic PGA (GB) or Space-Saving 68-Pin Ceramic Quad Flatpack (HV)†**

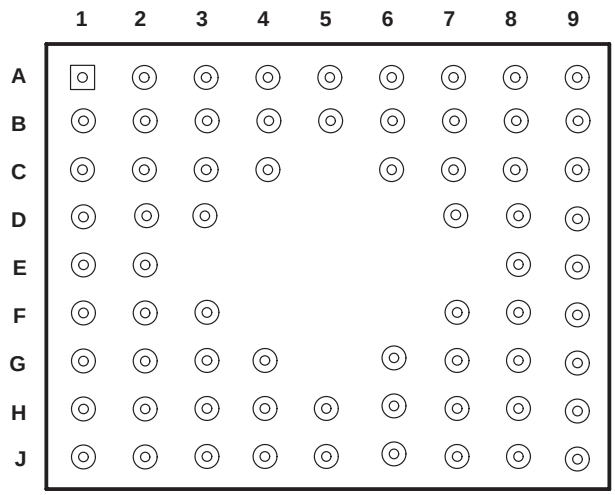
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN54ACT7811 is a 1024 × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 28.5 MHz and access times of 20 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN54ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

The SN54ACT7811 is characterized for operation from –55°C to 125°C.

GB PACKAGE
(TOP VIEW)



† The SN54ACT7811 HV is not production released.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

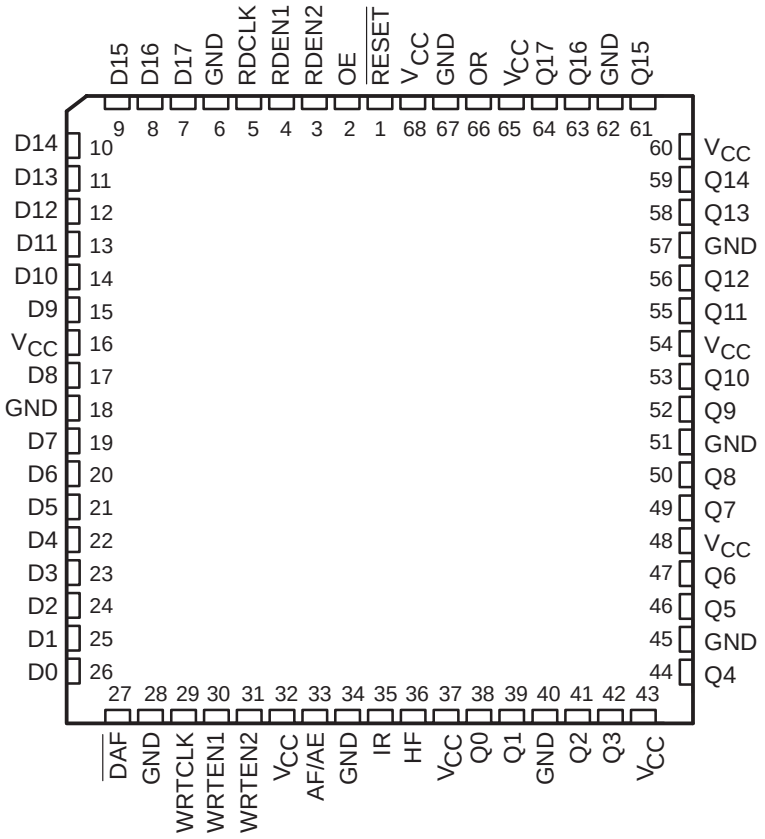
Widebus is a trademark of Texas Instruments Incorporated.

GB-Package Terminal Assignments

TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME
A1	Q15	B7	Q5	F2	D17	H8	D0
A2	Q13	B8	Q4	F8	WRTEN2	H9	$\overline{\text{DAF}}$
A3	Q12	B9	Q1	F9	AF/AE	J1	D11
A4	Q11	C1	$\overline{\text{RESET}}$	G1	D16	J2	D10
A5	Q10	C2	Q16	G2	D15	J3	D8
A6	Q8	C8	Q2	G8	WRTCLK	J4	NC
A7	Q7	C9	Q0	G9	WRTEN1	J5	D7
A8	Q6	D1	OE	H1	D14	J6	D6
A9	Q3	D9	HF	H2	D13	J7	D5
B1	OR	E1	RDEN1	H3	D12	J8	D3
B2	Q17	E2	RDEN2	H4	D9	J9	D2
B3	Q14	E9	IR	H6	D4		
B5	Q9	F1	RDCLK	H7	D1		

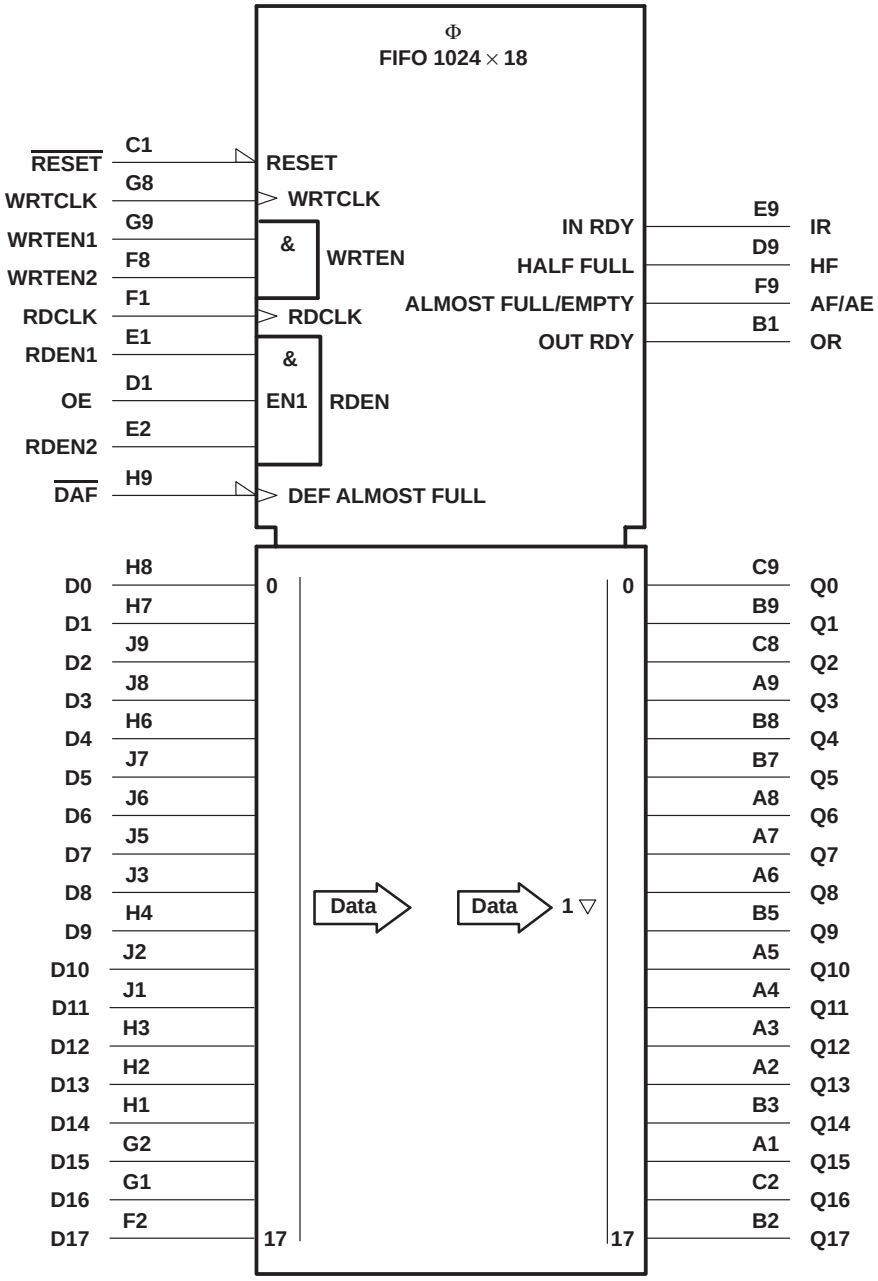
V_{CC} = B4, C6, C7, D2, D7, E8, G3, G4, G6 GND = B6, C3, C4, D3, D8, F3, F7, G7, H5
NC = No internal connection

HV PACKAGE†
(TOP VIEW)



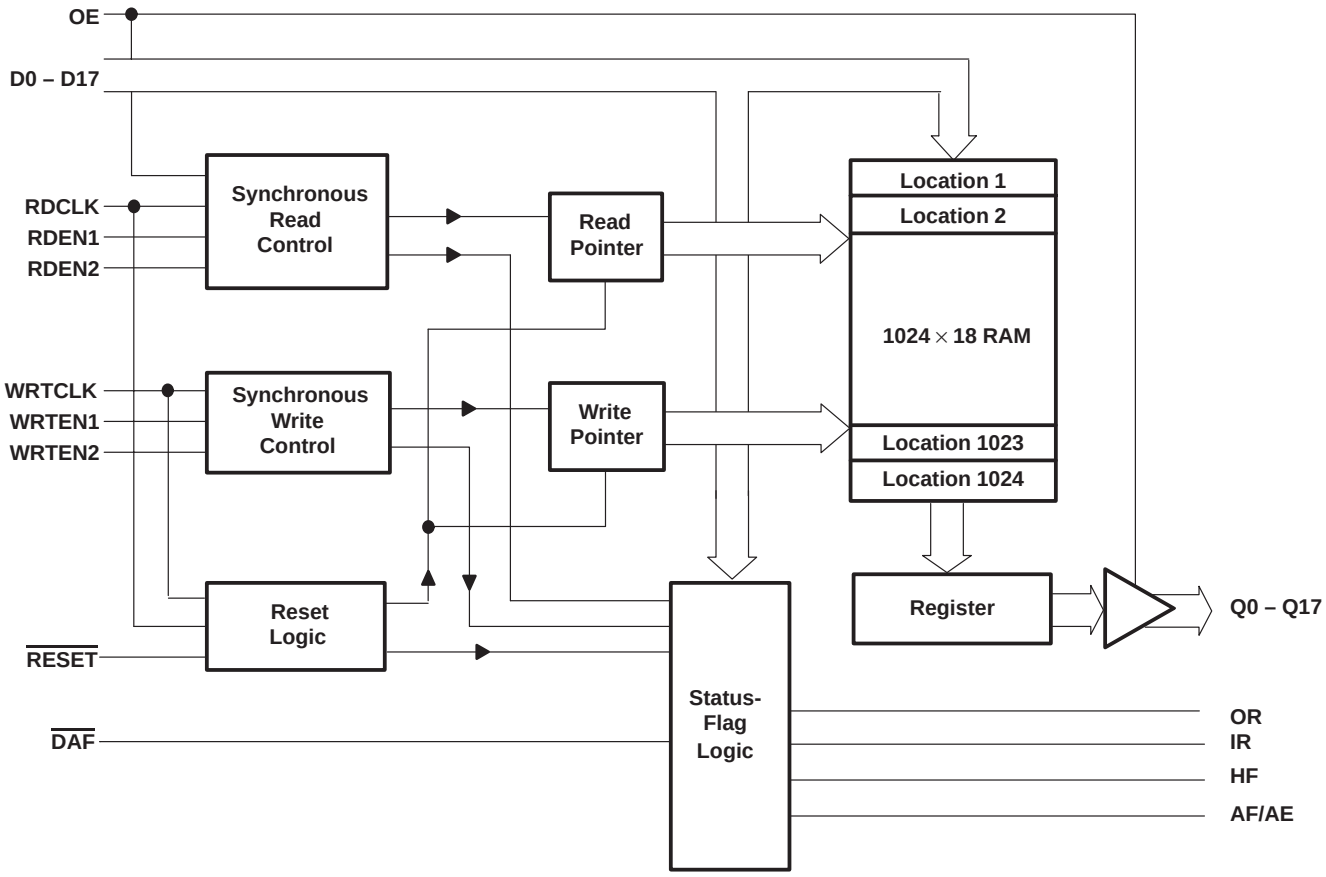
† The SN54ACT7811 HV is not production released.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the GB package.

functional block diagram



Terminal Functions

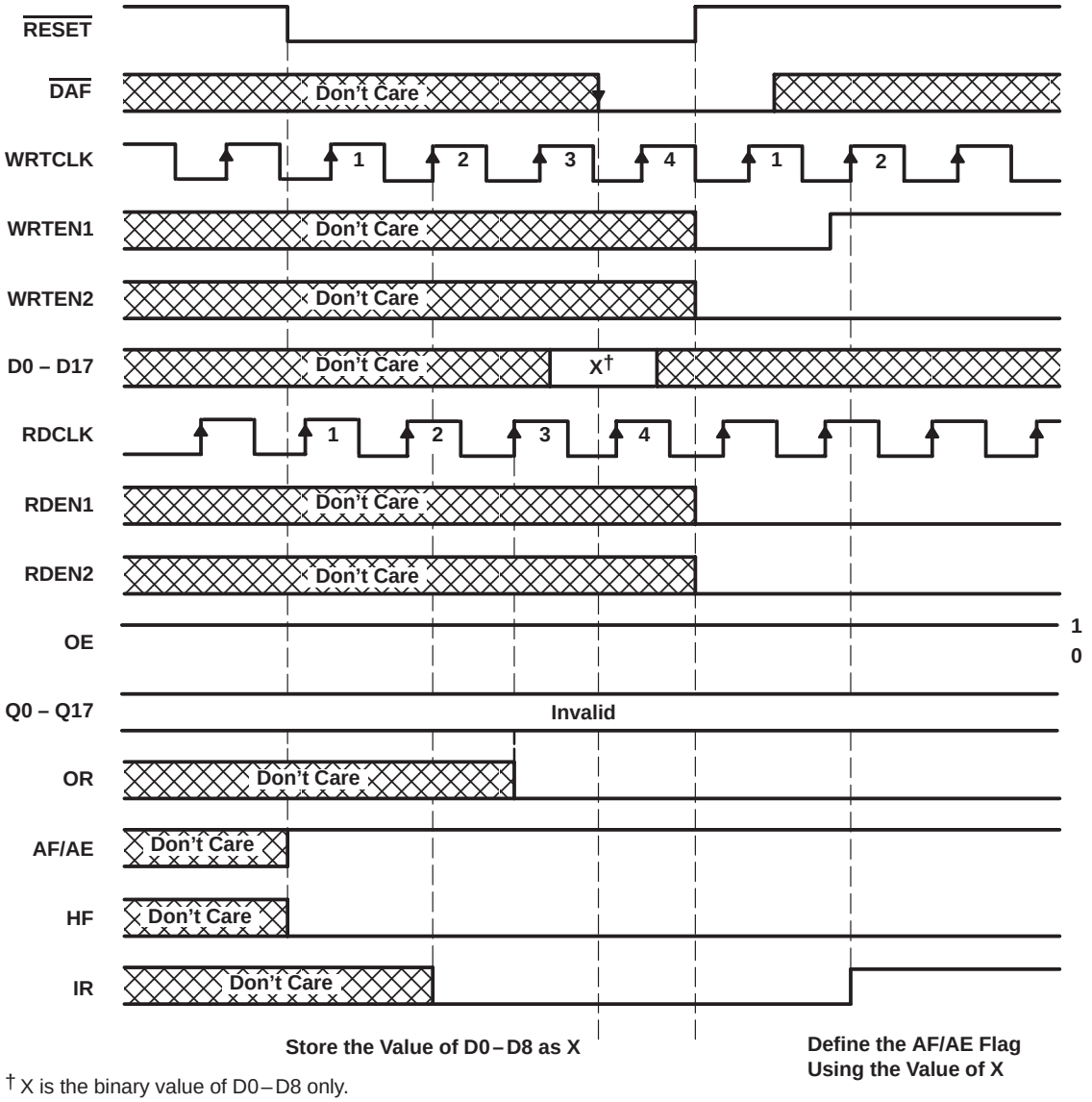
TERMINAL† NAME	TERMINAL† NO.	I/O	DESCRIPTION
AF/AE	F9	O	AF/AE boundary is defined by the AF/AE offset value (X). This value can be programmed during reset, or the default value of 256 can be used. The AF/AE flag is high when the FIFO contains (X + 1) or fewer words or (1025 – X) or more words. The AF/AE flag is low when the FIFO contains between (X + 2) and (1024 - X) words. Programming procedure for AF/AE – The AF/AE flag is programmed during each reset cycle. The AF/AE offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{\text{DAF}}$ from high to low. Step 2: If the reset ($\overline{\text{RESET}}$) input is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE flag using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. Default X To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	H9	I	Define almost full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the AF/AE offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on the reset ($\overline{\text{RESET}}$) input defines the AF/AE flag using X.
D0–D17	F2, G1, G2, H1–H4, H6–H8, J1–J3, J5–J9	I	Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0–D8 also carry the AF/AE offset value (X) on a high-to-low transition of the $\overline{\text{DAF}}$ input.
HF	D9	O	Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or fewer words.
IR	E9	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second write clock (WRTCLK) pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	D1	I	Output enable. The data-out (Q0–Q17) outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of read clock (RDCLK) to read a word from memory.
OR	B1	O	Output ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third read clock (RDCLK) pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	A1–A9, B2, B3, B5, B7–B9, C2, C8, C9	O	Data outputs. The first data word to be loaded into the FIFO is moved to the data-out (Q0–Q17) register on the rising edge of the third read clock (RDCLK) pulse to occur after the first valid write. The read-enable (RDEN1, RDEN2) inputs do not affect this operation. The following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	F1	I	Read clock. Data is read out of memory on a low-to-high transition at RDCLK if the OR output and the OE, RDEN1, and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	E1 E2	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. The read enables are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	C1	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ input at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the AF/AE offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines AF/AE using the default value of X = 256.

† Terminals listed are for the GB package.

Terminal Functions (Continued)

TERMINAL† NAME	TERMINAL† NO.	I/O	DESCRIPTION
WRTCLK	G8	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if the IR output and the WRTEN1 and WRTEN2 control inputs are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR output is also driven synchronously with respect to the WRTCLK signal.
WRTEN1, WRTEN2	G9 F8	I	Write enables. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. The write enables do not affect the storage of the AF/AE offset value (X).

† Terminals listed are for the GB package.



† X is the binary value of D0 – D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X

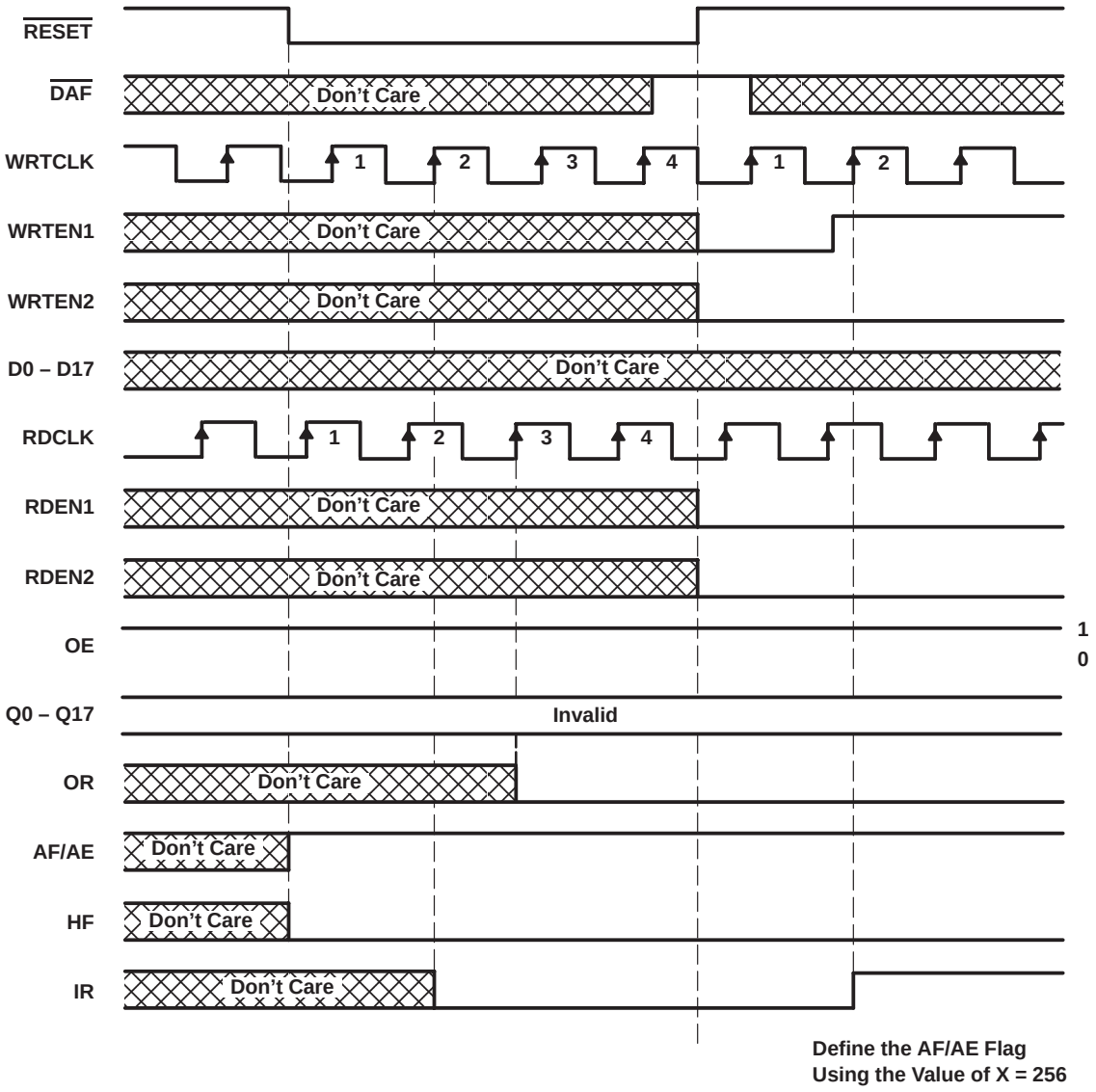


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

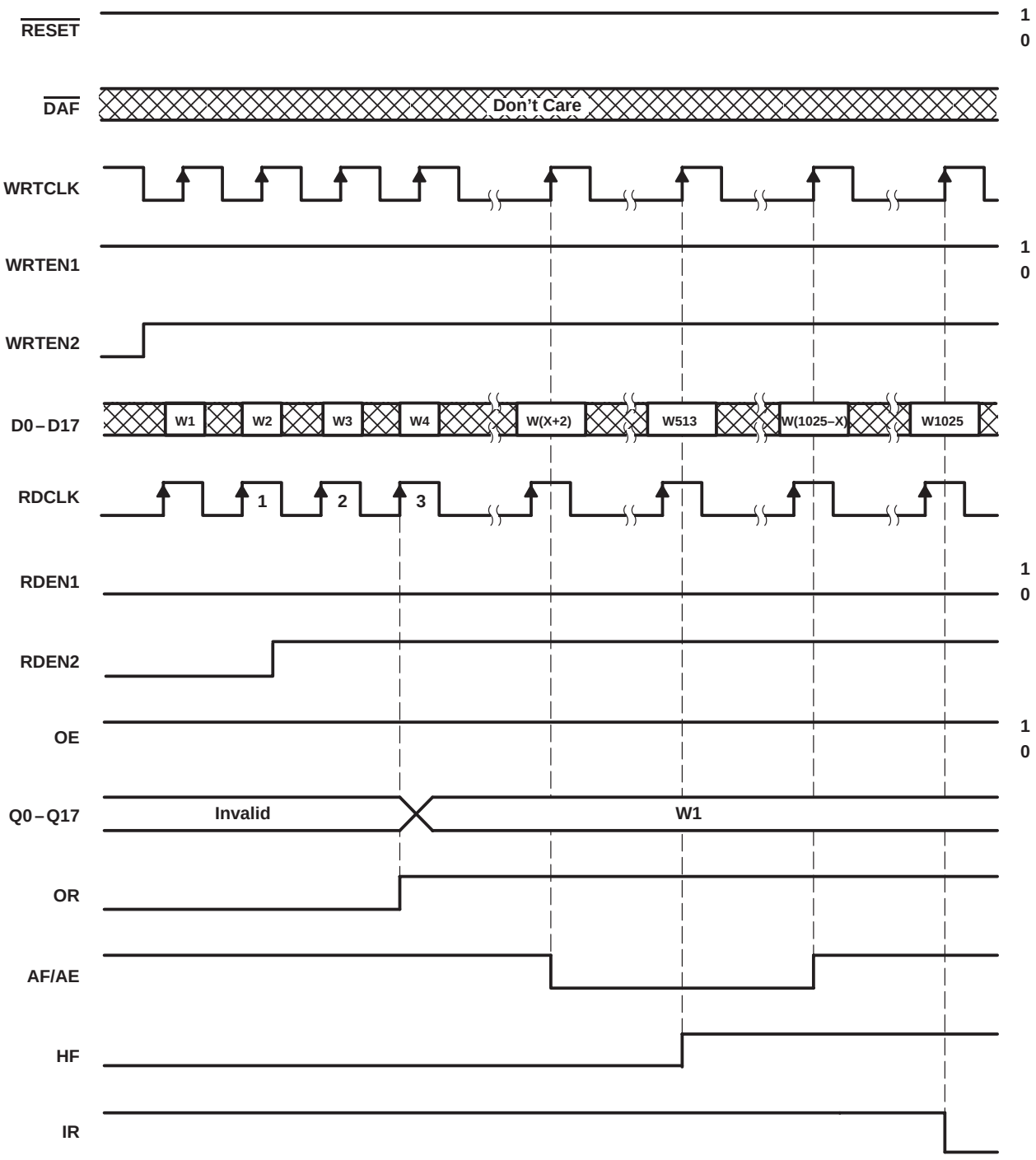


Figure 3. Write Cycle

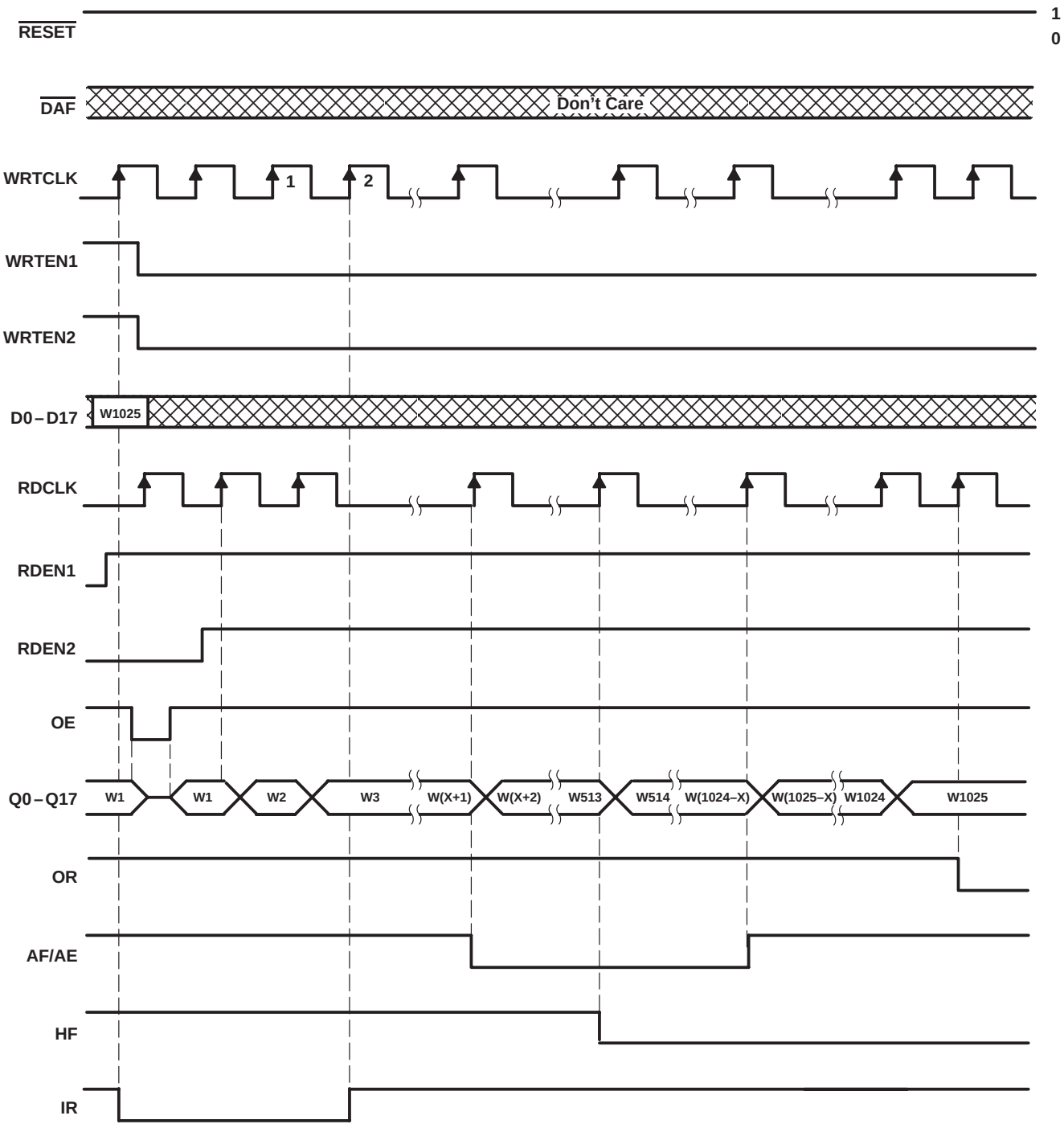


Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	–55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			±5	µA
I_{CC}§	V_I = V_{CC} – 0.2 V or 0 V				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0 V,	f = 1 MHz		4		pF
C_o	V_O = 0 V,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open

timing requirements (see Figures 1 through 8)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		28.5		MHz
t_w	Pulse duration	Data in (D0–D17) high or low	14		ns
		WRTCLK high	10		
		WRTCLK low	14		
		RDCLK high	10		
		RDCLK low	14		
		$\overline{DAF}$ high	10		
		WRTEN1, WRTEN2 high or low	10		
		OE, RDEN1, RDEN2 high or low	10		
t_{su}	Setup time	Data in (D0–D17) before WRTCLK↑	5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	5		
		OE, RDEN1, RDEN2 high before RDCLK↑	5		
		Reset: $\overline{RESET}$ low before first WRTCLK and RDCLK↑†	7		
		Define AF/AE: D0–D8 before $\overline{DAF}$↓	5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	5		
t_h	Hold time	Data in (D0–D17) after WRTCLK↑	1		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	1		
		OE, RDEN1, RDEN2 high after RDCLK↑	1		
		Reset: $\overline{RESET}$ low after fourth WRTCLK and RDCLK↑†	0		
		Define AF/AE: D0–D8 after $\overline{DAF}$↓	1		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = –55°C to 125°C		UNIT
			MIN	MAX	
f_{max}	WRTCLK or RDCLK		28.5		MHz
t_{pd}	RDCLK↑	Any Q	3	20	ns
t_{pd}†					
t_{pd}	WRTCLK↑	IR	1	14	ns
t_{pd}	RDCLK↑	OR	1	14	ns
t_{pd}	WRTCLK↑	AF/AE	5	24	ns
	RDCLK↑		5	24	
t_{PLH}	WRTCLK↑	HF	5	23	ns
t_{PHL}	RDCLK↑		5	23	
t_{PLH}	RESET↓	AF/AE	2	23	ns
t_{PHL}		HF	3	25	
t_{en}	OE	Any Q	1	11	ns
t_{dis}			1	14	

† This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

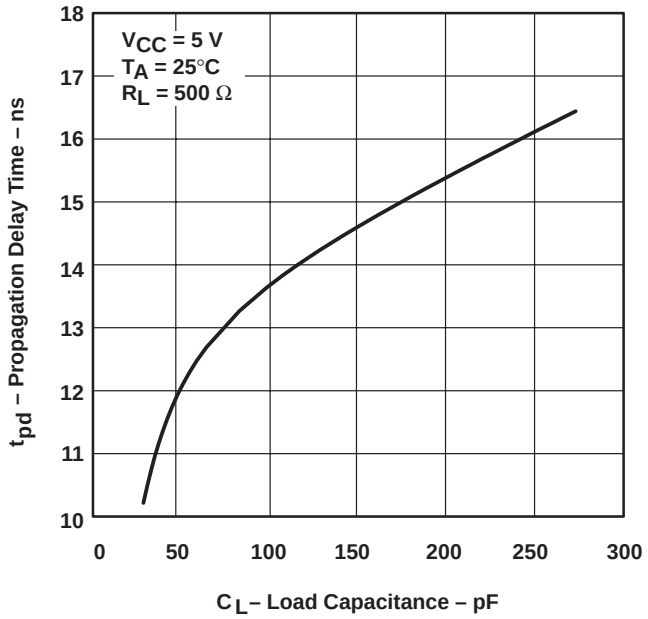


Figure 5

TYPICAL POWER DISSIPATION CAPACITANCE vs SUPPLY VOLTAGE

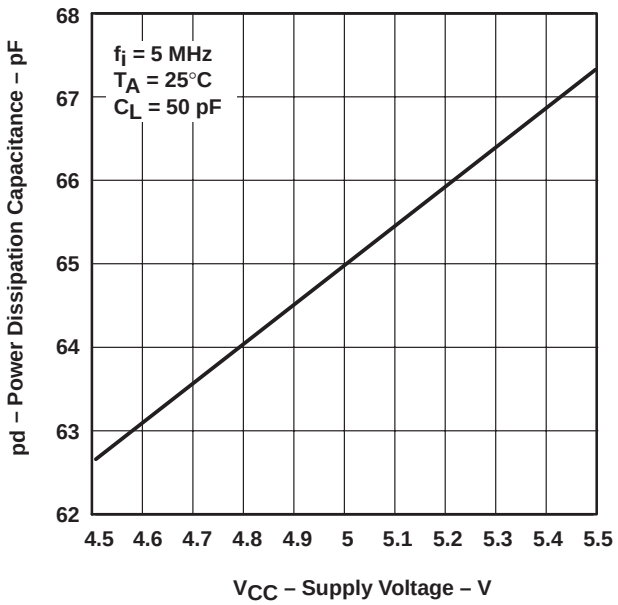


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN54ACT7811 can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

Where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

expanding the SN54ACT7811

The SN54ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

– After the first data word is loaded into the FIFO, the word is unloaded, and the OR output goes high after (N × 3) RDCLK cycles, where N is the number of devices used in depth expansion.

– After the FIFO is filled, the IR output goes low, the first word is unloaded, and the IR is driven high after (N × 2) write clock cycles, where N is the number of devices used in depth expansion.

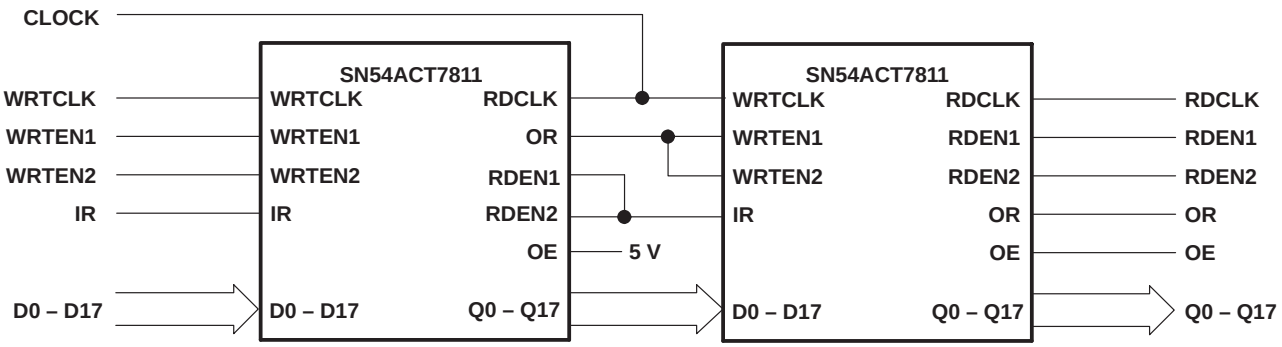


Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2

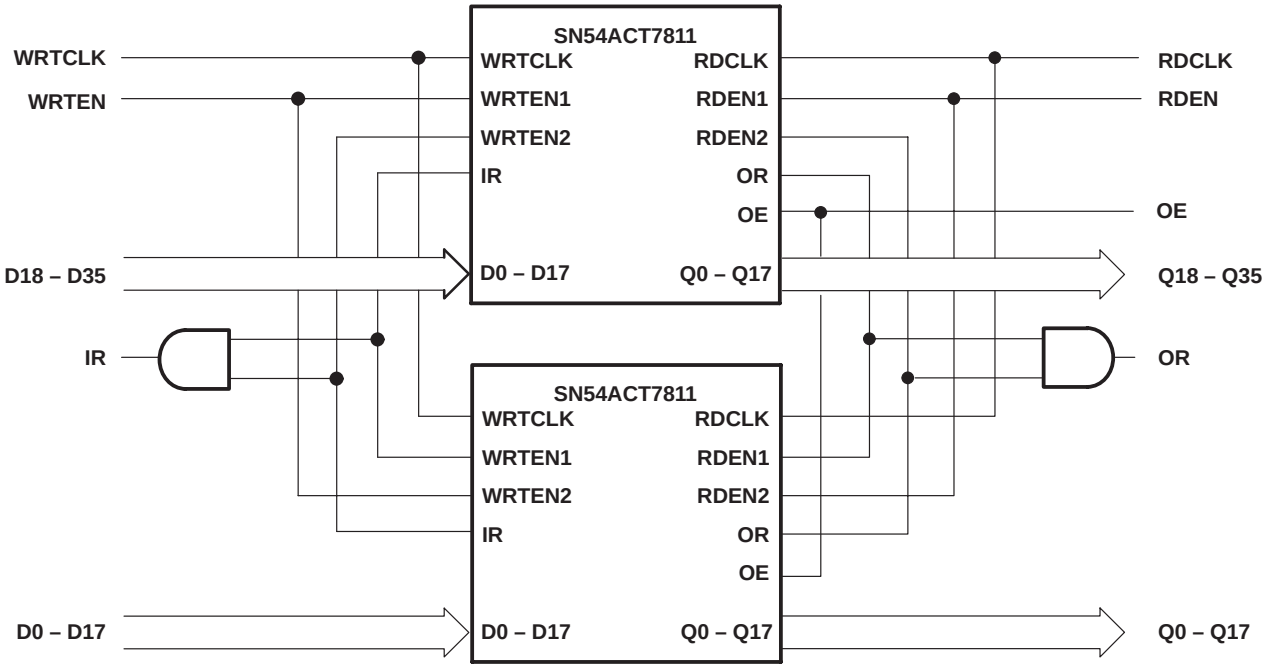


Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

PARAMETER MEASUREMENT INFORMATION

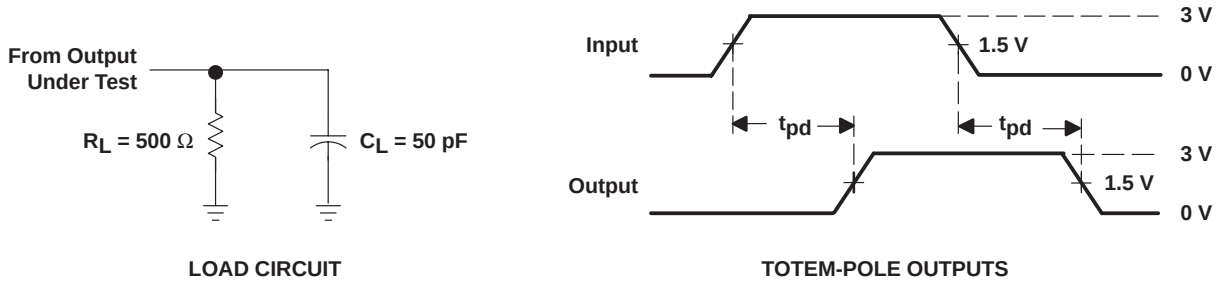
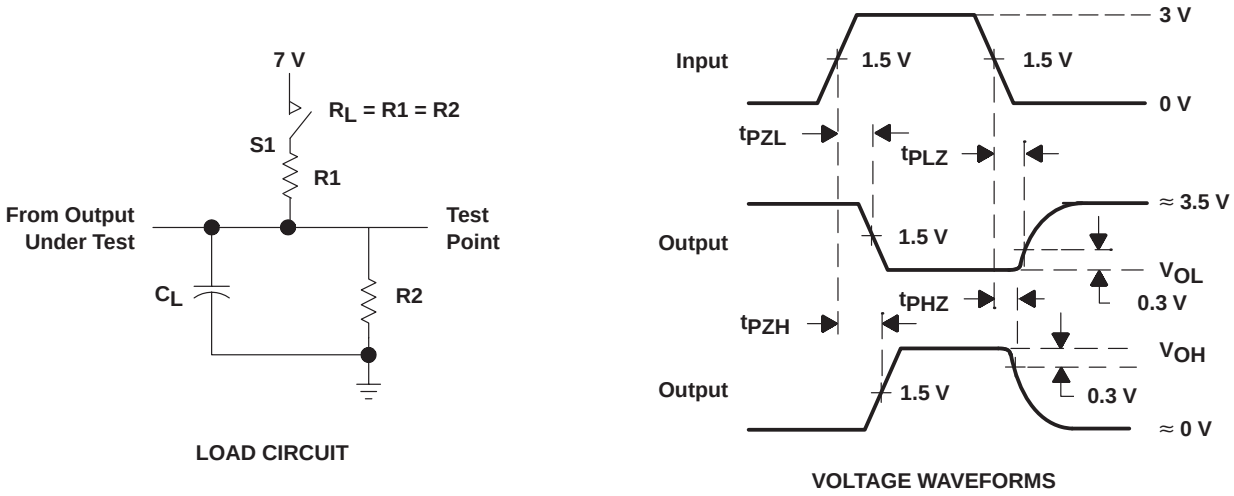


Figure 9. Standard CMOS Outputs



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs (Any Q)

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