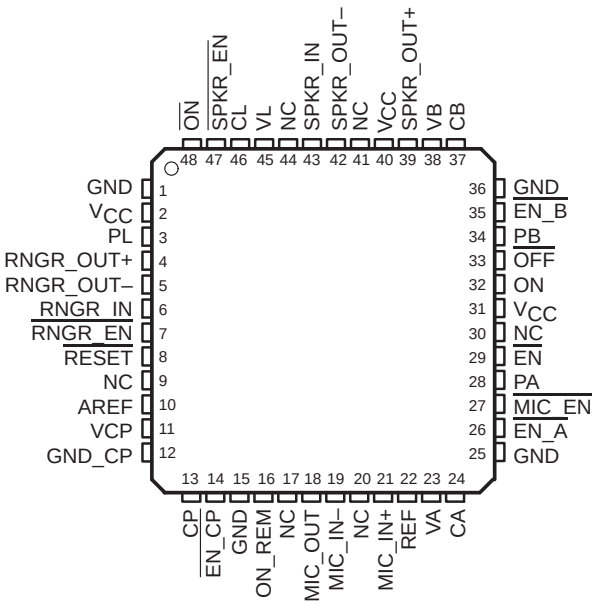
- **Complete Power-Supply/Audio System For Cellular Handsets**
- **Three Low-Dropout Regulators (LDOs) with 100-mV Dropout**
- **Speaker and Ringer Power Amplifiers Drive 32-Ω Dynamic Speakers or Piezo Devices**
- **Low-Noise Microphone Amplifier**
- **Depop Protection For All Amplifiers**
- **Less Than 1 μA Supply Current in Shutdown, Typical**
- **250-ms Microprocessor Reset Output**
- **10-mA Charge-Pump Driver Configurable For Inverted or Doubled Output**
- **Separate Enables for LDOs, Amplifiers, and Charge Pump**
- **1.185-V Reference Capable of Driving 2 mA**
- **48-Pin TQFP Package**

PT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS9104 incorporates a complete power supply and audio power system for a cellular subscriber terminal that uses battery packs with three or four NiMH/NiCd cells or a single lithium-ion cell. The device includes three low-dropout linear regulators rated for 3.3 V or 3 V at 100 mA each, a charge-pump driver, two power amplifiers for a speaker and a ringer, a low-noise microphone amplifier, and logic that includes a 250-ms reset, on/off control, and processor interface. Regulators A and B and the charge-pump driver are disabled until regulator L (logic regulator) reaches the rated voltage and $\overline{\text{RESET}}$ is logic high. Regulators A and B, the charge-pump driver, and the amplifiers have separate enables allowing circuitry to be powered up or down as necessary to conserve battery power.

Each of the amplifiers has a depop circuit to prevent objectionable noise when the IC is powered up or when the amplifiers are enabled. Both the speaker amplifier and the ringer amplifier are designed to supply 2 V peak-to-peak into 32 Ω or into a 90-nF piezoelectric speaker. The microphone amplifier is a low-noise high-gain (A_V=100) circuit capable of supplying 3 V peak-to-peak into a 10-kΩ load.

The TPS9104 operates over a free-air temperature range of –40°C to 85°C and is supplied in a 48-pin TQFP package.

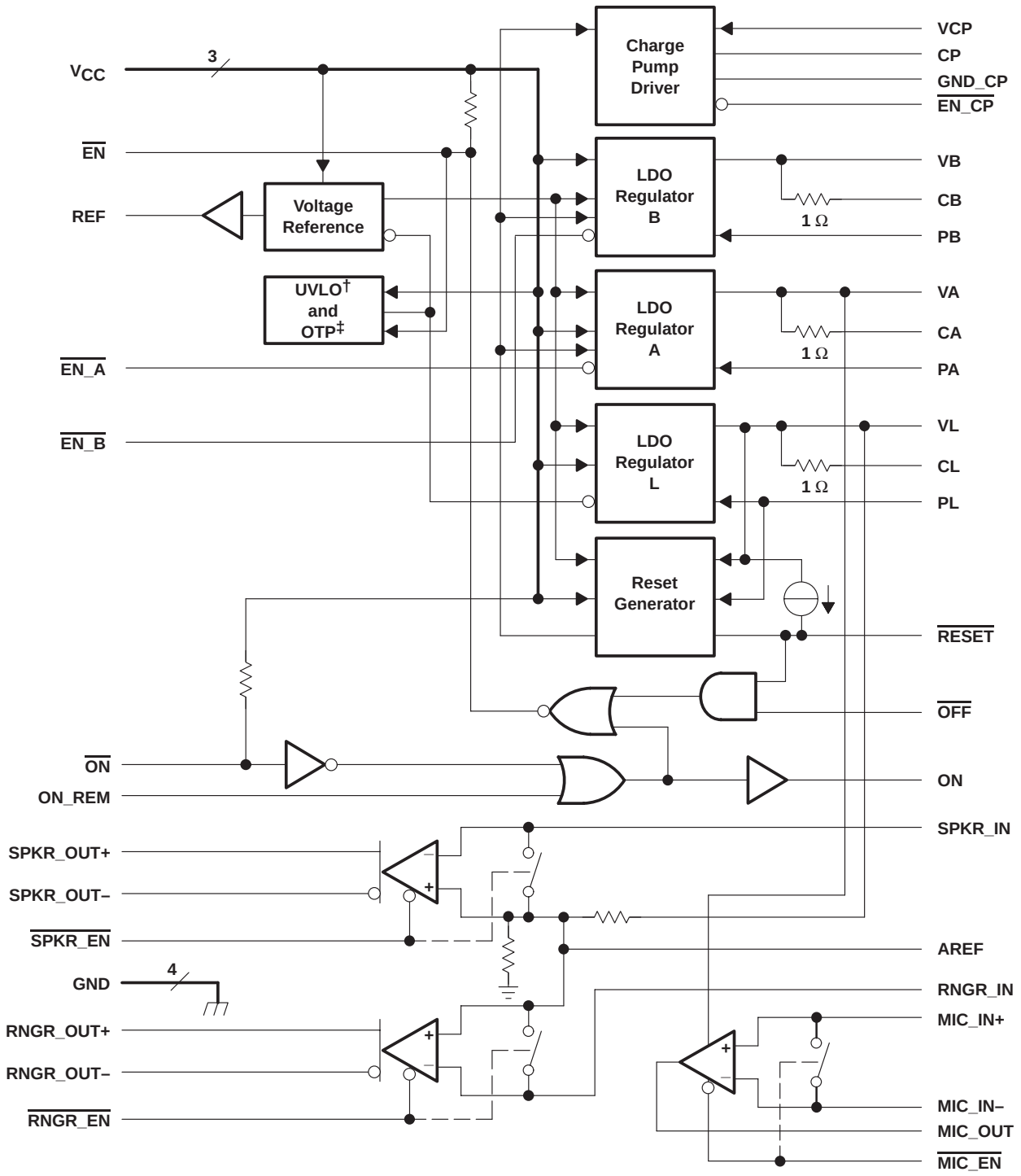
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM (Y)
	THIN QFP (PT)	
–40°C to 85°C	TPS9104IPT	TPS9104Y

The PT package is available taped and reeled. Add R suffix to the device type when ordering (e.g. TPS9104IPTR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram

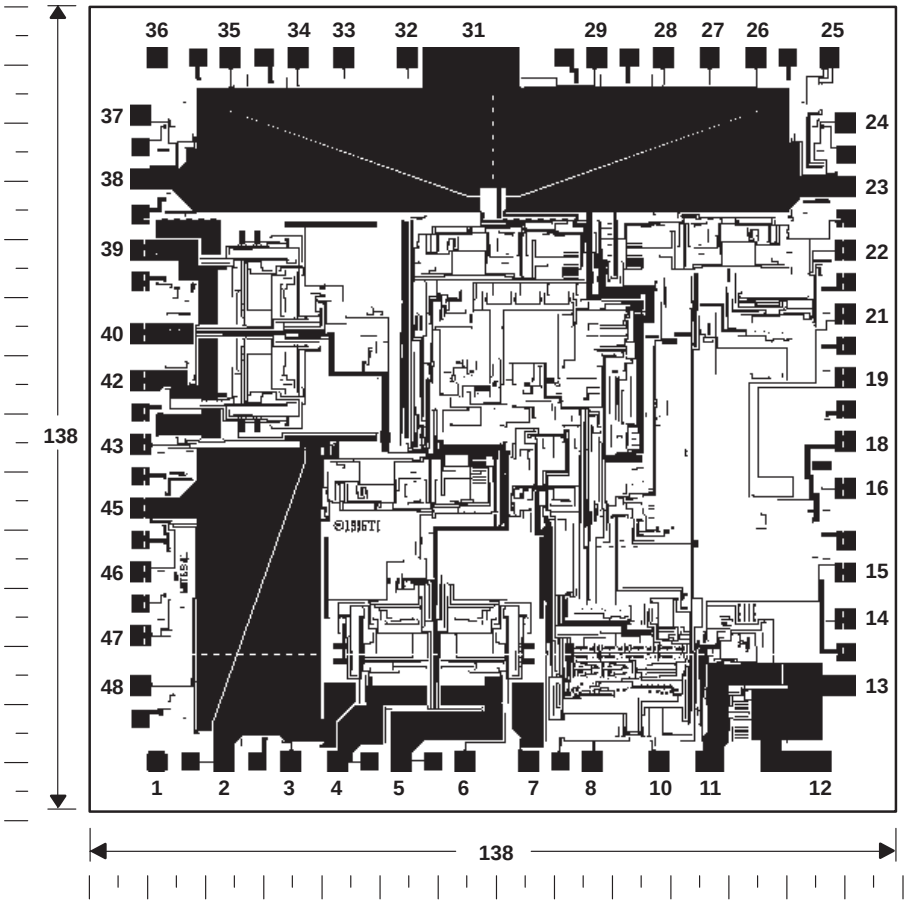


† UVLO - Undervoltage lockout
‡ OTP - Overtemperature protection

TPS9104Y chip information

These chips, when properly assembled, display characteristics similar to the TPS9104. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.3 × 3.3 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	1, 15, 25, 36		Ground. GND terminals should be externally connected to ground to ensure proper functionality.
V_{CC}	2, 31, 40		Supply voltage input. V_{CC} terminals are not connected internally and must be externally connected to ensure proper functionality.
PL	3	I	Program L. PL provides voltage programming input for regulator L.
RNGR_OUT+	4	O	Ringer amplifier noninverting output
RNGR_OUT–	5	O	Ringer amplifier inverting output
RNGR_IN	6	I	Ringer amplifier input
$\overline{\text{RNGR\_EN}}$	7	I	Ringer amplifier enable input; logic low enables the amplifier
$\overline{\text{RESET}}$	8	O	Microprocessor reset output
NC	9, 17, 20, 30 41, 44		No connection
AREF	10		Analog reference. A 0.1-μF capacitor must be connected from AREF to ground. No other connections are allowed.
VCP	11		Charge pump driver supply voltage
GND_CP	12		Charge pump driver ground
CP	13	O	Charge pump driver output
$\overline{\text{EN\_CP}}$	14	I	Charge pump driver enable input. Logic low on $\overline{\text{EN\_CP}}$ turns on the charge pump.
ON_REM	16	I	Remote on; logic high enables the part.
MIC_OUT	18	O	Microphone amplifier output
MIC_IN–	19	I	Microphone amplifier inverting input
MIC_IN+	21	I	Microphone amplifier noninverting input
REF	22	O	1.185-V reference output. Decouple with 0.01-μF to 0.1-μF capacitor to ground.
VA	23	O	Regulator A output voltage
CA	24		Regulator A filter capacitor connection
$\overline{\text{EN\_A}}$	26	I	Regulator A enable input; logic low turns on the regulator.
$\overline{\text{MIC\_EN}}$	27	I	Microphone amplifier enable input; logic low turns on the microphone amplifier.
PA	28	I	Program A. PA provides programming input for Regulator A.
$\overline{\text{EN}}$	29	I/O	Enable signal input/output; logic low enables the part.
ON	32	O	On-signal output
$\overline{\text{OFF}}$	33	I	Off signal
PB	34	I	Program B. PB provides programming input for Regulator B.
$\overline{\text{EN\_B}}$	35	I	Regulator B enable input; logic low turns on the regulator.
CB	37		Regulator B filter capacitor connection
VB	38	O	Regulator B output voltage
SPKR_OUT+	39	O	Speaker amplifier noninverting output
SPKR_OUT–	42	O	Speaker amplifier inverting output
SPKR_IN	43	I	Speaker amplifier input
VL	45	O	Regulator L output voltage
CL	46		Regulator L filter capacitor connection
$\overline{\text{SPKR\_EN}}$	47	I	Speaker amplifier enable input; logic low enables the amplifier.
$\overline{\text{ON}}$	48	I	On signal; logic low enables the part.

detailed description

voltage reference

The regulators and reset generator utilize an internal 1.185-V band-gap voltage reference. The reference is also buffered and brought out on REF for external use; REF can source a maximum of 2 mA. A 0.01-µF to 0.1-µF capacitor must be connected between REF and ground.

LDO regulators

The TPS 9104 includes three low-dropout regulators, implemented with 1-Ω PMOS series-pass transistors, with quiescent supply currents of 100 µA. Each of the regulators can supply up to 100 mA of continuous output current. The 1-Ω PMOS series-pass transistor achieves the dropout voltage of just 100 mV at the maximum rated output current. Each regulator output voltage can be independently programmed to either 3.3 V or 3 V using its programming control input PL, PA or PB (Px). A logic low on Px sets the output voltage of the regulator to 3.3 V; a logic high sets it to 3 V.

Each LDO contains a current limit circuit. When the current demand on the regulator exceeds the current limit, the output voltage drops in proportion to the excess current. When the excess load current is removed, the output voltage returns to regulation. Exceeding the current limit on VL can disable the TPS9104. If enough current demand is placed on VL, the output voltage drops below the reset threshold voltage causing $\overline{\text{RESET}}$ to go low, effectively unlatching the enable.

VL is intended to be the primary supply voltage for the microprocessor and other system logic functions. VA and VB can be used to power low-noise analog circuits and/or implement system power management. The enable terminals $\overline{\text{EN\_A}}$ and $\overline{\text{EN\_B}}$ are utilized to power down circuitry when it is not required. $\overline{\text{EN\_A}}$ and $\overline{\text{EN\_B}}$ are TTL-compatible inputs with 10-µA active current-source pullups. A logic low enables the respective regulator while a logic high pulls the regulator output voltage to ground and reduces the regulator quiescent current to leakage levels. Both $\overline{\text{EN\_A}}$ and $\overline{\text{EN\_B}}$ are not active until $\overline{\text{RESET}}$ is logic high.

Stability of the LDOs is ensured by the addition of compensation terminals CL, CA, and CB, which connect to the output of the regulator through an internal 1-Ω resistor. This compensation scheme allows for capacitors with equivalent series resistance (ESR) of up to 15 Ω, eliminating the need for expensive, low-ESR capacitors.

reset generator

$\overline{\text{RESET}}$ is a microprocessor reset signal that goes to logic low at power-up, or whenever VL drops below 2.93 V (2.6 V for 3-V applications), and remains in that state for 250 ms after VL exceeds the $\overline{\text{RESET}}$ threshold (see Figure 5). The open-drain output has a 30-µA pullup that eliminates the need for an external pullup resistor and still allows it to be connected with other open-drain or open-collector signals. $\overline{\text{RESET}}$ is valid for supply voltages as low as 1.5 V.

$\overline{\text{ON}}$, $\overline{\text{OFF}}$, ON, ON_REM and $\overline{\text{EN}}$ functions

The $\overline{\text{ON}}$ input is intended to be the main enable for the TPS9104 and should be connected to ground through a push-button switch. Once the switch is pressed, internal logic pulls $\overline{\text{EN}}$ low. The $\overline{\text{EN}}$ terminal is designed to sink 3.2 mA and can be used as a pulldown to enable other functions on the TPS9104 or other system circuitry. When $\overline{\text{EN}}$ is pulled low, the TPS9104 checks to make sure the supply voltage is above the UVLO threshold voltage and the die temperature is below 160°C. If both of these conditions are met, the reference circuitry, regulator L, reset generator, and other support circuitry are enabled. When $\overline{\text{RESET}}$ goes high, the system can respond with a logic high on $\overline{\text{OFF}}$, which latches the TPS9104 on, and the $\overline{\text{ON}}$ push button can then be released.

The TPS9104 is disabled in a similar manner. If the $\overline{\text{ON}}$ push button is pressed while the TPS9104 is enabled, the ON signal responds with a logic high. Once this logic high is detected, the system can respond with a logic low on $\overline{\text{OFF}}$, disabling the TPS9104 and reducing supply currents to 1 µA (see Figure 1).

The ON_REM signal can be used in the same manner as $\overline{ON}$ in enabling or disabling the TPS9104. The signal is provided as a system interface to increase the flexibility of the system. $\overline{EN}$ can also be used as an input wired-OR open collector/drain to enable the TPS9104; however, it does not produce a logic signal ON and therefore cannot be used in the disable sequence described above. It is not recommended that $\overline{EN}$ be used as the primary enable signal for the TPS9104.

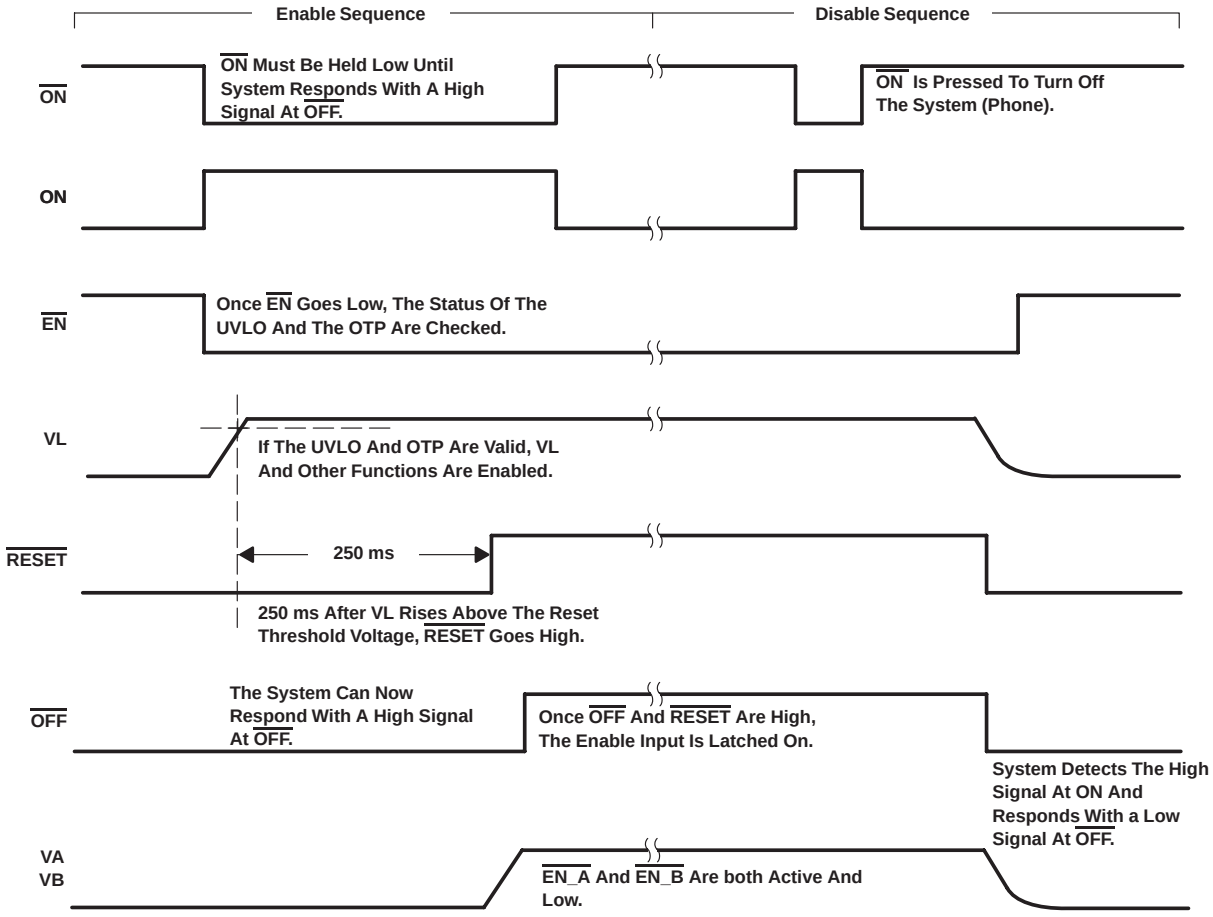


Figure 1. Recommended Enable and Disable Sequence

speaker/ringer power amplifiers

The TPS9104 includes two differential-output power amplifiers capable of driving dynamic or piezoelectric speakers. Both amplifiers have enable inputs to reduce supply current to leakage levels when the amplifiers are not in use. Depopping circuitry prevents objectionable noise when the enable inputs are cycled on or off. Each amplifier requires only two gain-setting resistors and a capacitor for dc blocking (see Figure 46). $\overline{RNGR\_EN}$ and $\overline{SPKR\_EN}$ inputs are disabled when $\overline{RESET}$ is asserted. Both the $\overline{SPKR\_EN}$ and the $\overline{RNGR\_EN}$ have internal 10-µA pullups.

microphone amplifier

This is a high-gain amplifier capable of driving a 10-kΩ load at 3 V peak-to-peak output. $\overline{MIC\_EN}$ input is disabled when $\overline{RESET}$ is asserted. The microphone amplifier has an enable input that reduces supply current to leakage levels when disabled. Added depopping circuitry prevents objectionable noise when the enable input

is cycled on or off. The microphone amplifier needs only two resistors to set the gain, and one capacitor for dc blocking (see Figure 47). Regulator A is the analog supply for the microphone amplifier, and $\overline{\text{EN\_A}}$ must be asserted for correct operation.

undervoltage lockout

Undervoltage lockout (UVLO) prevents operation of the functions in the TPS9104 until the supply voltage exceeds the threshold voltage, eliminating abnormal power-up conditions internally and externally, and providing an orderly turn-on.

overtemperature shutdown

If the die temperature exceeds 160°C, the thermal protection circuit shuts off the TPS9104. When the die temperature drops below 150°C, the device can be restarted with the $\overline{\text{ON}}$ input.

charge pump driver

An unregulated inverting or doubler charge pump is implemented (see Figure 44) by connecting a network of two capacitors and two diodes to CP. In the inverting configuration, the charge pump can power an LCD or provide gate bias for a GaAs power amplifier. A 5-V supply for flash-memory programming or powering the subscriber identity module (SIM) European applications can be achieved using the doubler configuration and an external LDO. A logic-low input to the charge-pump enable, $\overline{\text{EN\_CP}}$, turns on the oscillator and driver; a logic high turns them off. $\overline{\text{EN\_CP}}$ input is disabled when $\overline{\text{RESET}}$ is asserted. The $\overline{\text{EN\_CP}}$ has a 10-µA internal pullup.

DISSIPATION RATING TABLE 1 – Free-Air Temperature

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PT	1350 mW	10.8 mW/°C	864 mW	702 mW

DISSIPATION RATING TABLE 2 – Case Temperature

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PT	6579 mW	52.6 mW/°C	4212 mW	3423 mW

MAXIMUM CONTINUOUS POWER DISSIPATION vs FREE-AIR TEMPERATURE

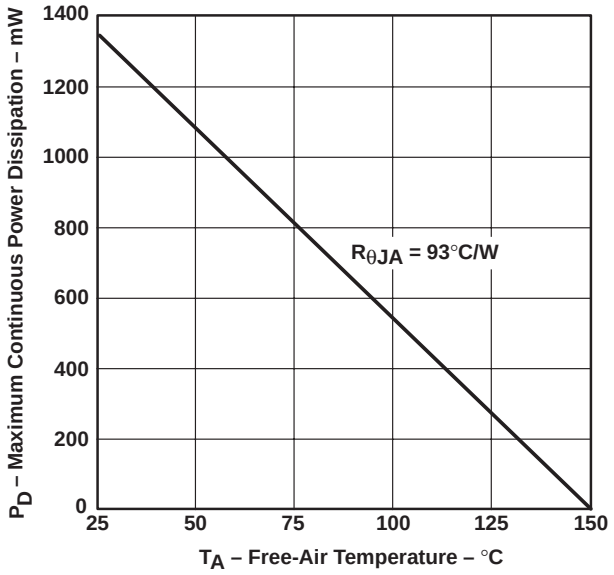


Figure 2

MAXIMUM CONTINUOUS POWER DISSIPATION vs CASE TEMPERATURE

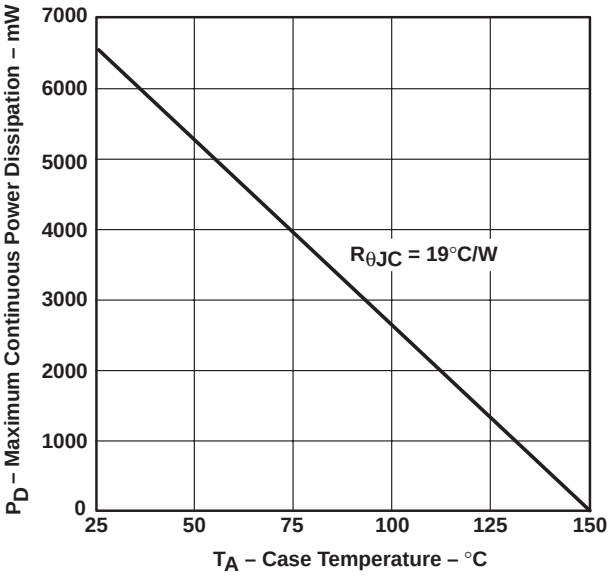


Figure 3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply voltage range, V_{CC}, VCP . . . . . –0.3 V to 12 V
Input voltage range at $\overline{OFF}$, $\overline{MIC\_EN}$, $\overline{SPKR\_EN}$, $\overline{RNGR\_EN}$, SPKR_IN, RNGR_IN, MIC_IN+, MIC_IN– . . . . . –0.3 V to 7 V
Input voltage range at PL, PA, PB, $\overline{EN}$, $\overline{EN\_A}$, $\overline{EN\_B}$, $\overline{ON}$, ON_REM, $\overline{EN\_CP}$ . . . . . –0.3 V to V_{CC}
Continuous total power dissipation . . . . . See dissipation rating table
Peak output current . . . . . Internally limited
Output current range at SPKR_OUT+, SPKR_OUT–, RNGR_OUT+, RNGR_OUT– . . . . . –100 mA to 100 mA
Power dissipation . . . . . See dissipation rating table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead Temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}, VCP	3		10	V
Input voltage, $\overline{OFF}$, $\overline{MIC\_EN}$, $\overline{SPKR\_EN}$, $\overline{RNGR\_EN}$	0		5	V
Input voltage at PL, PA, PB, $\overline{EN}$, $\overline{EN\_A}$, $\overline{EN\_B}$, $\overline{ON}$, ON_REM, $\overline{EN\_CP}$	0		V_{CC}	V
Reference output current	0		2	mA
Continuous regulator output current	0		100	mA
Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 μF (unless otherwise noted)

voltage reference (REF)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	T_A = 25°C,	I_O = 0		1.185		V
	4 V ≤ V_{CC} ≤ 10 V,	0 ≤ I_O ≤ 2 mA	1.161		1.209	V

LDO regulators

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage at VA, VB, VL (Vx)	T_A = 25°C		3.25	3.3	3.35	V
	0 ≤ $I_{O(Vx)}$ ≤ 100 mA,	3.5 V ≤ V_{CC} ≤ 10 V	3.2		3.4	V
	Px = V_{CC},	T_A = 25°C	2.95	3	3.05	V
	Px = V_{CC}, 3.2 V ≤ V_{CC} ≤ 10 V	0 ≤ $I_{O(Vx)}$ ≤ 100 mA,	2.9		3.10	V
Dropout voltage	$I_{O(Vx)}$ = 100 mA,	V_{CC} = 3.2 V		100	200	mV
Load regulation	$I_{O(Vx)}$ = 0 mA to 100 mA			30		mV
Line regulation	$I_{O(Vx)}$ = 100 mA,	V_{CC} = 3.5 V to 10 V		10		mV
Ripple rejection	f = 120 Hz			60		dB
Quiescent current (each regulator)				100		μA

charge pump driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency		50	100	150	kHz
Duty cycle			50%		
Output resistance			15	30	Ω

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 μF (unless otherwise noted) (continued)

speaker amplifier/ringer amplifier

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage swing	Single-ended,	R_L = 32 Ω	1.6	2		V
Output offset voltage	A_V = 1 V/V			15	30	mV
Total harmonic distortion (THD)	$V_{I(PP)}$ = 1 V, A_V = 1 V/V,	f = 1 kHz, R_L = 32 Ω		0.5%	1%	
Gain bandwidth product (GBW)	A_V = 10 V/V		4	20		kHz
Input noise	100 Hz ≤ BW ≤ 100 kHz			200		μVrms
Quiescent current (each amplifier)				2		mA
Reference voltage, AREF	PL = V_{CC}			1.221		V
	PL = 0 V			1.345		

microphone amplifier

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Common mode input voltage range			1		VA –1	V
Input bias current	Both inputs = VA/2		–1		1	μA
Output voltage swing	10 kΩ load,	VA = 3.3 V	2.7	3		V
Output offset voltage	A_V = 1 V/V				6	mV
Total harmonic distortion (THD)	f = 1 kHz, Output voltage swing = 1 V, $V_{O(PP)}$	A_V = 100 V/V,		0.5%	1%	
Power-supply rejection ratio (PSRR)	A_V = 100 V/V			100		dB
Common-mode rejection ratio (CMRR)	A_V = 100 V/V			80		dB
Gain bandwidth product (GBW)	A_V = 100 V/V		4			kHz
Input noise	100 Hz ≤ BW ≤ 100 kHz			10		μVrms
Quiescent current				180		μA

$\overline{RESET}$

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Input threshold voltage	VL voltage decreasing		2.871	2.93	2.989	V
Input threshold voltage	VL voltage decreasing,	PL = V_{CC}	2.548	2.6	2.652	V
Timeout delay at $\overline{RESET}$	See Figure 5		125	250	375	ms
Low-level output voltage	I_O = 1 mA,	V_{CC} = 1.5 V			0.4	V
High-level output current	V_O = 2.4 V		–40		–20	μA
Low-level output current	V_O = 0.4 V				3.2	mA
Hysteresis				40		mV

logic inputs at $\overline{EN\_A}$, $\overline{EN\_B}$, $\overline{SPKR\_EN}$, $\overline{RNGR\_EN}$, $\overline{MIC\_EN}$, $\overline{EN\_CP}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2			V
Low-level input voltage				0.8	V
Input current		–20	–10	1	μA

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 μF (unless otherwise noted) (continued)

logic inputs at PL, PA, PB, $\overline{OFF}$, ON_REM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2			V
Low-level input voltage				0.8	V
Input current		–1		1	μA

logic inputs at $\overline{ON}$†

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2			V
Low-level input voltage				0.8	V
Input current		–20		1	μA

logic inputs at $\overline{EN}$†

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
Source current	V_O = 2.4 V $\overline{OFF}$ = 0	–50	–30	1	μA
Sink current	V_O = 0.4 V			3.2	mA

logic outputs at ON

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	1-mA source current	2.4			V
Low-level output voltage	1-mA sink current			0.4	V

overtemperature shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature threshold			160		°C
Temperature hysteresis			10		°C

undervoltage lockout (UVLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Threshold	V_{CC} increasing	1.80		2.52	V
Hysteresis			50		mV

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown	$\overline{OFF}$ = 0 V		0.5	10	μA
Operating	$\overline{EN\_CP}$ = VCP, $\overline{SPKR\_EN}$ = VL, $\overline{RNGR\_EN}$ = VL, $\overline{MIC\_EN}$ = VL		0.7	1	mA

† High and low level voltages are dependent on V_{CC}. See graphs.

TPS9104Y electrical characteristics, T_J = 25°C, V_{CC} = VCP = 4 V, Px = 0 V, $I_{O(Vx)}$ = 35 mA, $\overline{OFF}$ = VL, $\overline{ON}$ open, ON_REM = 0 V, Cx = 10 µF (unless otherwise noted)

voltage reference (REF)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage	I_O = 0		1.185		V

LDO Regulators

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage at VA, VB, VL (Vx)	$P_X = V_{CC}$	2.95	3	3.05	V
Dropout voltage	$I_{O(Vx)}$ = 100 mA, V_{CC} = 3.2 V		100		mV
Load regulation	$I_{O(Vx)}$ = 0 mA to 100 mA		30		mV
Line regulation	$I_{O(Vx)}$ = 100 mA, V_{CC} = 3.5 V to 10 V		10		mV
Ripple rejection	f = 120 Hz		60		dB
Quiescent current (each regulator)			100		µA

charge pump driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			100		kHz
Duty cycle			50%		
Output resistance			15		Ω

speaker amplifier/ringer amplifier

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage swing	Single-ended, R_L = 32 Ω		2		V
Output offset voltage	A_V = 1 V/V		15		mV
Total harmonic distortion (THD)	$V_{I(PP)}$ = 1 V, f = 1 kHz, A_V = 1 V/V, R_L = 32 Ω		0.5%		
Gain bandwidth product (GBW)	A_V = 10 V/V		20		kHz
Input noise	100 Hz ≤ BW ≤ 100 kHz		200		µVrms
Quiescent current (each amplifier)			2		mA
Reference, AREF	PL = V_{CC}		1.221		V
	PL = 0 V		1.345		

microphone amplifier

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Common mode input range		1		VA –1	V
Output voltage swing	10 kΩ load, VA = 3.3 V	2.7	3		V
Output offset voltage	A_V = 1 V/V			6	mV

$\overline{RESET}$

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Threshold voltage	VL voltage decreasing		2.93		V
Threshold voltage	VL voltage decreasing, PL = V_{CC}		2.6		V
Delay	See Figure 5		250		ms
Hysteresis			40		mV

† Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effect must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

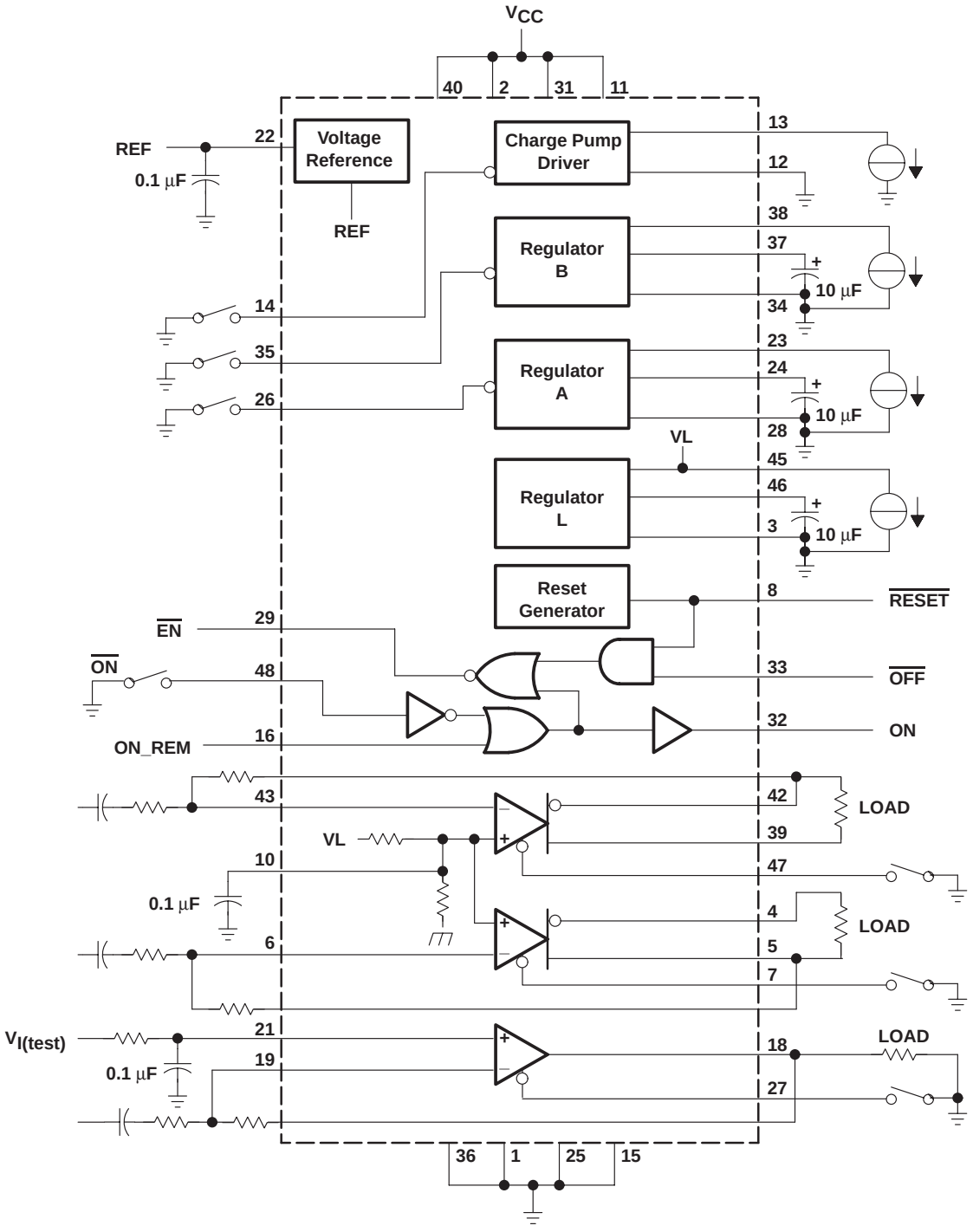


Figure 4. Test Circuit

PARAMETER MEASUREMENT INFORMATION

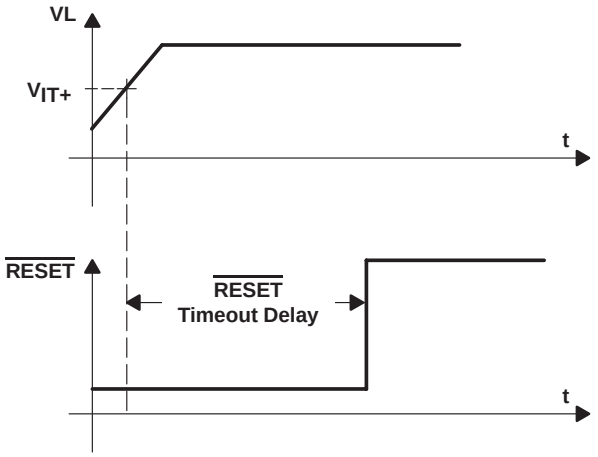


Figure 5. $\overline{\text{RESET}}$ Timing Diagram

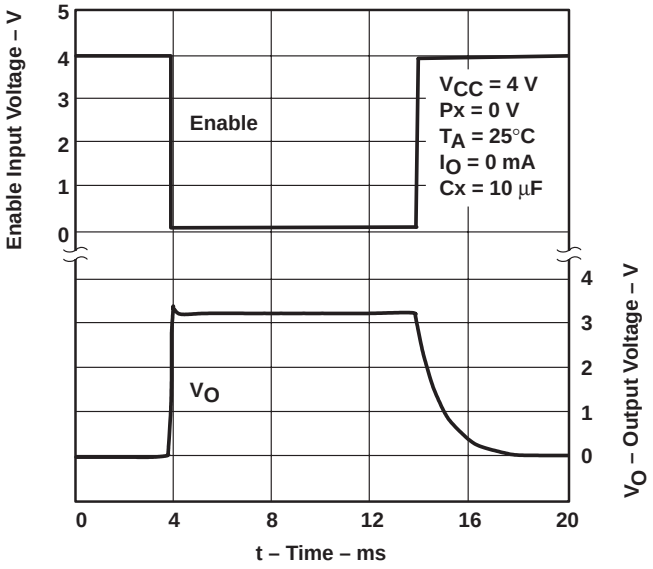


Figure 6. LDO Regulator Output Voltage Rise Time and Fall Time

PARAMETER MEASUREMENT INFORMATION

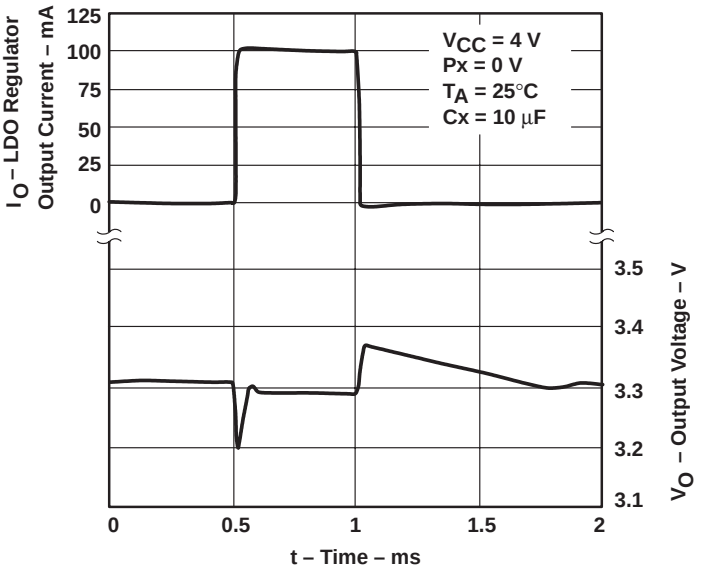


Figure 7. LDO Regulator Load Transient, 1 mA to 100 mA Pulsed Load

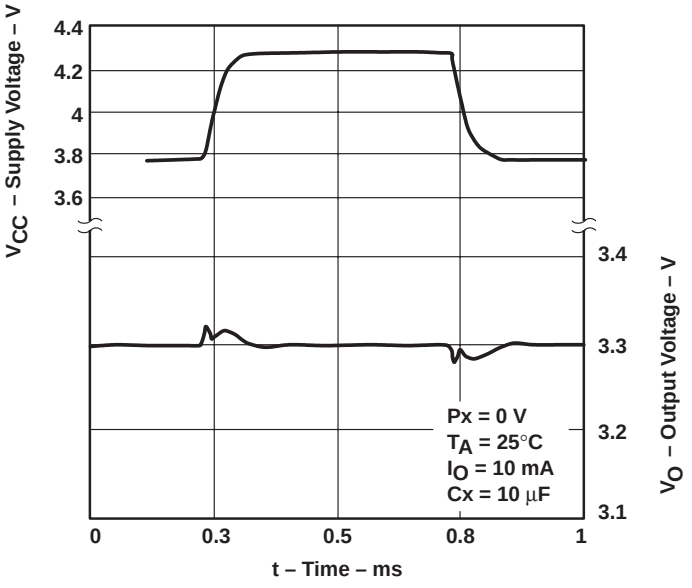


Figure 8. LDO Regulator Line Transient

PARAMETER MEASUREMENT INFORMATION

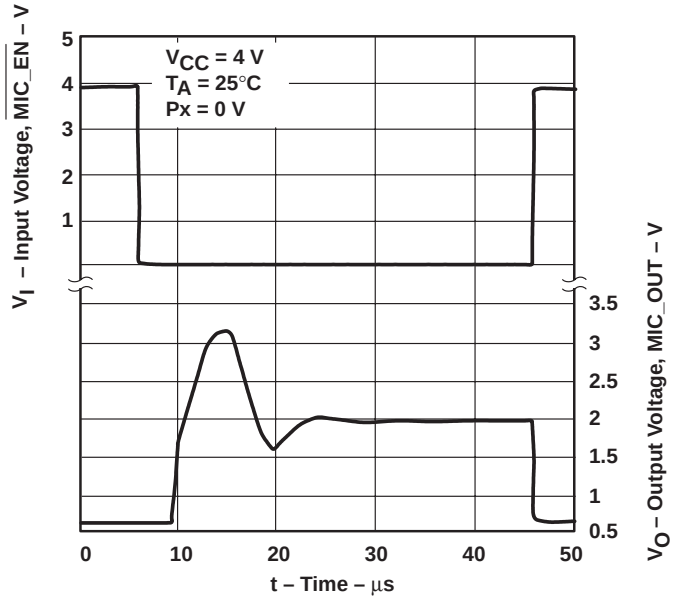


Figure 9. Microphone Enable Output Response

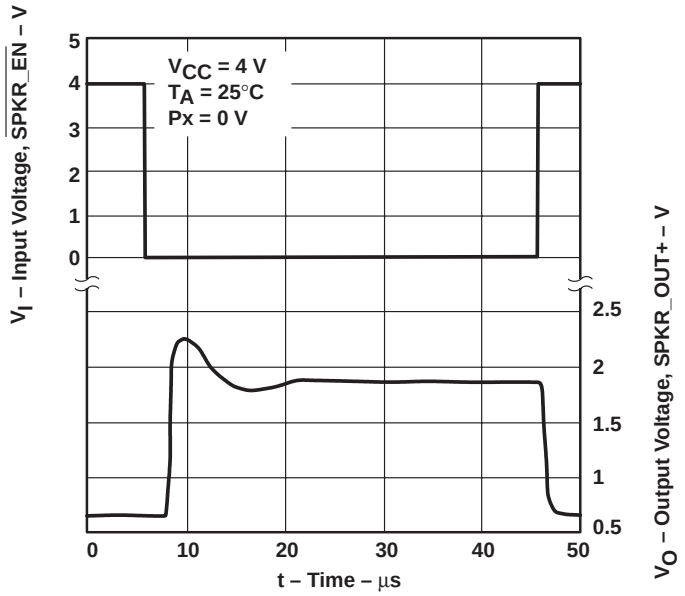


Figure 10. Speaker Enable Output Response

PARAMETER MEASUREMENT INFORMATION

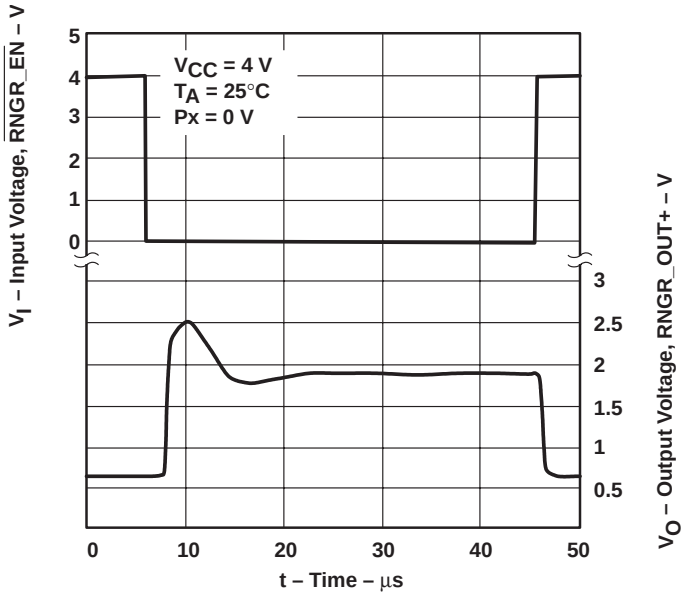


Figure 11. Ringer Enable Output Response

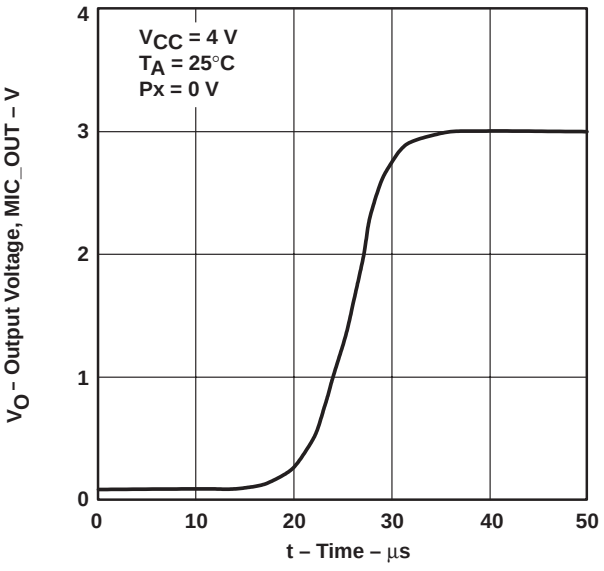


Figure 12. Microphone Slew Rate, Rising

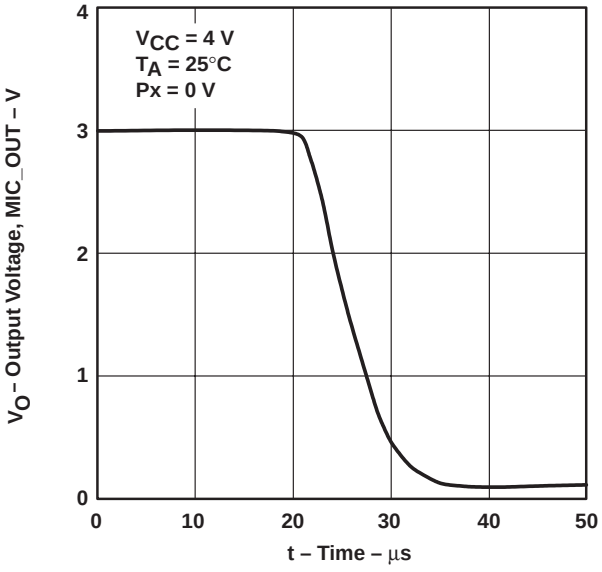


Figure 13. Microphone Slew Rate, Falling

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

QUIESENT CURRENT
vs
SUPPLY VOLTAGE

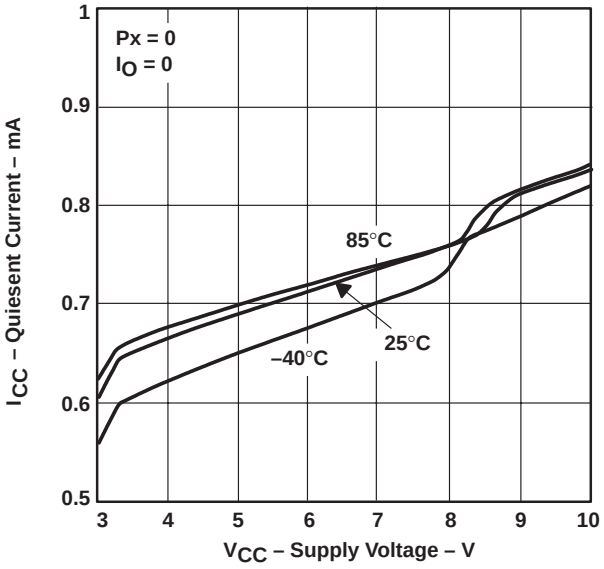

Figure 14

LDO REGULATORS
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

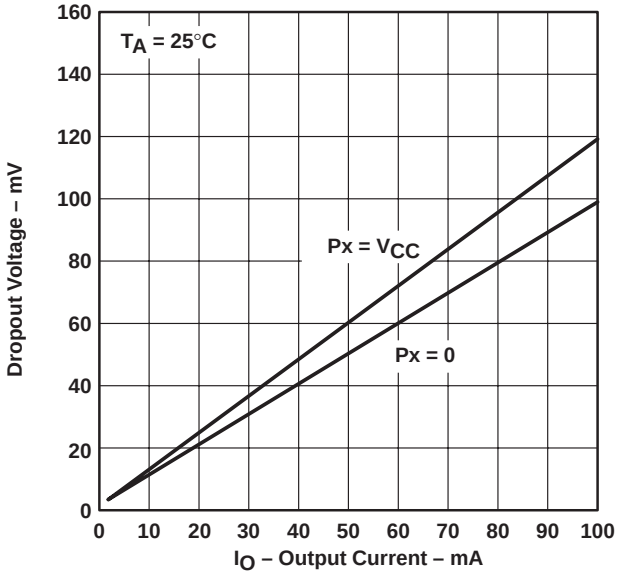

Figure 15

LDO REGULATORS
DROPOUT VOLTAGE
vs
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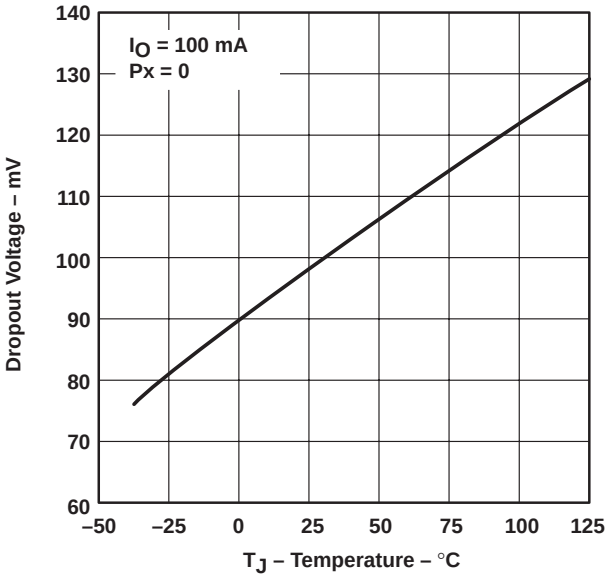

Figure 16

LDO REGULATORS
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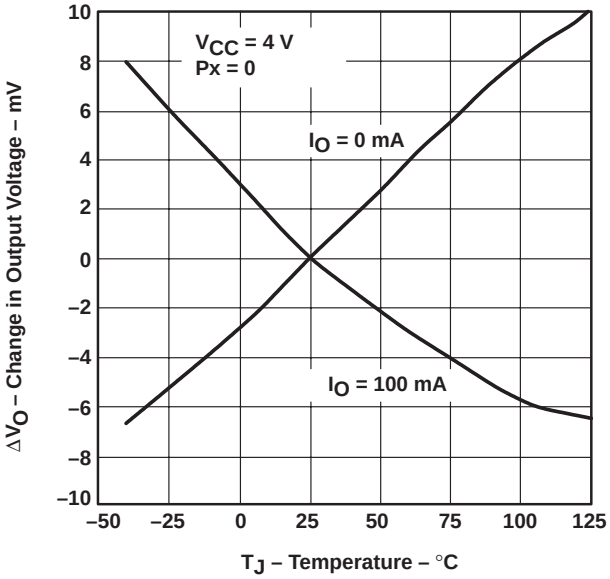

Figure 17

TYPICAL CHARACTERISTICS

REGULATOR L
OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

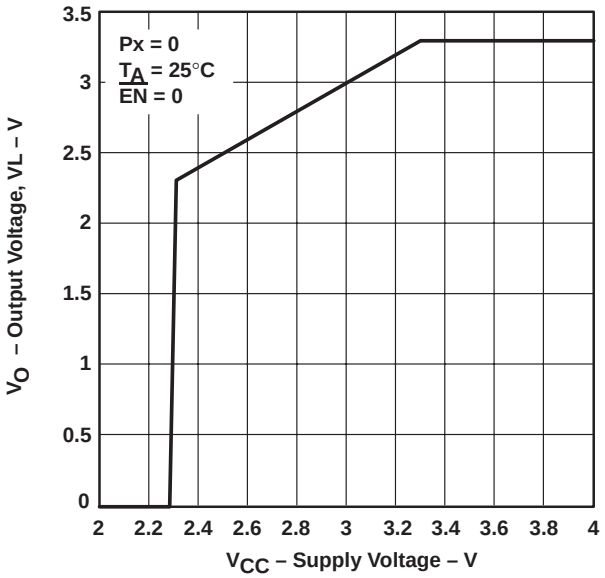

Figure 18

LDO REGULATORS
CHANGE IN OUTPUT VOLTAGE
vs
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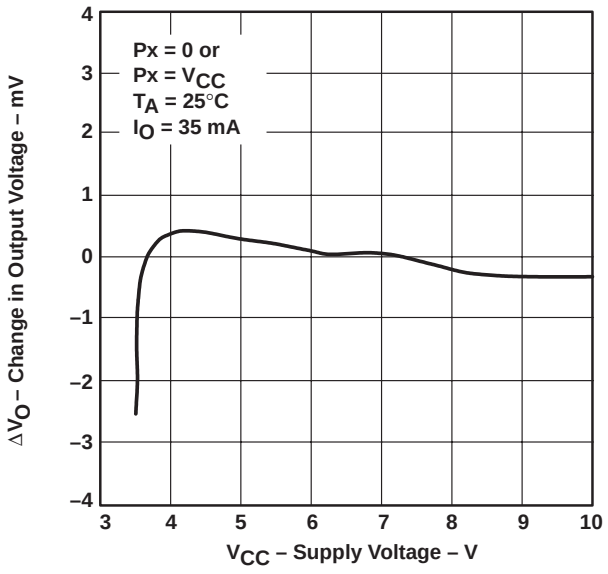

Figure 19

LDO REGULATORS
CHANGE IN OUTPUT VOLTAGE
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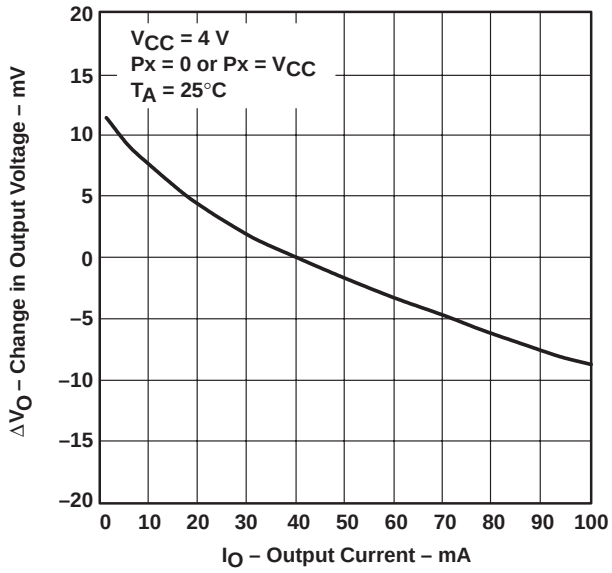

Figure 20

SHUTDOWN CURRENT
vs
SUPPLY VOLTAGE

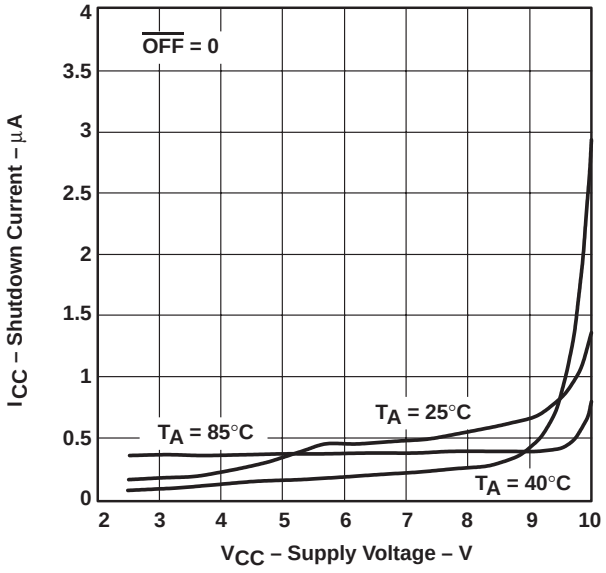

Figure 21

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TYPICAL CHARACTERISTICS

INPUT THRESHOLD VOLTAGE, $\overline{ON}$ vs SUPPLY VOLTAGE

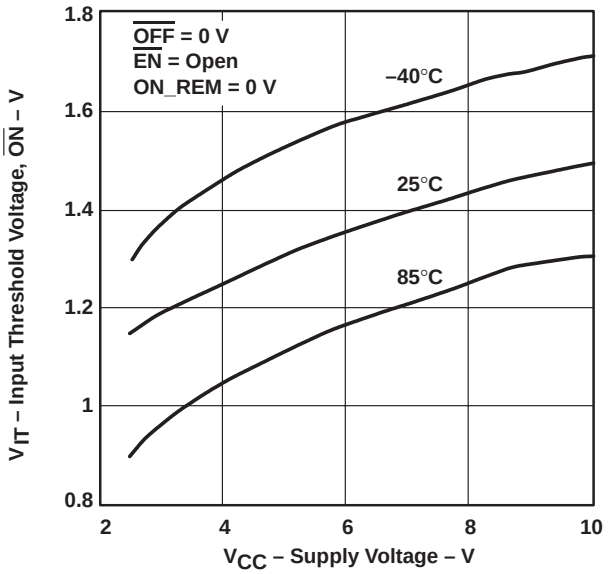


Figure 22

INPUT THRESHOLD VOLTAGE, EN vs SUPPLY VOLTAGE

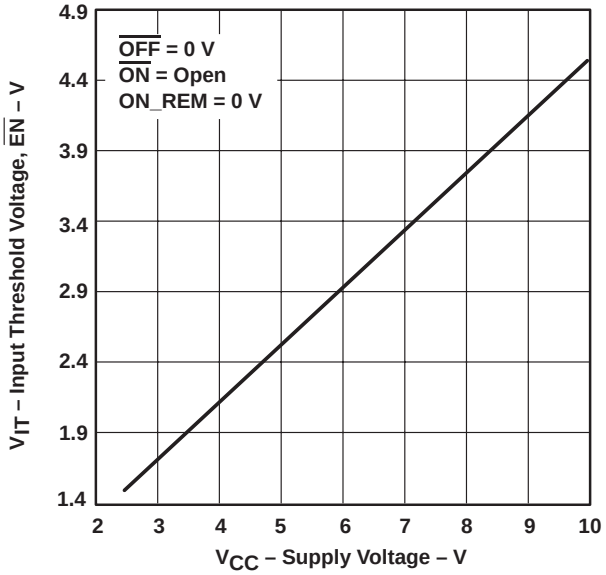


Figure 23

INPUT THRESHOLD VOLTAGE, ON_REM vs SUPPLY VOLTAGE

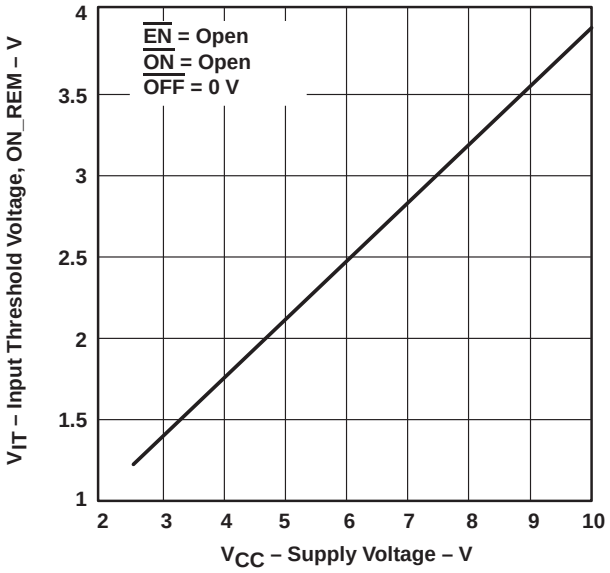


Figure 24

LDO REGULATORS
RIPPLE REJECTION vs FREQUENCY

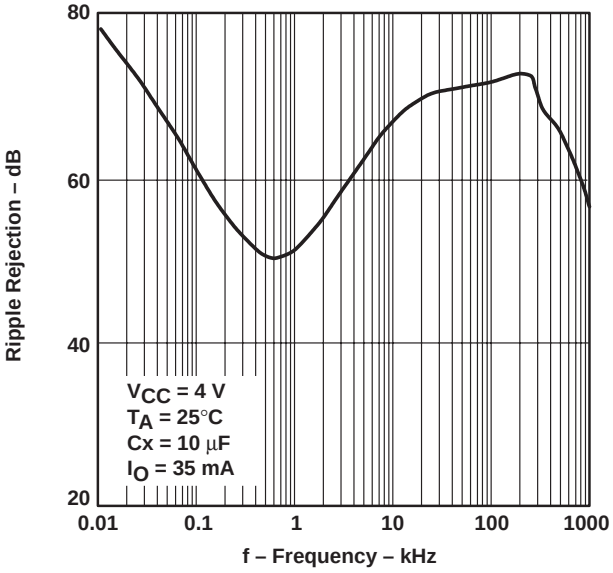


Figure 25

TYPICAL CHARACTERISTICS

REGULATOR L

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

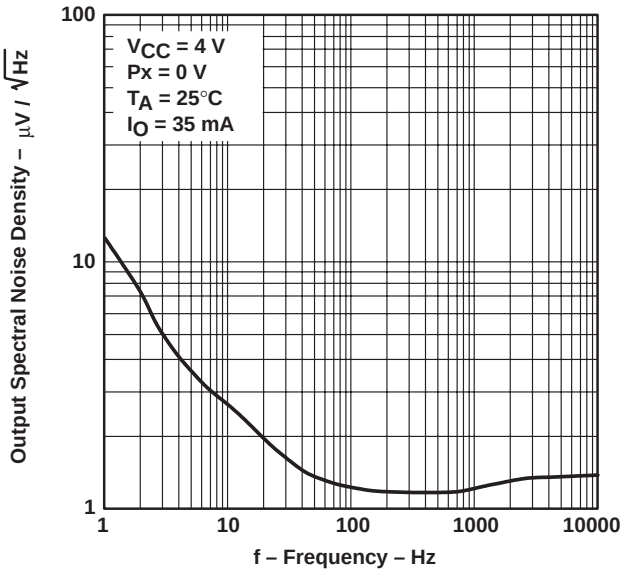


Figure 26

CHANGE IN FREQUENCY, CP
vs
JUNCTION TEMPERATURE

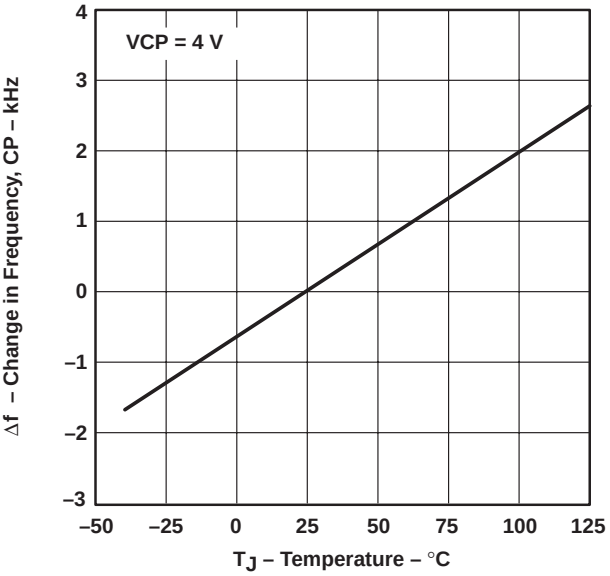


Figure 27

OUTPUT RESISTANCE, CP
vs
SUPPLY VOLTAGE

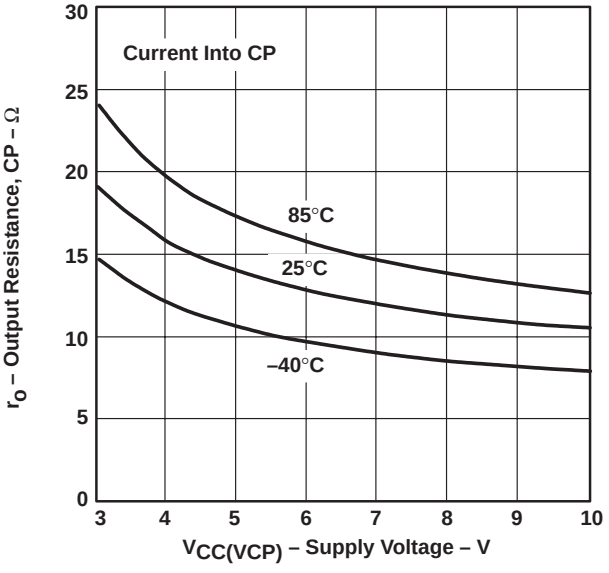


Figure 28

OUTPUT RESISTANCE, CP
vs
SUPPLY VOLTAGE

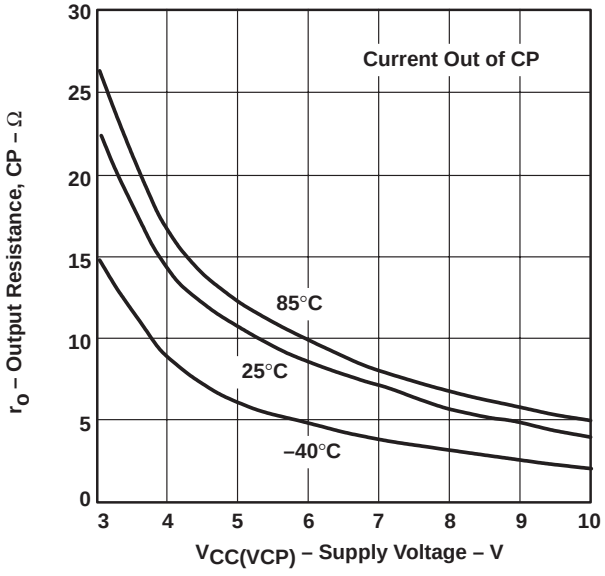


Figure 29

TYPICAL CHARACTERISTICS

SPEAKER AND RINGER AMPLIFIERS
MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

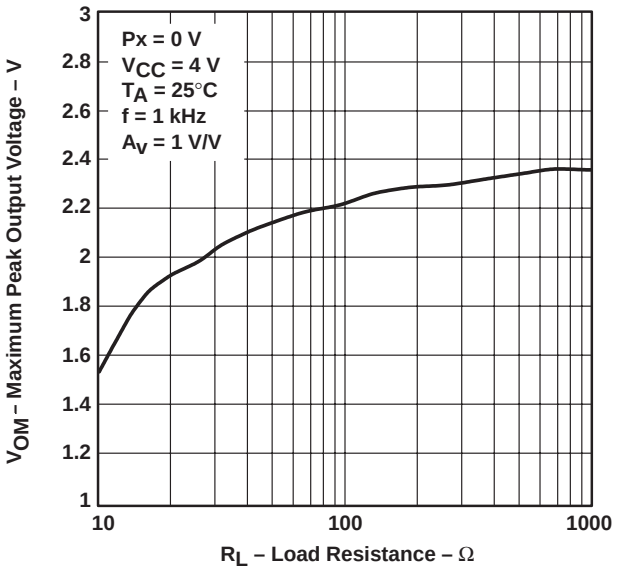


Figure 30

SPEAKER AND RINGER AMPLIFIERS
TOTAL HARMONIC DISTORTION
vs
FREQUENCY

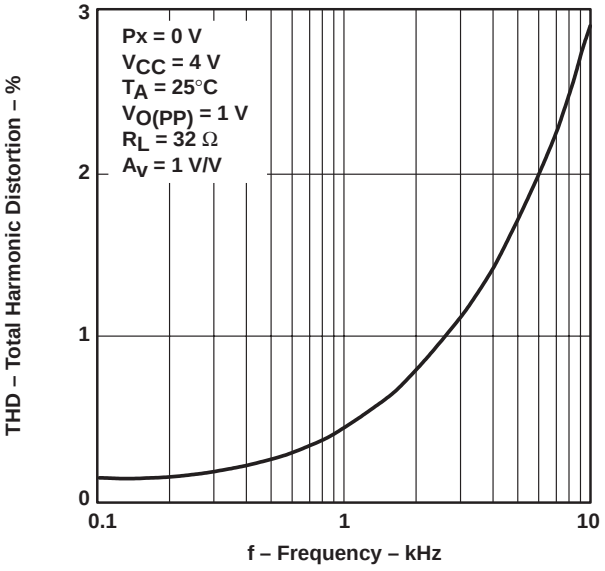


Figure 31

SPEAKER AND RINGER AMPLIFIERS
TOTAL HARMONIC DISTORTION
vs
LOAD RESISTANCE

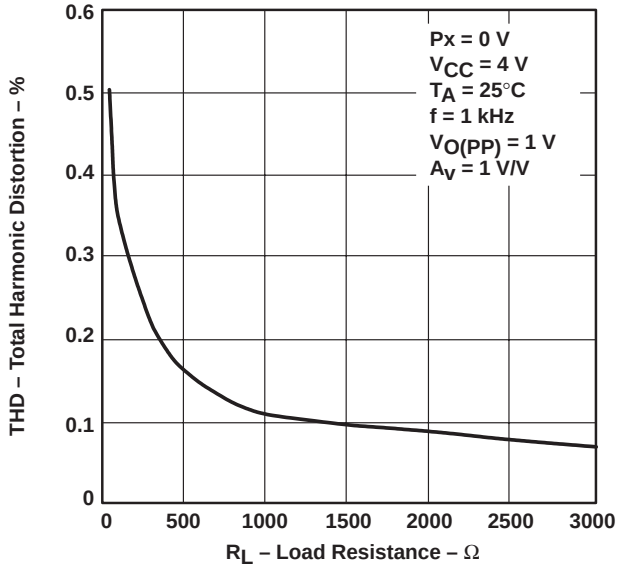


Figure 32

SPEAKER AND RINGER AMPLIFIERS
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

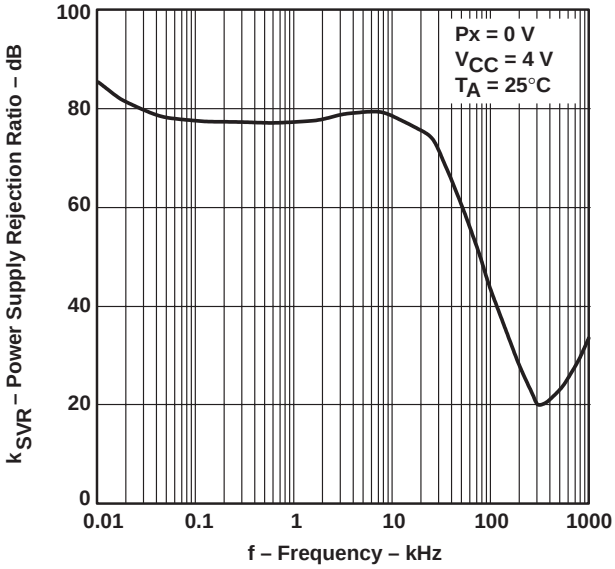


Figure 33

TYPICAL CHARACTERISTICS

SPEAKER AND RINGER AMPLIFIERS
OUTPUT NOISE VOLTAGE
vs
FREQUENCY

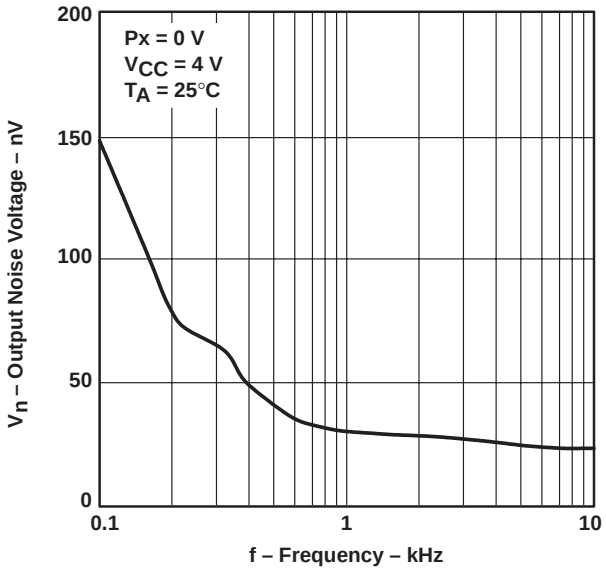


Figure 34

SPEAKER AND RINGER AMPLIFIERS
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

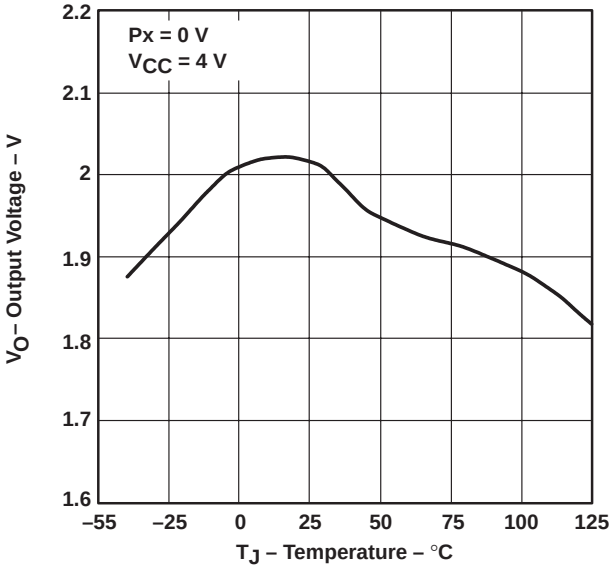


Figure 35

MICROPHONE AMPLIFIER
MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

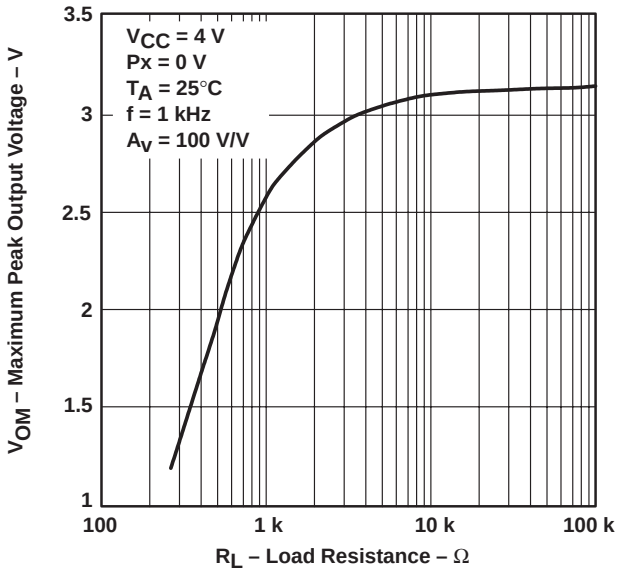


Figure 36

MICROPHONE AMPLIFIER
TOTAL HARMONIC DISTORTION
vs
FREQUENCY

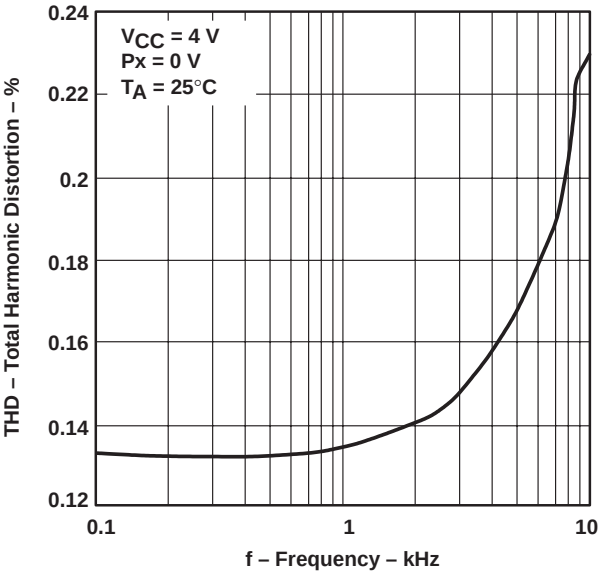


Figure 37

TYPICAL CHARACTERISTICS

MICROPHONE AMPLIFIER
TOTAL HARMONIC DISTORTION
vs
LOAD RESISTANCE

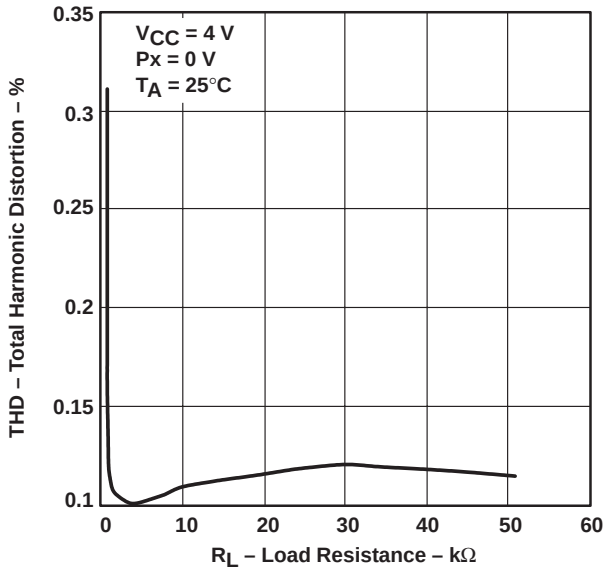


Figure 38

MICROPHONE AMPLIFIER
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

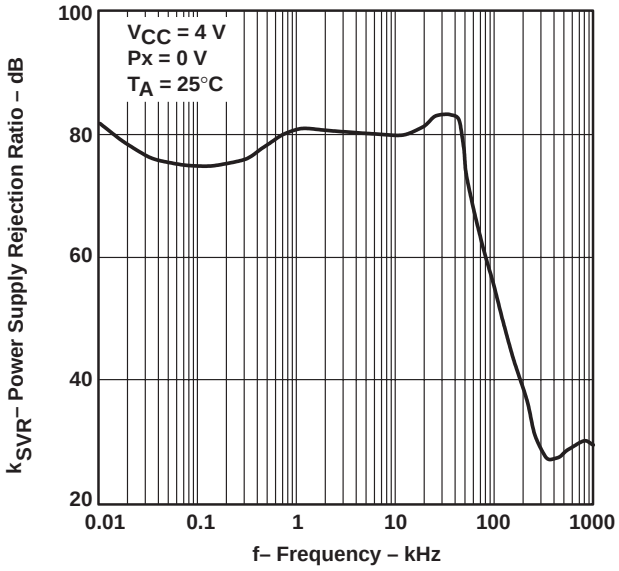


Figure 39

MICROPHONE AMPLIFIER
CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY

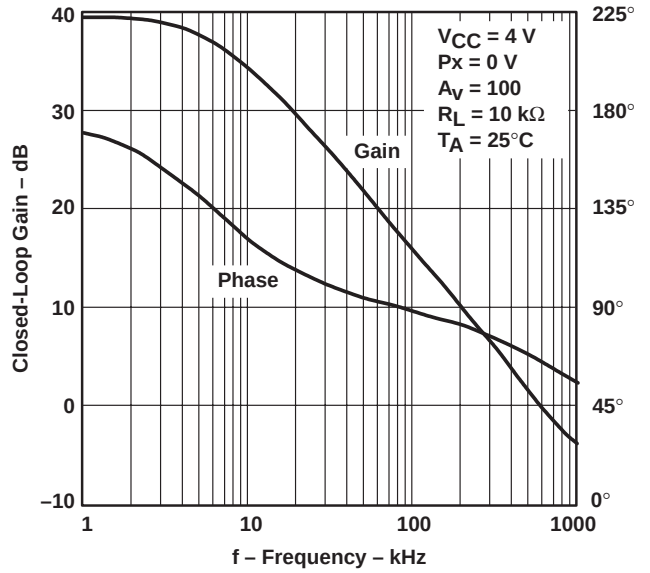


Figure 40

MICROPHONE AMPLIFIER
OUTPUT NOISE VOLTAGE
vs
FREQUENCY

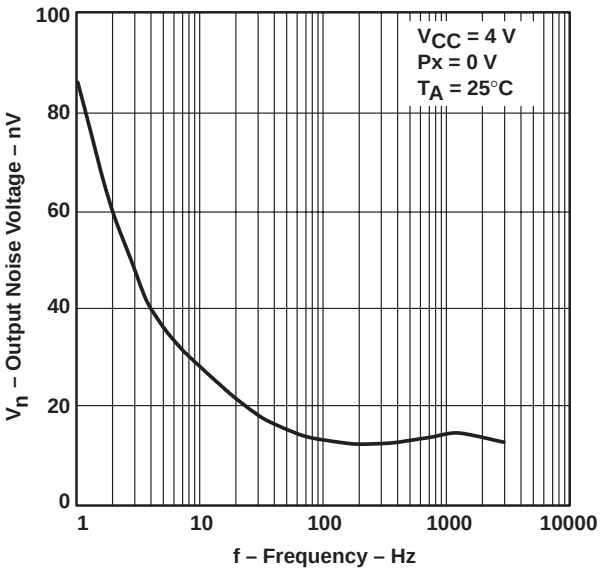


Figure 41

TYPICAL CHARACTERISTICS

MICROPHONE AMPLIFIER
PHASE MARGIN
vs
LOAD CAPACITANCE

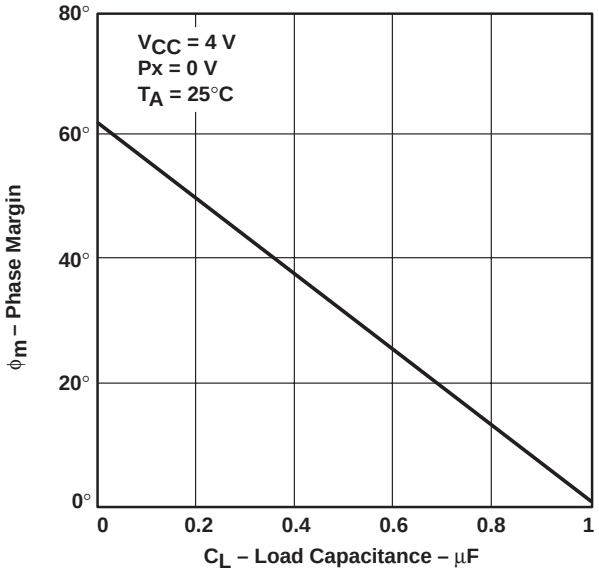


Figure 42

THERMAL INFORMATION

Using thermal resistance, junction-to-ambient ($R_{\theta JA}$), maximum power dissipation can be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

Where $T_{J(max)}$ is the maximum allowable junction temperature or 125°C.

This limit should then be applied to the internal power dissipation of the TPS9104. The equation for calculating total internal power dissipation of the TPS9104 is:

$$P_{D(max)} = \sum_{x} \left(V_I - V_X\right) \times I_X + V_I \times I_Q$$

Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

APPLICATION INFORMATION

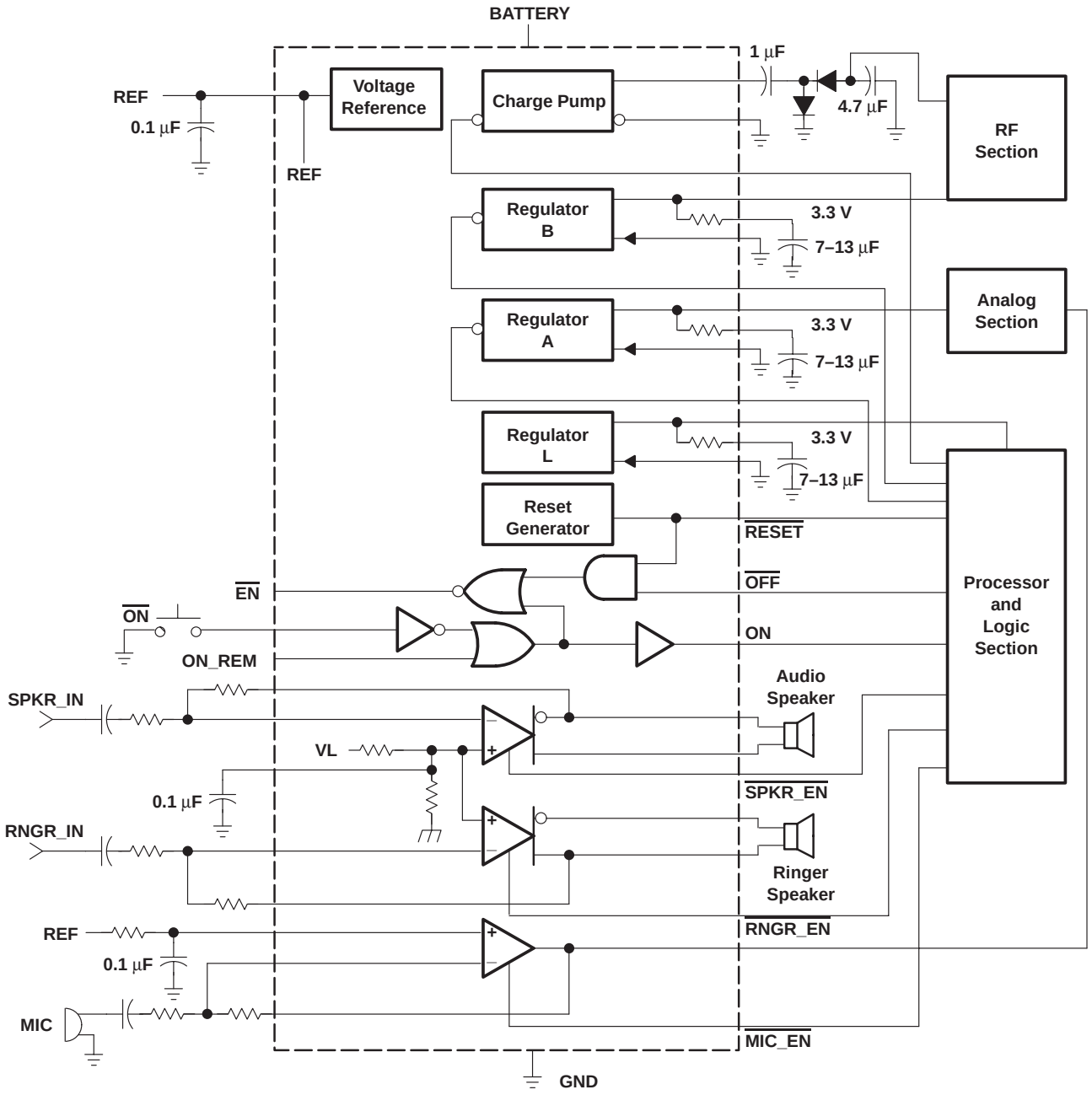


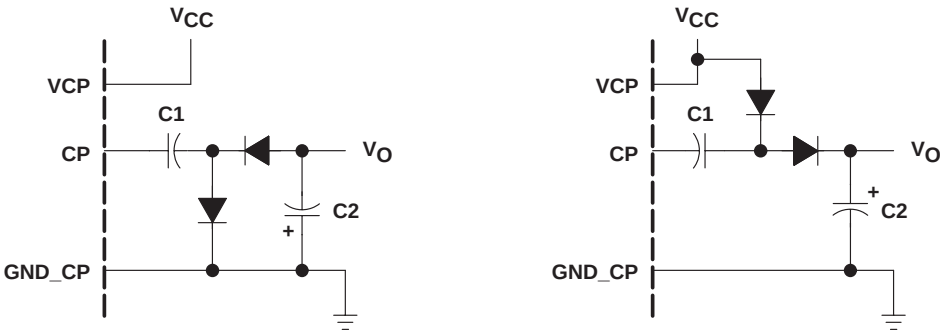
Figure 43. Typical Application

APPLICATION INFORMATION

LDOs (VL, VA, VB) output capacitors

A 10-μF capacitor must be tied to Cx (CL, CA, or CB). The Cx terminal is connected internally to the output of the LDO through a 1-Ω resistor. The stability of LDOs is dependent on the ESR of the output filter capacitor. Most LDOs are designed to be stable over a narrow range of ESR with lower limits and upper limits, thus limiting the type of capacitor that can be used. With the use of the internal 1-Ω resistor, the lower ESR limit of the capacitor is eliminated, permitting the upper limit to be raised. Therefore, almost any tantalum or ceramic capacitor can be used, provided the ESR does not exceed 15 Ω over temperature.

charge pump design



a. Voltage Inverter b. Voltage Doubler

Figure 44. Charge Pump Configurations

The charge-pump terminal can drive either a voltage inverter or a voltage doubler. In either case only two capacitors and two signal diodes are needed. The output voltage is unregulated and a regulator may be added if needed.

The charge transfer of C1 is:

$$\Delta q = C1 \times (V_{CC} - V_O)$$

This occurs f times a second and the charge transfer per unit time (current) is:

$$I = f \times C1 \times (V_{CC} - V_O)$$

Rewriting this equation in the form of I = V/R

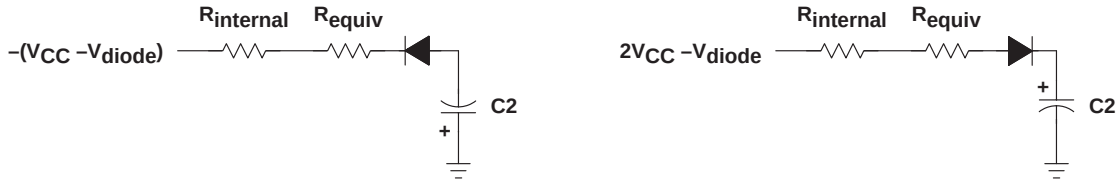
$$I = \frac{V_{CC} - V_O}{\frac{1}{f \times C1}}$$

where $\frac{1}{f \times C1}$ is an equivalent resistor.

APPLICATION INFORMATION

charge pump design (continued)

An equivalent circuit can now be drawn taking the diodes into account.



a. Voltage Inverter **b. Voltage Doubler**

Figure 45. Equivalent Circuit

The output voltage for the doubler is then:

$$V_O = 2 \times V_{CC} - 2 \times V_{diode} - I_O \times R_{total}$$

and the output voltage for the inverter is:

$$V_O = -(V_{CC} - 2 \times V_{diode}) + I_O \times R_{total}$$

To determine the size of C1 use

$$C = \frac{I}{f \times \Delta V}$$

where f = 100,000 and ΔV = ripple voltage.

For an output current of 10 mA calculate

$$C1 = \frac{0.01\ A}{100\ kHz \times 0.1\ V_{ripple}} = 1\ \mu F$$

Because of losses caused by diode switching and ESR, the calculated capacitance should be multiplied by 1.5 to 2. A 2-µF capacitance should drive a 10-mA voltage doubler or inverter.

amplifier design

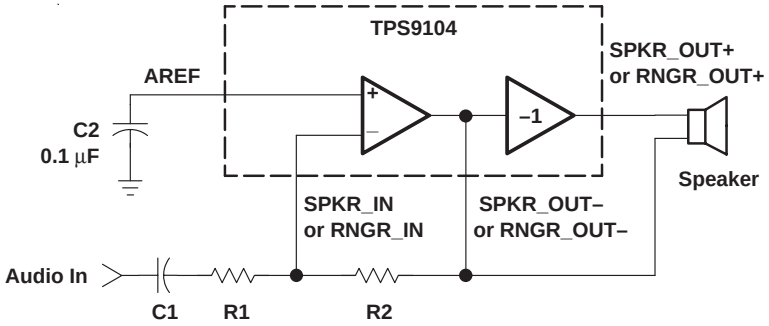


Figure 46. Speaker and Ringer Amplifiers

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APPLICATION INFORMATION

amplifier design (continued)

The speaker and ringer amplifiers are capable of driving either dynamic or piezoelectric speakers. The gain is set with two external resistors connected as shown. There is an inverting stage and a noninverting stage, both of which can drive a speaker differentially. When the speaker is connected in the differential mode, the gain is doubled. The gain equation is

$$G = \frac{R2}{R1} \times 2$$

Typically R2 is in the range of 10 kΩ to 100 kΩ and the gain can be as high as 10. The noninverting amplifier input is connected to the internal reference and should be bypassed with a 0.1-μF capacitor. The audio input signal must be capacitor-coupled (refer to C1 in Figure 47). R1 and C1 determine the low-frequency pole (f_p) location. The frequency response of the input RC is:

$$f_p = \frac{1}{2 \times \pi \times R1 \times C1}$$

For a 0.22-μF capacitor and a 1-kΩ resistor, the 3-dB point is

$$f_p = \frac{1}{2 \times \pi \times 1K \times 0.22\ \mu F} = 750\ Hz$$

Both V_{CC} and VL supply power to the speaker and ringer amplifiers. The output of VL is used to power the high-gain input stage, and V_{CC} is used to power the low-gain high-current output stage. When driving a highly capacitive load, series resistance should be added to minimize signal distortion.

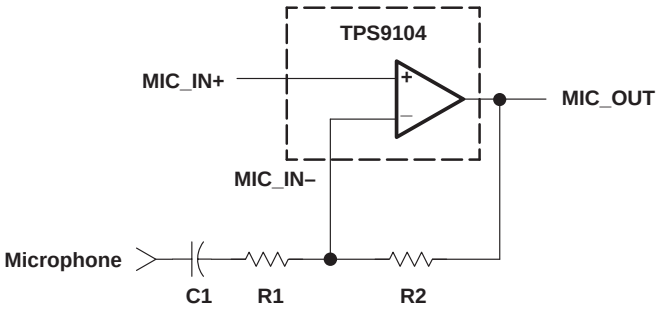


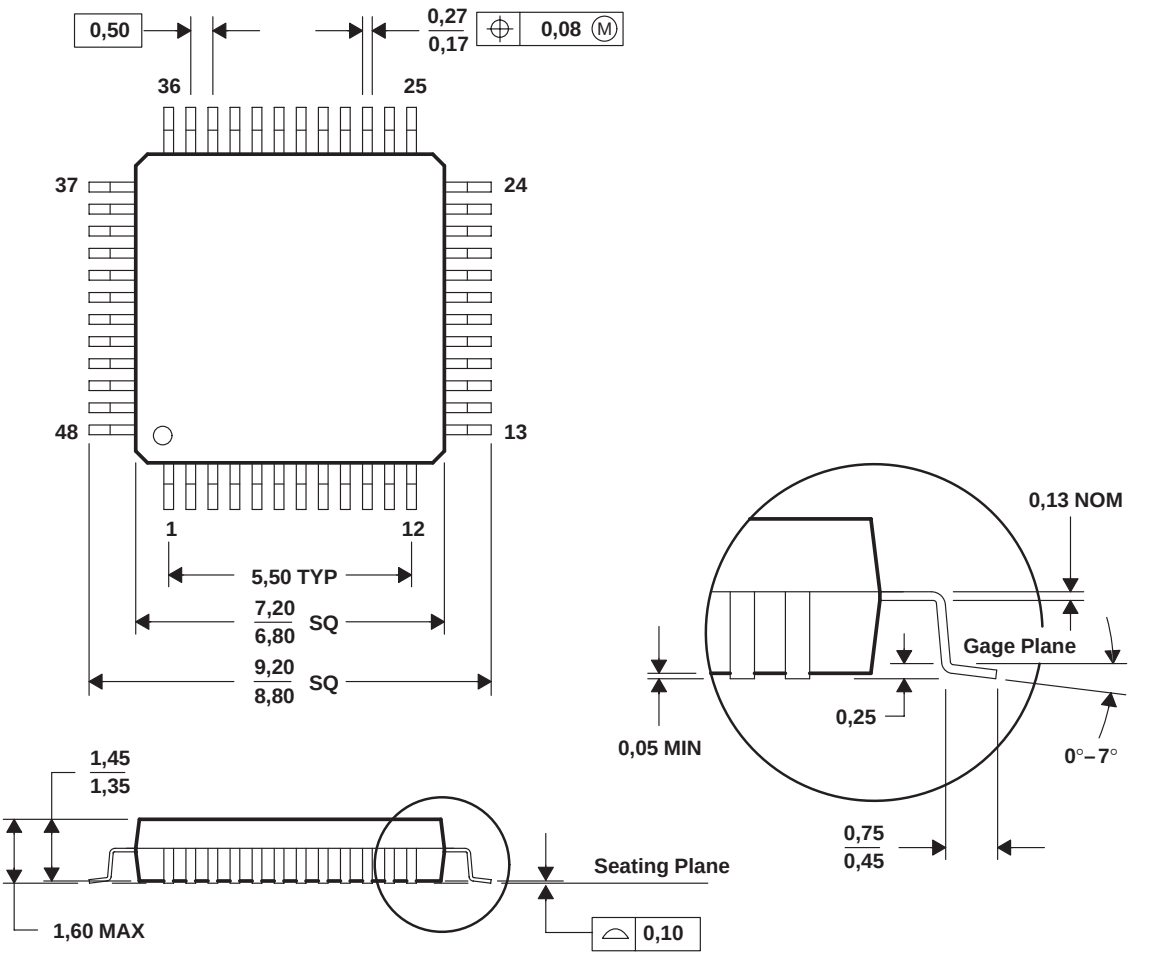
Figure 47. Microphone Amplifier

This is a high-gain amplifier capable of driving a 10 kΩ load at 3 V. The gain is set using two external resistors, R1 and R2. A low noise reference must be connected to MIC_IN+. The gain equation is: $G = \frac{R2}{R1}$. Typically R2 can be in the range of 10 kΩ to 100 kΩ and the gain can be up to 100. The microphone must be either capacitor-coupled (C1) or tied to the reference. The closed-loop –3 dB point for this amplifier is a minimum of 4 kHz. The location of the low-frequency pole can be calculated using

$$f_p = \frac{1}{2 \times \pi \times R1 \times C1}$$

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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