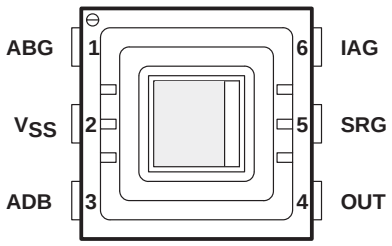
- **Full-Frame Operation**
- **Antiblooming Capability**
- **Single-Phase Clocking for Horizontal and Vertical Transfers**
- **Fast Clear Capability**
- **Dynamic Range . . . 60 dB Typical**
- **High Blue Response**
- **High Photoresponse Uniformity**
- **Solid-State Reliability With No Image Burn-In, Residual Imaging, Image Distortion, Image Lag, or Microphonics**
- **6-Pin Dual-In-Line Ceramic Package**
- **Square Image Area:**
  - **2640 μm by 2640 μm**
  - **192 Pixels (H) by 165 Pixels (V)**
  - **Each Pixel 13.75 μm (H) by 16 μm (V)**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

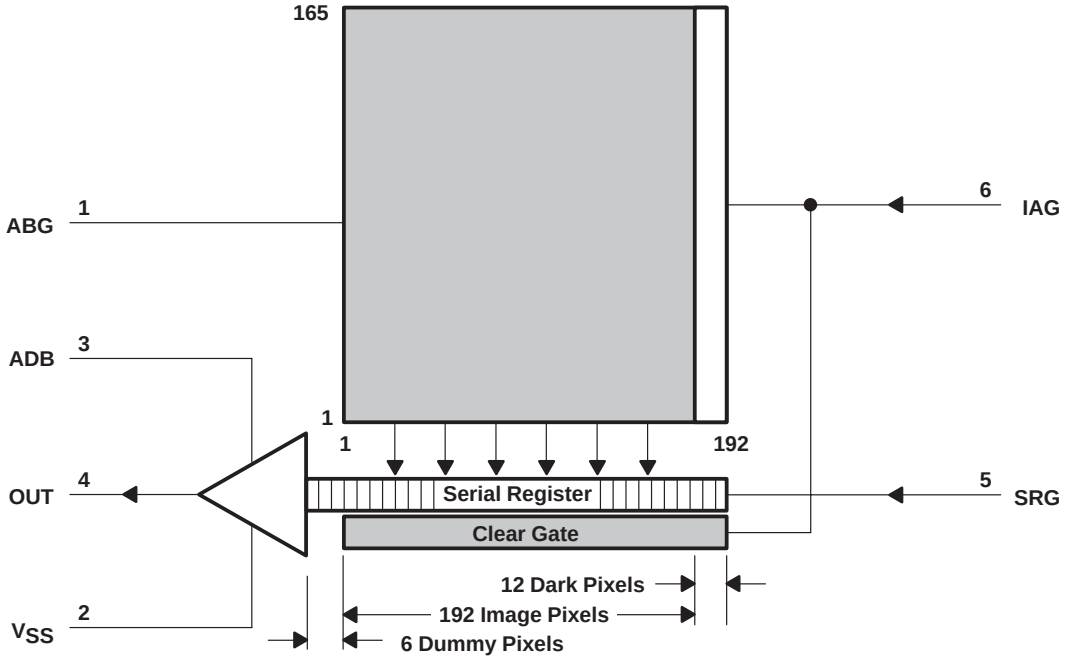
The TC211 is a full-frame charge-coupled device (CCD) image sensor designed specifically for industrial applications requiring ruggedness and small size. The image-sensing area is configured into 165 horizontal lines each containing 192 pixels. Twelve additional pixels are provided at the end of each line to establish a dark reference and line clamp. The antiblooming feature is activated by supplying clock pulses to the antiblooming gate, an integral part of each image-sensing element. The charge is converted to signal voltage at 4 μV per electron by a high-performance structure with built-in automatic reset and a voltage-reference generator. The signal is further buffered by a low-noise two-stage source-follower amplifier to provide high output-drive capability.

The TC211 is supplied in a 6-pin dual-in-line ceramic package approximately 7,5 mm (0.3 in.) square. The glass window can be cleaned using any standard method for cleaning optical assemblies or by wiping the surface with a cotton swab soaked in alcohol.

The TC211 is characterized for operation from –10°C to 45°C.

This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to V_{SS}. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to V_{SS} during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABG	1	I	Antiblooming gate
V_{SS}	2		Amplifier ground
ADB	3	I	Supply voltage for amplifier drain bias
OUT	4	O	Output signal
SRG	5	I	Serial-register gate
IAG	6	I	Image-area gate storage

functional description

The image-sensing area consists of 165 horizontal image lines each containing 192 photosensitive elements (pixels). Each pixel is 13.75 µm (horizontal) by 16.00 µm (vertical). As light enters the silicon in the image-sensing area, free electrons are generated and collected in potential wells (see Figure 1). During this time, the antiblooming gate is activated by applying a burst of pulses every horizontal blanking interval. This prevents blooming caused by the spilling of charge from overexposed elements into neighboring elements. The antiblooming gate is typically held at a midlevel voltage during readout. The quantity of charge collected in each pixel is a linear function of the incident light and the exposure time. After exposure and under dark conditions, the charge packets are transferred from the image area to the serial register at the rate of one image line per each clock pulse applied to the image-area gate. Once an image line has been transferred into the serial register, the serial-register gate can be clocked until all of the charge packets are moved out of the serial register to the charge detection node at the amplifier input.

There are 12 dark pixels to the right of the 192 image pixels on each image line. These dark pixels are shielded from incident light and the signal derived from them can be used to generate a dark reference for restoration of the video black level on the next image line.

functional description (continued)

Each clock pulse applied to the image area gate causes an automatic fast clear of the 192 image pixels and 12 dark pixels of the serial register before the next image line is transferred into the serial register. (Note that the six dummy pixels at the front of the serial register, which are used to transport charge packets from the serial register to the amplifier input, are not cleared by the image area gate clock.) The automatic fast-clear feature can be used to initialize the image area by transferring all 165 image lines to the serial register gate under dark conditions without clocking the serial register gate.

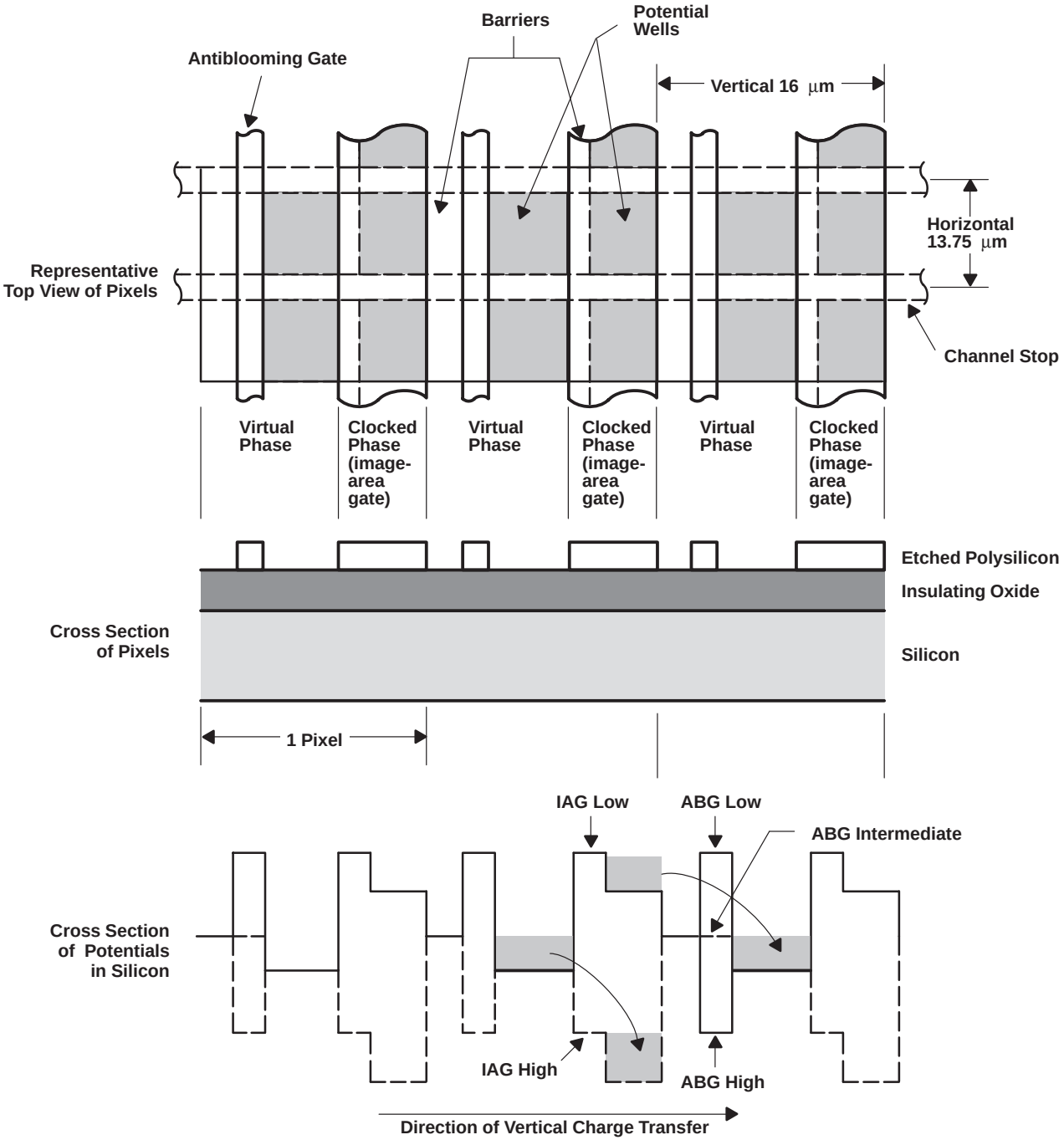


Figure 1. Charge Accumulation and Transfer Process

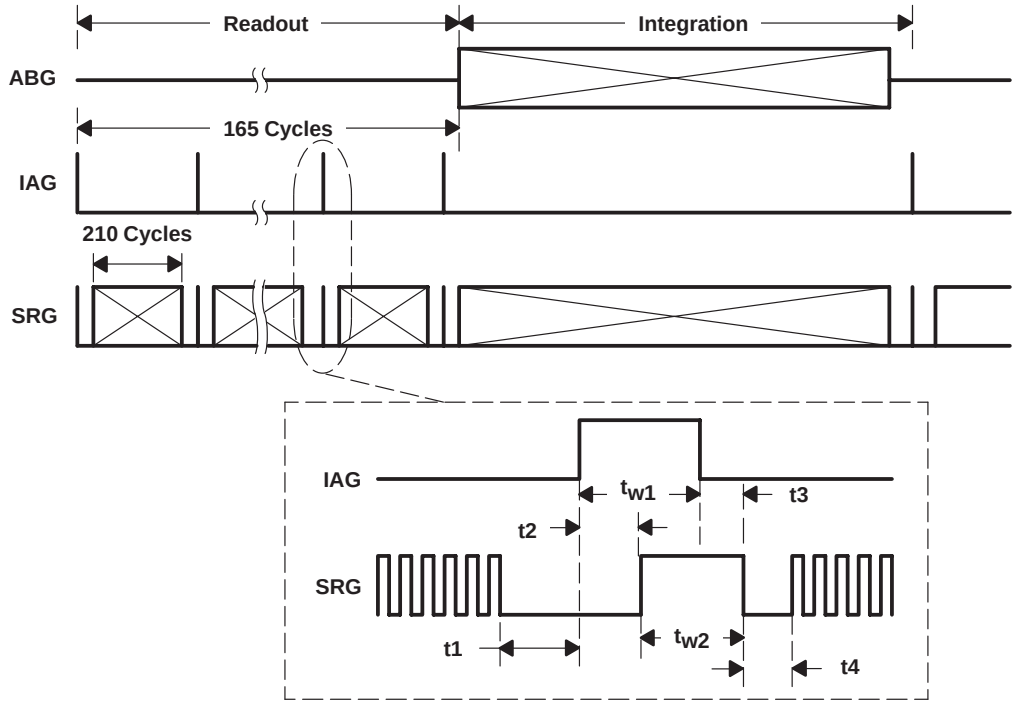


Figure 2. Timing Diagram, Noninterlace Mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range for ADB (see Note 1) . . . . . 0 V to 15 V
Input voltage range for IAG, SRG, ABG, V_I . . . . . –15 V to 5 V
Operating free-air temperature range . . . . . –30°C to 85°C
Storage temperature range, T_A . . . . . –30°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, ADB			11	12	13	V
Substrate bias voltage				0		V
Input voltage, V_I†	IAG	High level	1.5	2	2.5	V
		Intermediate level‡	–10	–5	2	
		Low level	–11	–10	–9	
	SRG	High level	1.5	2	2.5	
		Low level	–11	–10	–9	
	ABG	High level	4	4.5	5	
		Intermediate level‡	–3	–2.5	–2	
		Low level	–7.5	–7	–6.5	
Clock frequency, f_{clock}	IAG				1.5	MHz
	SRG				10	
	ABG				2	
t1	Time interval, SRG↓ to IAG↑		70			ns
t2	Time interval, IAG↑ to SRG transfer pulse ↑		0			ns
t_{W1}	Pulse duration, IAG high		350			ns
t_{W2}	Pulse duration, SRG transfer pulse high		350			ns
t3	Time interval, IAG↓ to SRG transfer pulse ↓		350			ns
t4	Time interval, SRG transfer pulse ↓ to SRG clock pulse ↑		70			ns
Capacitive load	OUT			12		pF
Operating free-air temperature, T_A			–10		45	°C

† The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.

‡ Adjustment is required for optimal performance.

electrical characteristics over recommended operating range of supply voltage, T_A = –10°C to 45°C

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)	Antiblooming disabled (see Note 3)	60			dB
	Antiblooming enabled	57			
Charge conversion factor			4		μV/e
Charge transfer efficiency (see Note 4)		0.99990	0.99998		
Signal response delay time, τ (see Note 5 and Figure 5)			25		ns
Gamma (see Note 6)		0.97	0.98	0.99	
Output resistance			700	800	Ω
Noise voltage	1/f noise (5 kHz)		370		nV/√Hz
	Random noise, f = 100 kHz		70		
Noise equivalent signal			150		electrons
Rejection ratio at 7.16 MHz	From ADB to OUT (see Note 7)		19		dB
	From SRG to OUT (see Note 8)		37		
Supply current			5	10	mA
Input capacitance, C_i	IAG		1600		pF
	SRG		25		
	ABG		780		

† All typical values are at T_A = 25°C

NOTES: 2. Dynamic range is –20 times the logarithm of the mean noise signal divided by the saturation output signal.
3. For this test, the antiblooming gate must be biased at the intermediate level.
4. Charge transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical input signal.
5. Signal response delay time is the time between the falling edge of the SRG clock pulse and the output signal valid state.
6. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer function curve (this value represents points near saturation):

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

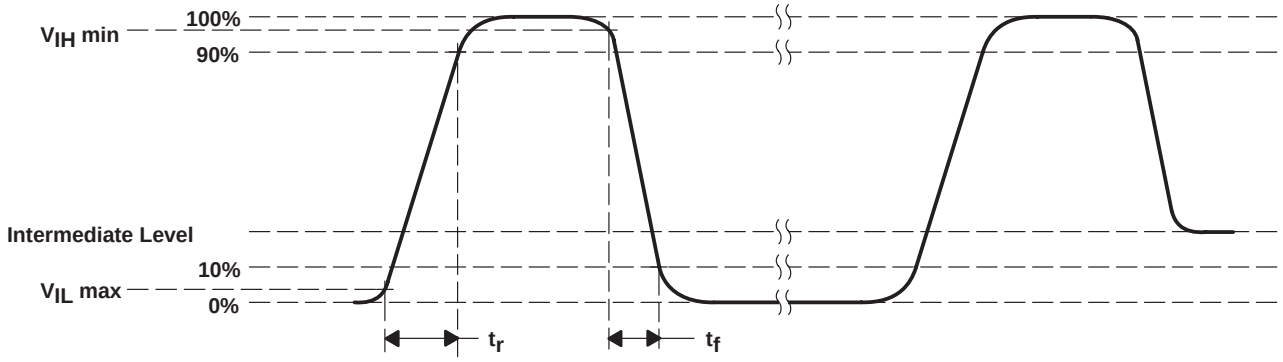
7. ADB rejection ratio is –20 times the logarithm of the ac amplitude at the OUT divided by the ac amplitude at ADB.
8. SRG rejection ratio is –20 times the logarithm of the ac amplitude at the OUT divided by the ac amplitude at SRG.

optical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity (see Note 9)	No IR filter	Measured at V_U (see Note 10)		260		mV/lx
	With IR filter			33		
Saturation signal (see Note 11)		Antiblooming disabled	400	600		mV
		Antiblooming enabled	350	450		
Blooming overload ratio (see Note 12)		Strobe		5		
		Shuttered light		100		
Output signal nonuniformity (1/2 saturation) (see Note 13)				10%	20%	
Image-area well capacity				150×10^3		electrons
Dark current		T_A = 21°C		0.027		nA/cm^2
Dark signal (see Note 14)				10	15	mV
Dark signal nonuniformity for entire field (see Note 15)				4	15	mV
Modulation transfer function		Horizontal		50%		
		Vertical		70%		

NOTES: 9. Sensitivity is measured at an integration time of 16.667 ms and a source temperature of 2856 K. A CM-500 filter is used.
10. V_U is the output voltage that represents the threshold of operation of antiblooming. $V_U \approx$ 1/2 saturation signal.
11. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.
12. Blooming overload ratio is the ratio of blooming exposure to saturation exposure.
13. Output signal nonuniformity is the ratio of the maximum pixel-to-pixel difference in output signal to the mean output signal for exposure adjusted to give 1/2 the saturation output signal.
14. Dark-signal level is measured from the dummy pixels.
15. Dark-signal nonuniformity is the maximum pixel-to-pixel difference in a dark condition.

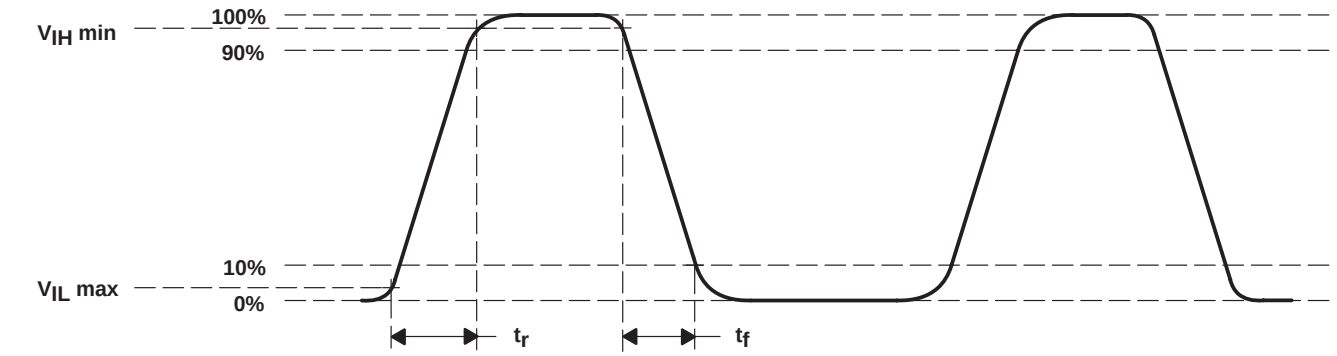
PARAMETER MEASUREMENT INFORMATION



t_r = 220 ns, t_f = 330 ns for IAG
t_r = 115 ns, t_f = 135 ns for ABG

Figure 3. Typical Clock Waveform for IAG and ABG

PARAMETER MEASUREMENT INFORMATION



t_r = 25 ns, t_f = 30 ns

Figure 4. Typical Clock Waveform for SRG

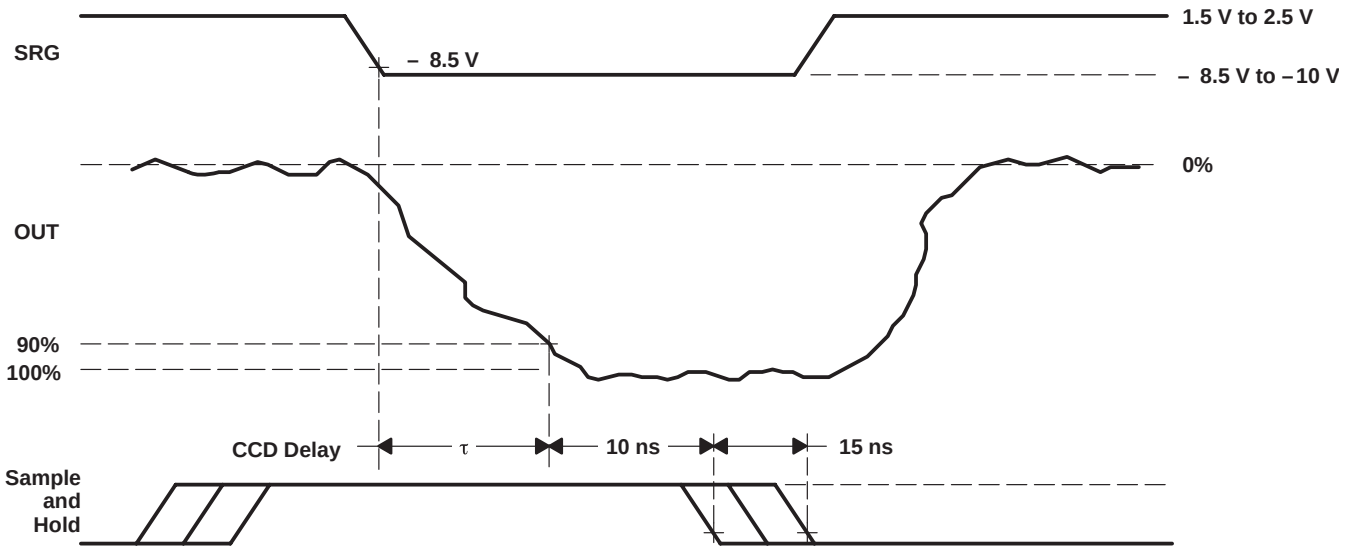


Figure 5. SRG and OUT Waveforms

TYPICAL CHARACTERISTICS

VERTICAL MODULATION TRANSFER FUNCTION (BARS PARALLEL TO SERIAL REGISTER)

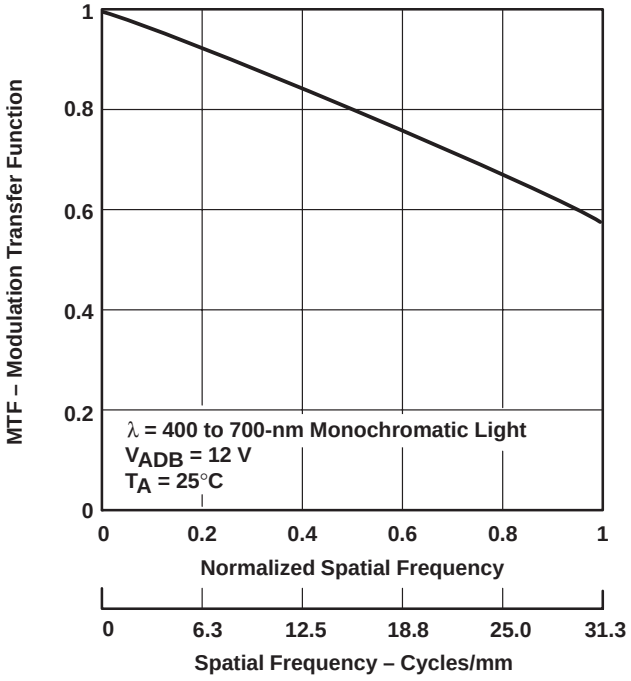


Figure 6

HORIZONTAL MODULATION TRANSFER FUNCTION (BARS PERPENDICULAR TO SERIAL REGISTER)

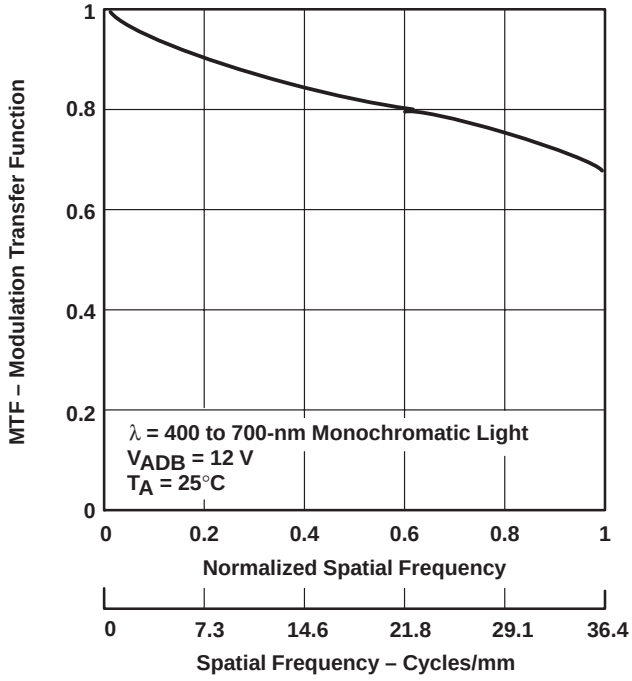


Figure 7

NOISE SPECTRUM OF OUTPUT AMPLIFIER

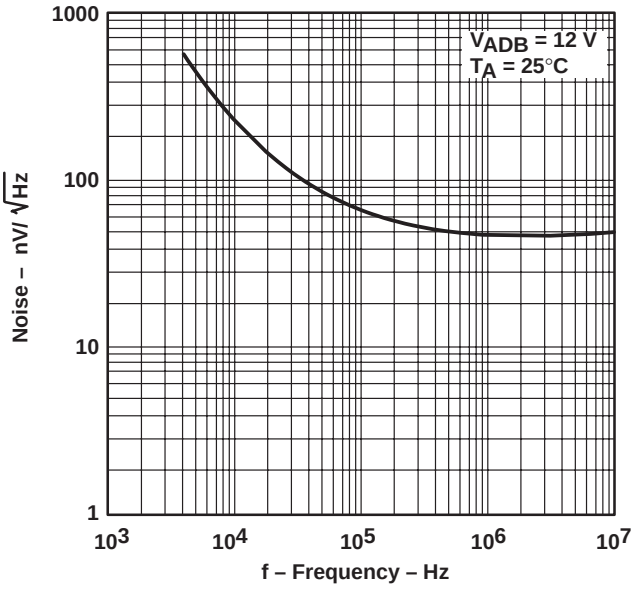


Figure 8

CCD SPECTRAL RESPONSIVITY

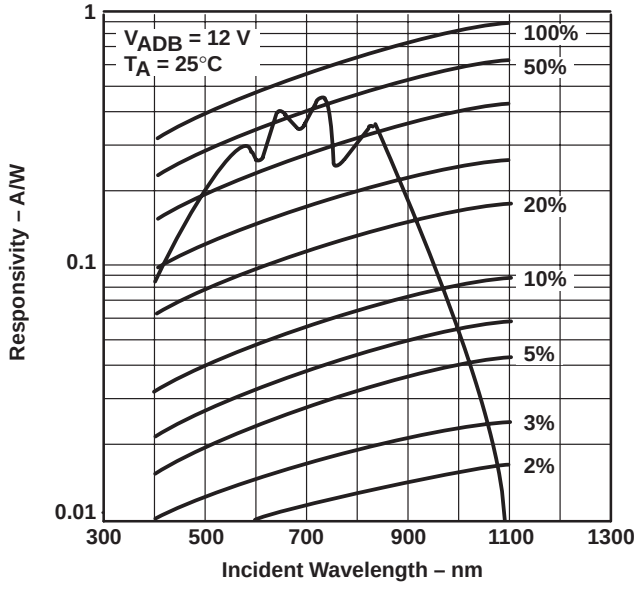
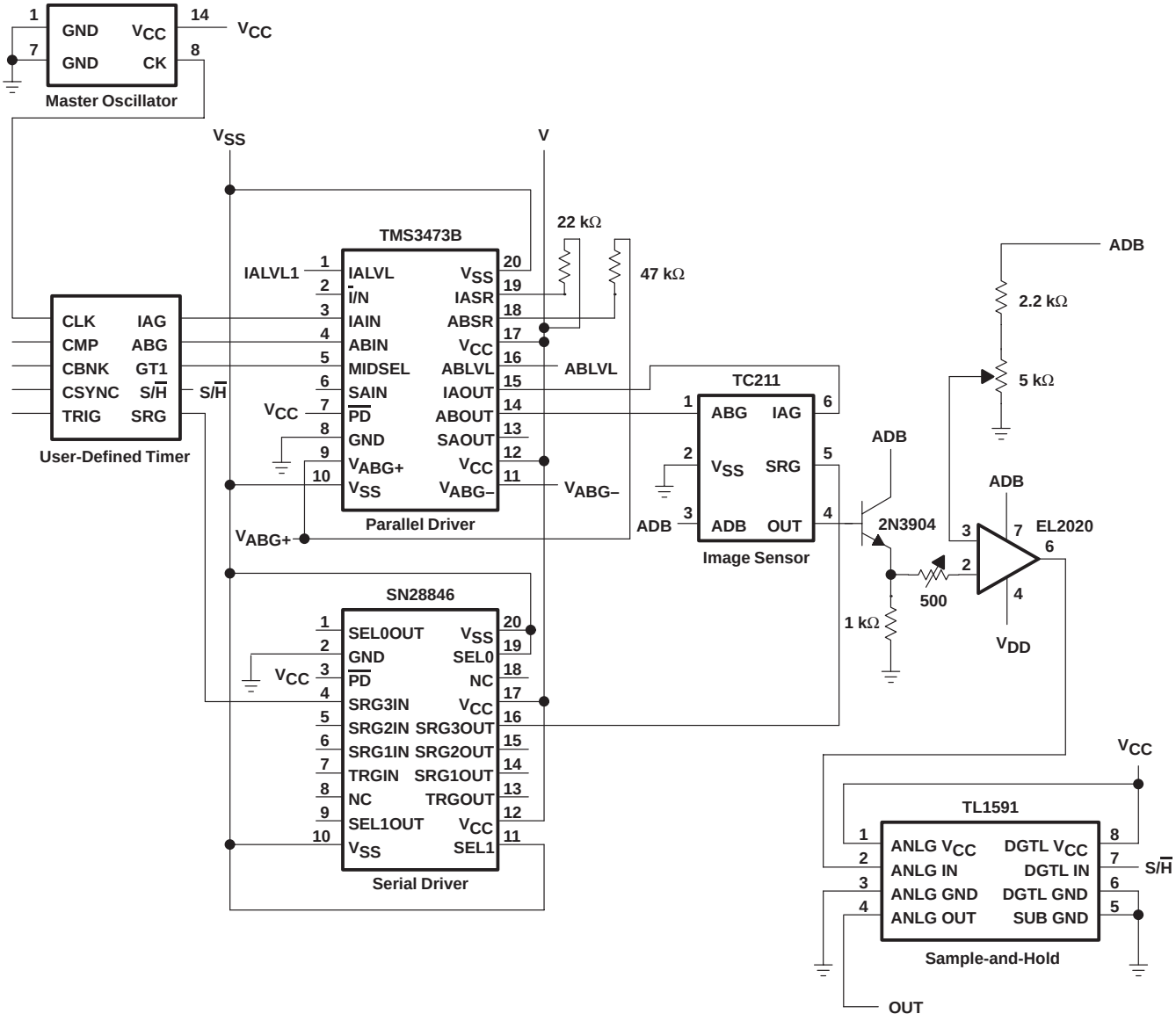


Figure 9

TYPICAL APPLICATION DATA

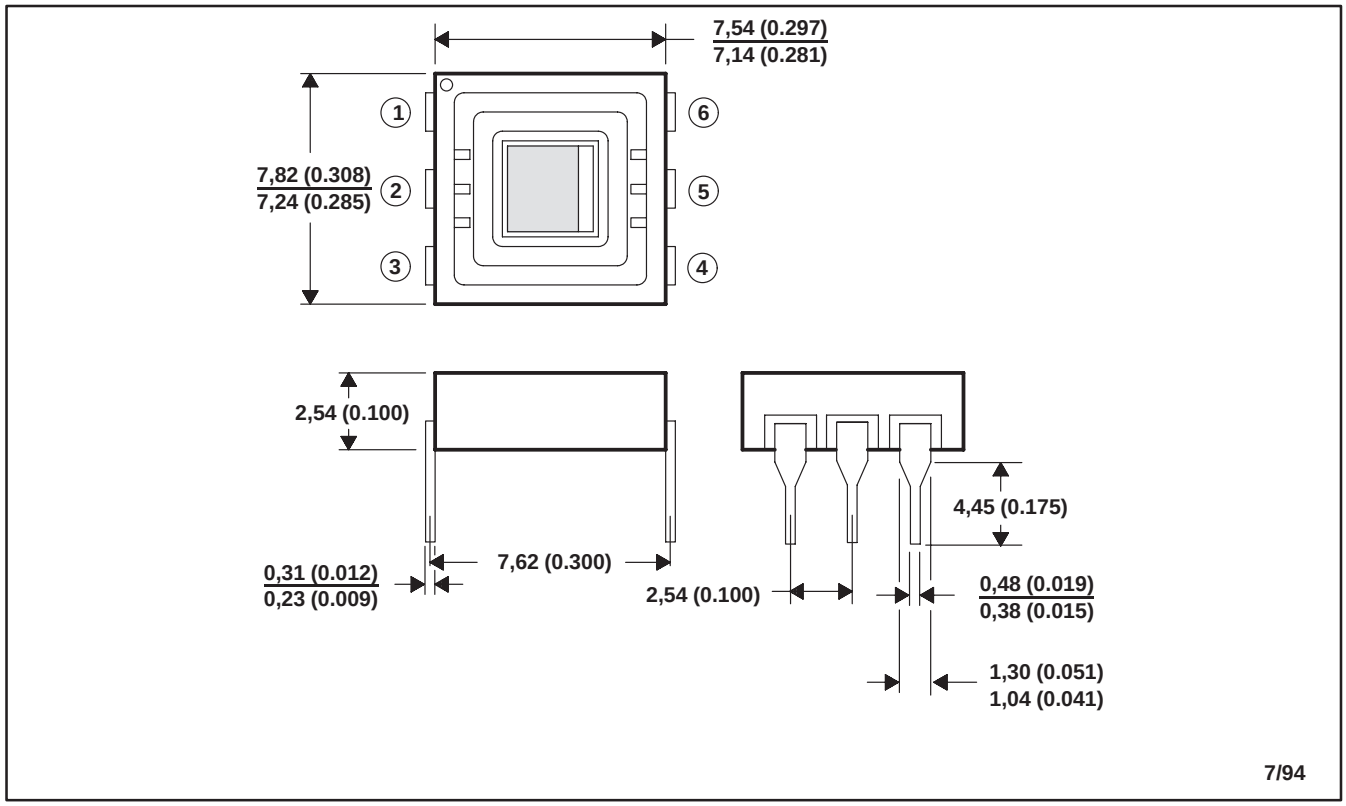


SUPPORT CIRCUITS			
DEVICE	**PACKAGE**	**APPLICATION**	**FUNCTION**
SN28846DW	20 pin small outline	Serial driver	Driver for SRG
TMS3473BDW	20 pin small outline	Parallel driver	Driver for IAG, ABG
TL1591CPS	8 pin small outline (EIAJ)	Sample and hold	Single-channel sample-and-hold IC

Figure 10. Typical Application Circuit Diagram

MECHANICAL DATA

The package for the TC211 consists of a ceramic base, glass window, and a 6-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line organization and fit into mounting holes with 2,54 mm (0.1 inch) center-to-center spacings.



NOTES: A. Dimensions are in millimeters and parenthetically in inches. Single dimensions are nominal.
B. The center of the package and the center of the image area are not coincident.
C. The distance from the top of the glass to the image sensor surface is typically 1 mm (0.04 inch). The glass is typically 0.020 inch thick and has an index of refraction of 1.52.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.