

CD74HC173, CD74HCT173

High Speed CMOS Logic Quad D-Type Flip-Flop, Three-State

Features

- Three-State Buffered Outputs
- Gated Input and Output Enables
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

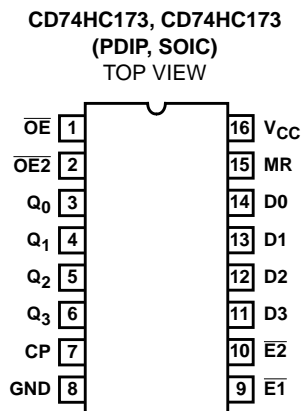
Description

The Harris CD74HC173 and CD74HCT173 high speed three-state quad D-type flip-flops are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus oriented systems.

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The CD74HCT173 logic family is functionally, as well as pin compatible with the standard 74LS logic family.

Pinout



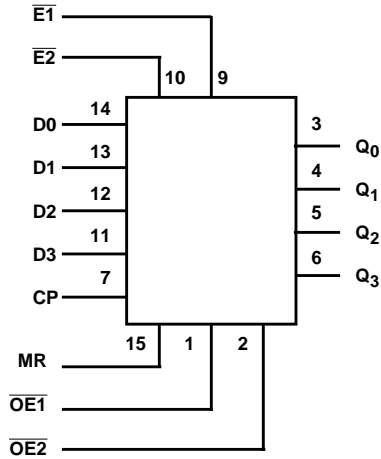
Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|------------|----------|
| CD74HC173E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HCT173E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74HC173M | -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74HCT173M | -55 to 125 | 16 Ld SOIC | M16.15 |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Functional Diagram



TRUTH TABLE

| INPUTS | | | | DATA | OUTPUT |
|--------|----|-----------------|-----------------|------|--------|
| MR | CP | DATA ENABLE | | | |
| | | $\overline{E1}$ | $\overline{E2}$ | D | Q_n |
| H | X | X | X | X | L |
| L | L | X | X | X | Q_0 |
| L | ↑ | H | X | X | Q_0 |
| L | ↑ | X | H | X | Q_0 |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

NOTE:

When either $\overline{OE1}$ or $\overline{OE2}$ (or both) is (are) high the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.

H = High Voltage Level

L = Low Voltage Level

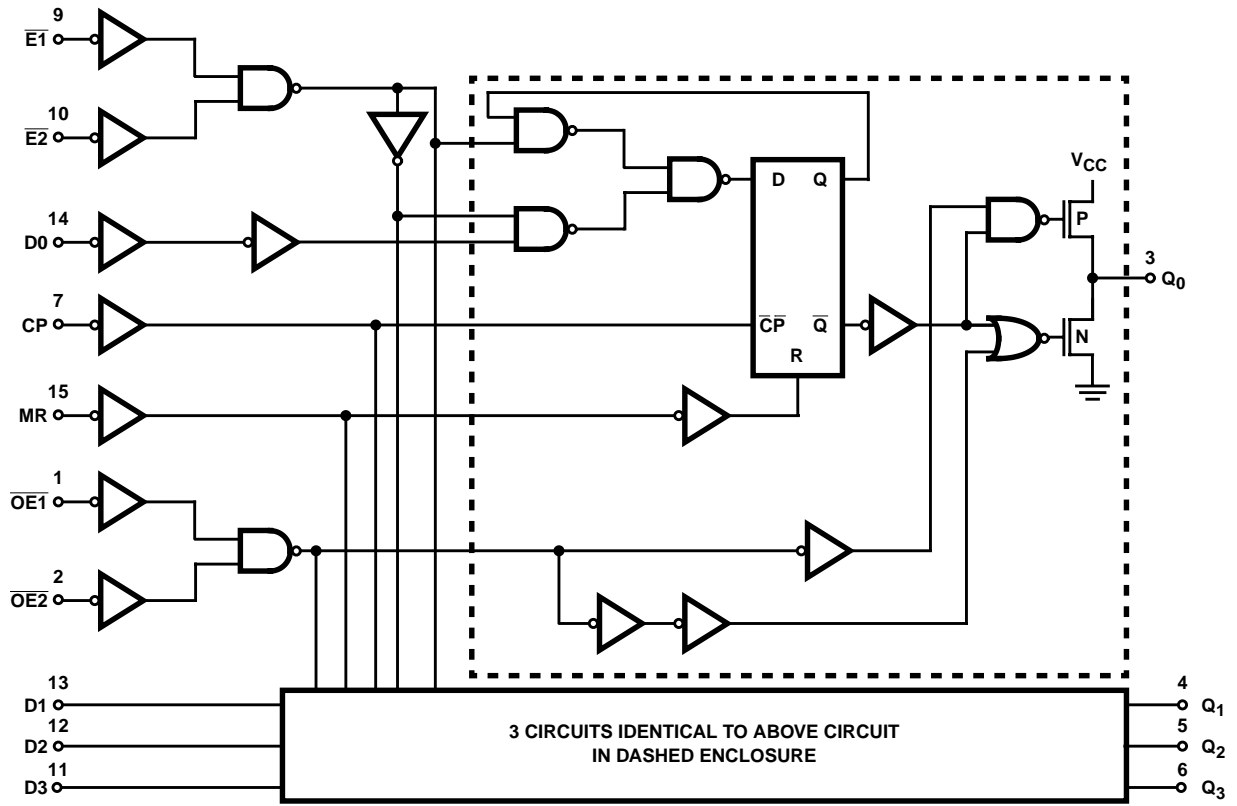
X = Irrelevant

↑ = Transition from Low to High Level

Q_0 = Level Before the Indicated Steady-State Input Conditions Were Established

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Logic Diagram



CD74HC173, CD74HCT173

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 70mA$ |

Thermal Information

| | |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 3) | θ_{JA} (°C/W) |
| PDIP Package | 90 |
| SOIC Package | 160 |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C (SOIC - Lead Tips Only) |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|----------|-------------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |

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DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-----------------|----------------------|------------|--------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | I_{OZ} | V_{IL} or V_{IH} | - | 6 | - | - | ±0.5 | - | ±0.5 | - | ±10 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4) | ΔI_{CC} | V_{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |
| Three-State Leakage Current | I_{OZ} | V_{IL} or V_{IH} | - | 5.5 | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |

NOTE:

4. For dual-supply systems theoretical worst case ($V_I = 2.4V$, $V_{CC} = 5.5V$) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|---------------------------------------|------------|
| D0-D3 | 0.15 |
| $\overline{E1}$ and $\overline{E2}$ | 0.15 |
| CP | 0.25 |
| MR | 0.2 |
| $\overline{OE1}$ and $\overline{OE2}$ | 0.5 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

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Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|--|---------------------|--------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | | |
| Propagation Delay, Clock to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 200 | 250 | 300 | ns |
| | | | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 17 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 34 | 43 | 51 | ns |
| Propagation Delay, MR to Output | t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 12 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 30 | 37 | 45 | ns |
| Propagation Delay Output Enable to Q (Figure 6) | t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH} | $C_L = 50\text{pF}$ | 2 | - | 150 | 190 | 225 | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 12 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 2 | - | 60 | 75 | 90 | ns |
| | | | 4.5 | - | 12 | 15 | 18 | ns |
| | | | 6 | - | 10 | 13 | 15 | ns |
| Maximum Clock Frequency | f_{MAX} | $C_L = 15\text{pF}$ | 5 | 60 | - | - | - | MHz |
| Input Capacitance | C_{IN} | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | C_O | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C_{PD} | - | 5 | 29 | - | - | - | pF |
| HCT TYPES | | | | | | | | |
| Propagation Delay, Clock to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 17 | - | - | - | ns |
| Propagation Delay, MR to Output | t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 44 | 55 | 66 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 18 | - | - | - | ns |
| Propagation Delay Output Enable to Q (Figure 6) | t_{PZL}, t_{PZH} | $C_L = 50\text{pF}$ | 2 | - | 150 | 190 | 225 | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 14 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | 15 | 19 | 22 | ns |
| Maximum Clock Frequency | f_{MAX} | $C_L = 15\text{pF}$ | 5 | 60 | - | - | - | MHz |
| Input Capacitance | C_{IN} | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C_{PD} | - | 5 | 34 | - | - | - | pF |

NOTES:

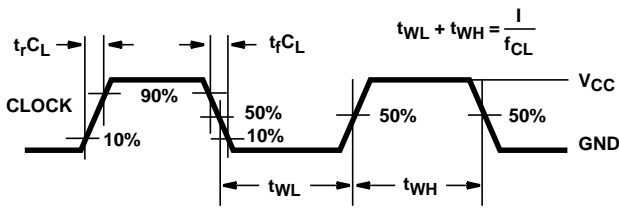
5. C_{PD} is used to determine the dynamic power consumption, per package.
6. $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

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Prerequisite For Switching Specifications

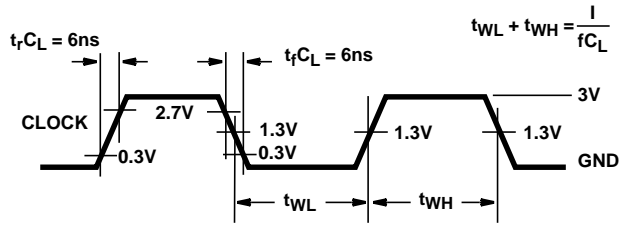
| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| MR Pulse Width | t _w | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Clock Pulse Width | t _w | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Set-up Time, Data to Clock and \bar{E} to Clock | t _{SU} | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| Hold Time, Data to Clock | t _H | 2 | 3 | - | 3 | - | 3 | - | ns |
| | | 4.5 | 3 | - | 3 | - | 3 | - | ns |
| | | 6 | 3 | - | 3 | - | 3 | - | ns |
| Hold Time, \bar{E} to Clock | t _H | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | t _{REM} | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| HCT TYPES | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 4.5 | 20 | - | 16 | - | 13 | - | MHz |
| MR Pulse Width | t _w | 4.5 | 15 | - | 19 | - | 22 | - | ns |
| Clock Pulse Width | t _w | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| Set-up Time, \bar{E} to Clock | t _{SU} | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| Set-up Time, Data to Clock | t _{SU} | 4.5 | 18 | - | 23 | - | 27 | - | ns |
| Hold Time, Data to Clock | t _H | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Hold Time, \bar{E} to Clock | t _H | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | t _{REM} | 4.5 | 12 | - | 15 | - | 18 | - | ns |

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

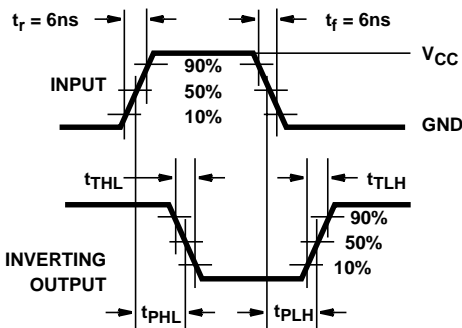


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

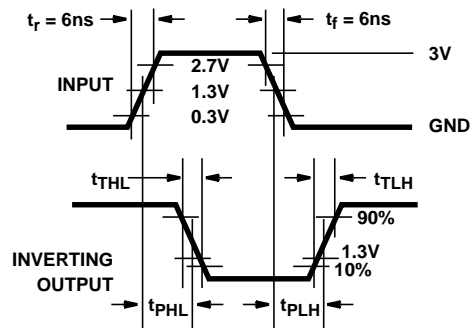


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

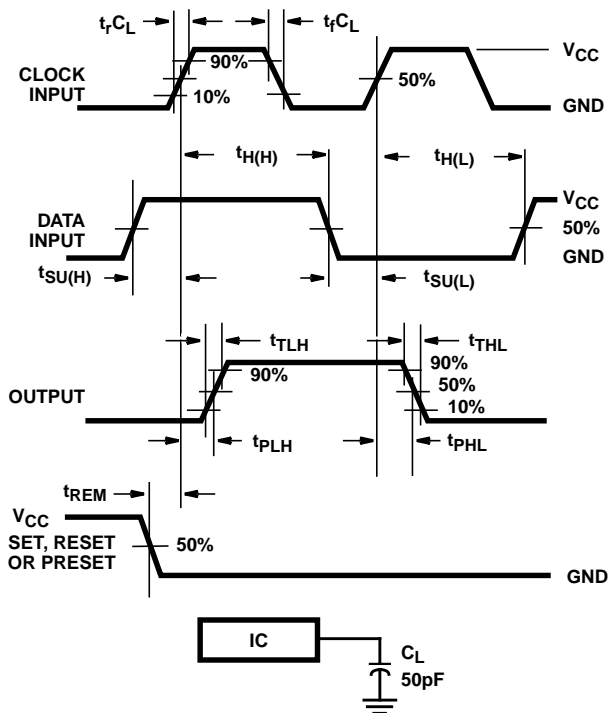


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

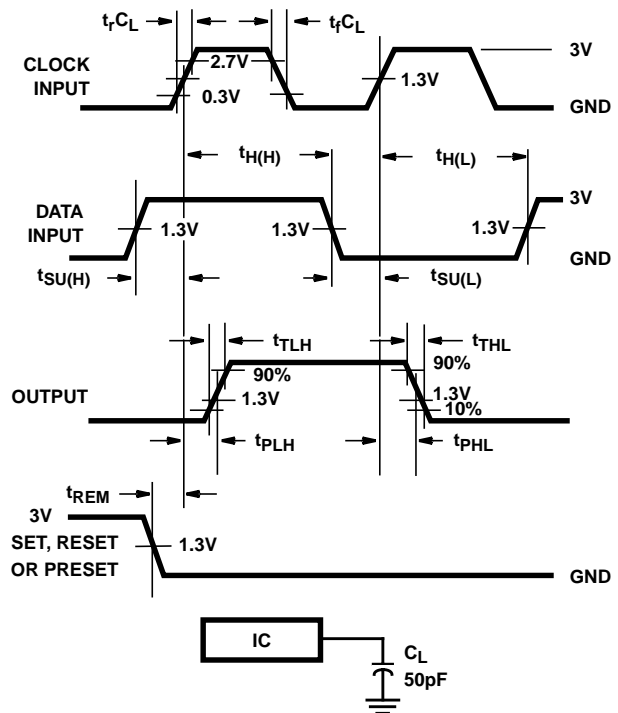


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

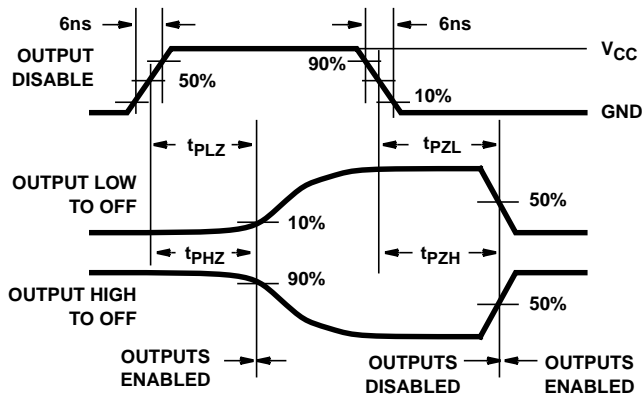


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

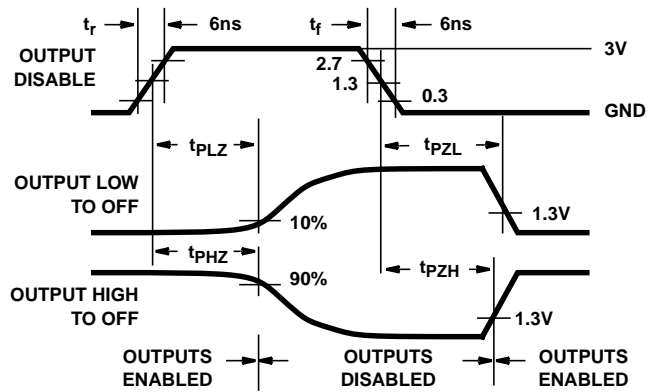
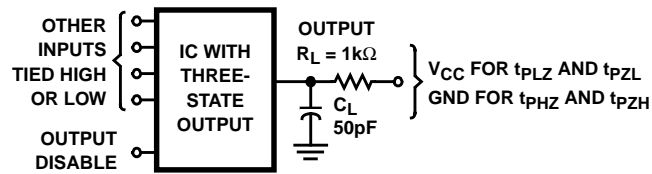


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{pLZ} and t_{pZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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