

# SN54ABT823, SN74ABT823 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS158E – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art EPIC-II<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (NT) and Ceramic (JT) DIPs

## description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

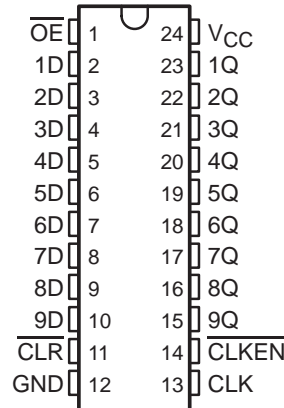
With the clock-enable ( $\overline{\text{CLKEN}}$ ) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high disables the clock buffer, thus latching the outputs. Taking the clear ( $\overline{\text{CLR}}$ ) input low causes the nine Q outputs to go low, independently of the clock.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

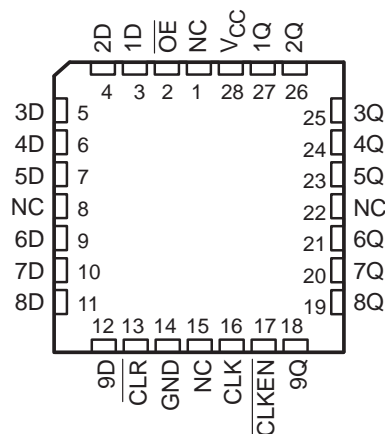
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT823 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT823 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT823 . . . JT OR W PACKAGE  
SN74ABT823 . . . DB, DW, OR NT PACKAGE  
(TOP VIEW)



SN54ABT823 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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**TEXAS  
INSTRUMENTS**

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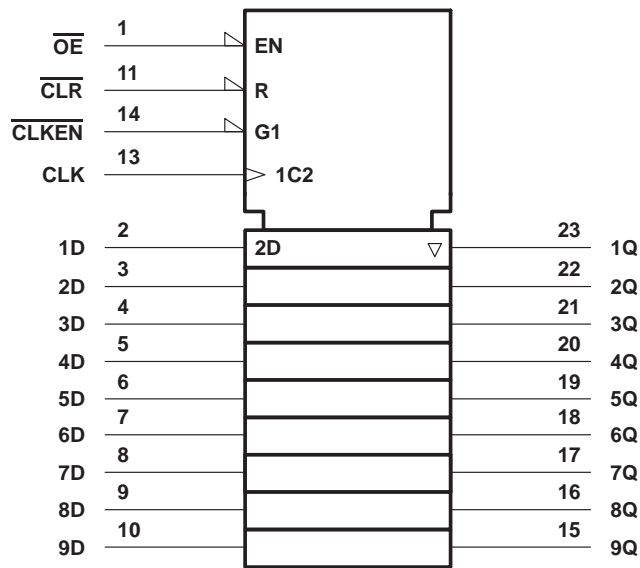
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**WITH 3-STATE OUTPUTS**

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**FUNCTION TABLE**  
 (each flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q <sub>0</sub>
H	X	X	X	X	Z

**logic symbol†**

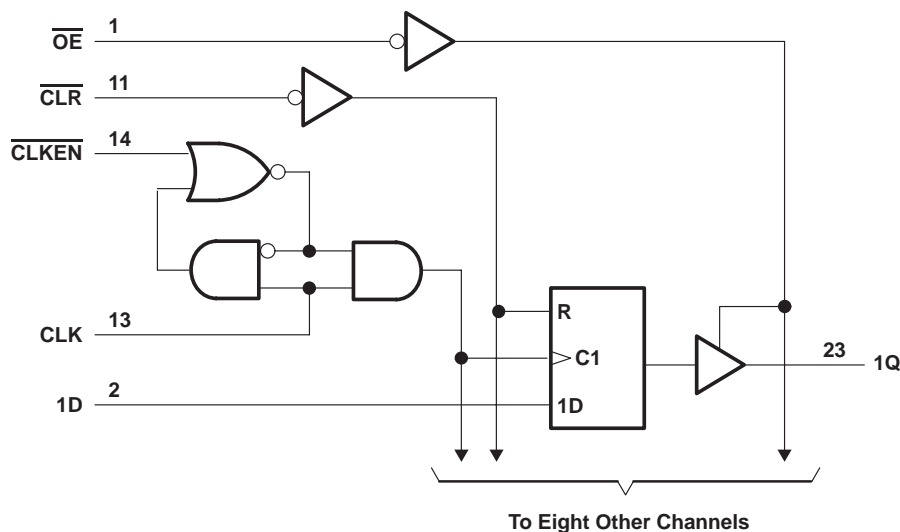


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DB, DW, JT, NT, and W packages.

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## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	.....	-0.5 V to 5.5 V
Current into any output in the low state, $I_{OL}$ : SN54ABT823	.....	96 mA
SN74ABT823	.....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	.....	104°C/W
DW package	.....	81°C/W
NT package	.....	67°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



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## recommended operating conditions (see Note 3)

		SN54ABT823		SN74ABT823		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		5		5	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT823		SN74ABT823		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5		2.5		2.5		V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3		3		3		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA		2		2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -32 mA		2*			2		V
		I <sub>OL</sub> = 48 mA		0.55		0.55			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 64 mA		0.55*			0.55		
				100					mV
V <sub>hys</sub>				100					mV
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>OZPU</sub> ‡	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZPD</sub> ‡	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10§		10§		10§	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10§		-10§		-10§	μA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> ¶	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-50 -140 -180		-50 -180		-50 -180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		1 250		250		250	μA
		Outputs low		24 38		38		38	mA
		Outputs disabled		0.5 250		250		250	μA
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			4					pF
C <sub>O</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			7					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT823		SN74ABT823		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0	125	0	125	MHz
t <sub>w</sub>	Pulse duration	CLR low	5.5	5.5	5.5	5.5	5.5	ns
		CLK high	2.9	2.9	2.9	2.9		
		CLK low	3.8	3.8	3.8	3.8		
t <sub>su</sub>	Setup time before CLK↑	CLR inactive	2.5	2.5	2.5	2.5	ns	
		Data	2.1	2.1	2.1	2.1		
		CLKEN high	2	2	2	2		
		CLKEN low	3.3	3.3	3.3	3.3		
t <sub>h</sub>	Hold time after CLK↑	Data	1.3	1.3	1.3	1.3	ns	
		CLKEN high	1	1	1	1		
		CLKEN low	2	2	2	2		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT823		SN74ABT823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			125	200		125		125	MHz	
t <sub>PLH</sub>	CLK	Q	2.1	4.3	5.9	2.1	8.1	2.1	6.8	ns
t <sub>PHL</sub>			2.2	4.4	6.1	2.2	7	2.2	6.7	
t <sub>PHL</sub>	CLR	Q	2	4.1	6.3	2	7.3	2	7.1	ns
t <sub>PZH</sub>	OE	Q	1	3	4.7†	1	6.3	1	6†	ns
t <sub>PZL</sub>			2.2	4.1	5.6	2.2	6.6	2.2	6.5†	
t <sub>PHZ</sub>	OE	Q	2.7	4.8	6.5†	2.7	7.7	2.7	7.5†	ns
t <sub>PLZ</sub>			1.9	5	6.4	1.9	7.4	1.9	6.9	

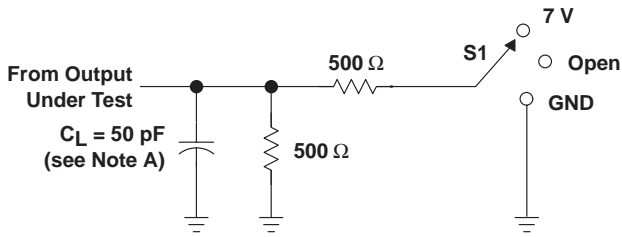
† This data sheet limit may vary among suppliers.



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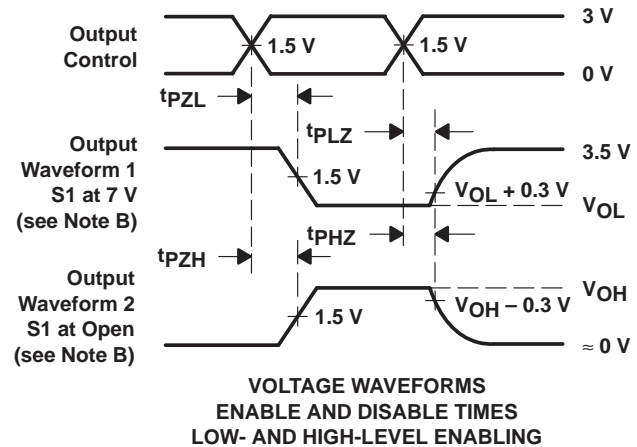
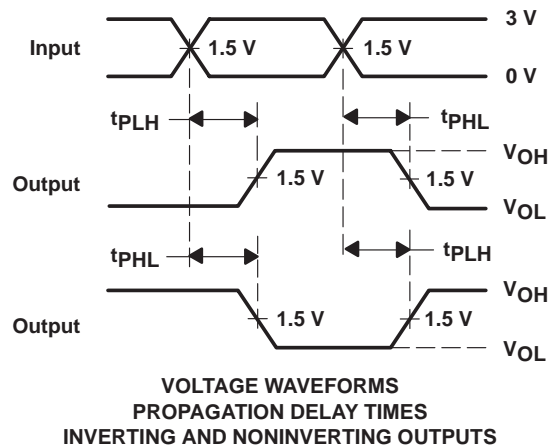
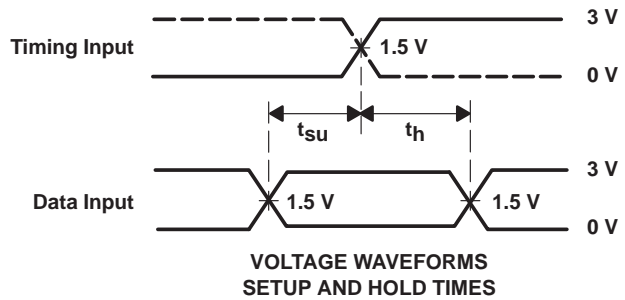
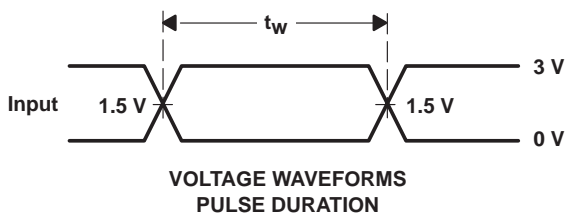
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**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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