

SN54HC574, SN74HC574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS148C – DECEMBER 1982 – REVISED JANUARY 1998

- **High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

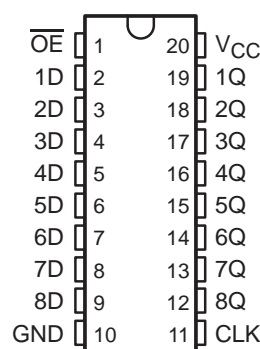
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

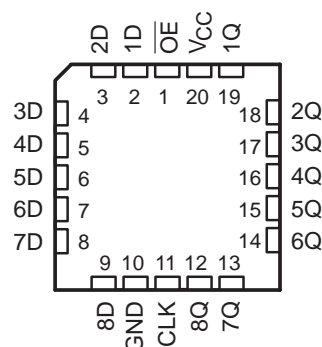
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC574 is characterized for operation from -40°C to 85°C .

SN54HC574 . . . J OR W PACKAGE
SN74HC574 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC574 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z



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**TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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recommended operating conditions (see Note 3)

		SN54HC574			SN74HC574			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0	0.5	0	0.5	V
		V _{CC} = 4.5 V		0	1.35	0	1.35	
		V _{CC} = 6 V		0	1.8	0	1.8	
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V		0	1000	0	1000	ns
		V _{CC} = 4.5 V		0	500	0	500	
		V _{CC} = 6 V		0	400	0	400	
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC574		SN74HC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	6		4		5		MHz
	4.5 V	30		20		24		
	6 V	38		24		28		
t _w Pulse duration, CLK high or low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before CLK↑	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		26		21		
t _h Hold time, data after CLK↑	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	11		4	5	MHz		
			4.5 V	30	36		20	24			
			6 V	36	40		24	28			
t _{pd}	CLK	Any Q	2 V		90	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t _{en}	\overline{OE}	Any Q	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t _{dis}	\overline{OE}	Any Q	2 V		52	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		22	26		38		32	
t _t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6					5		MHz
			4.5 V	30					24		
			6 V	36					28		
t _{pd}	CLK	Any Q	2 V	105		265	400		330		ns
			4.5 V	36		53	80		66		
			6 V	31		46	68		57		
t _{en}	$\overline{\text{OE}}$	Any Q	2 V	95		235	355		295		ns
			4.5 V	32		47	71		59		
			6 V	28		41	60		51		
t _t		Any Q	2 V	60		210	315		265		ns
			4.5 V	17		42	63		53		
			6 V	14		36	53		45		

operating characteristics, T_A = 25°C

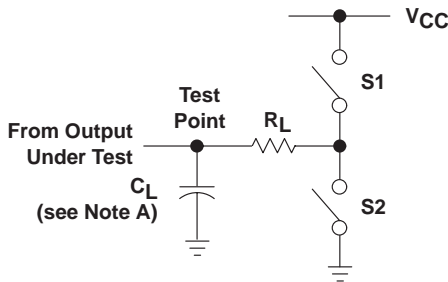
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per flip-flop	No load	100	pF



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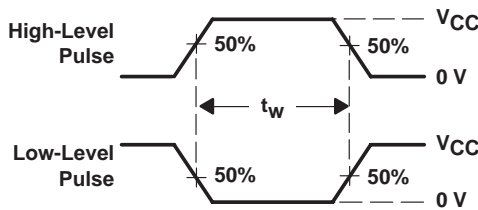
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PARAMETER MEASUREMENT INFORMATION

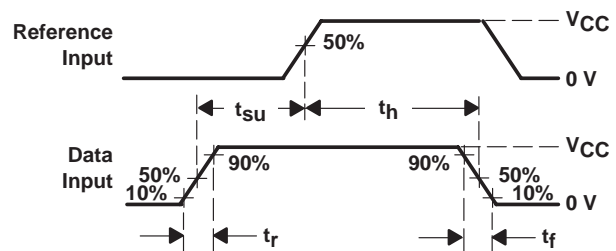


LOAD CIRCUIT

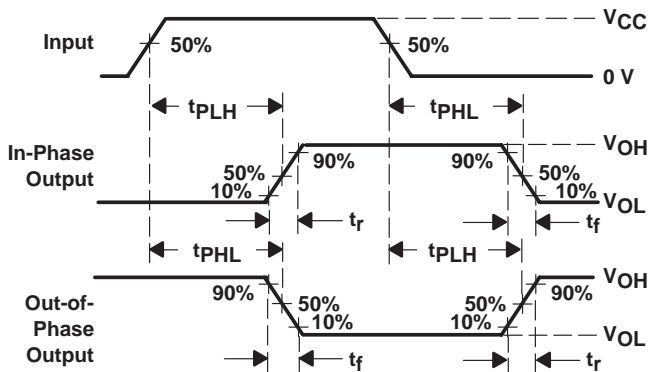
PARAMETER		R_L	C_L	S1	S2
t_{en}	$tpZH$	1 k Ω	50 pF or 150 pF	Open	Closed
	$tpZL$			Closed	Open
t_{dis}	$tpHZ$	1 k Ω	50 pF	Open	Closed
	$tpLZ$			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



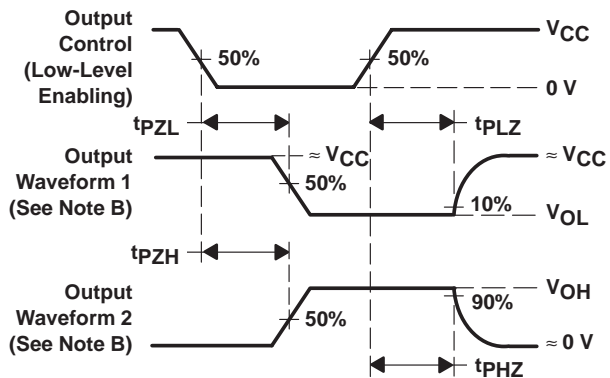
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. $tpLZ$ and $tpHZ$ are the same as t_{dis} .
 G. $tpZL$ and $tpZH$ are the same as t_{en} .
 H. $tpLH$ and $tpHL$ are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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