TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS242

CD74AC175, CD74ACT175

September 1998

Quad D Flip-Flop with Reset

Features

- **Buffered Inputs**
- **Typical Propagation Delay**
  - **6.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**
  - **Drives 50Ω Transmission Lines**

Description

The CD74AC175 and CD74ACT175 are quad D flip-flops with reset that utilize the Harris Advanced CMOS Logic technology. Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a LOW logic level independent of the clock.

Ordering Information

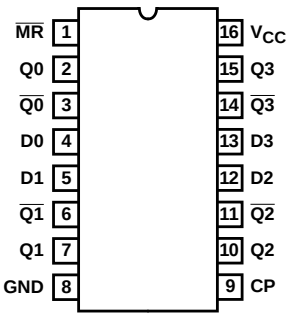
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74AC175E	-55 to 125	16 Ld PDIP	E16.3
CD74ACT175E	-55 to 125	16 Ld PDIP	E16.3
CD74AC175M	-55 to 125	16 Ld SOIC	M16.15
CD74ACT175M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

13. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
14. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

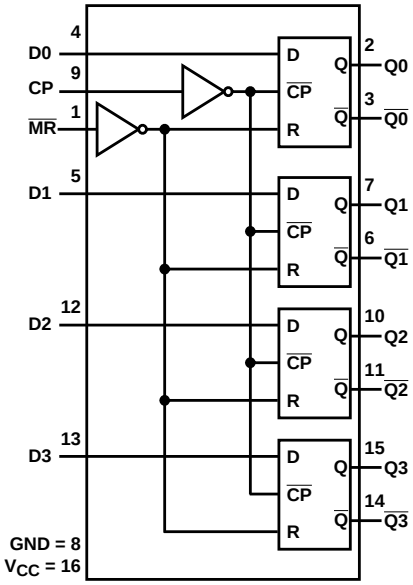
Pinout

CD74AC175, CD74ACT175
(PDIP, SOIC)
TOP VIEW



File Number **1964.1**

Functional Diagram



TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn	$\overline{Qn}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High level
Q0, $\overline{Q0}$ = Level before the Indicated Steady-State Input conditions were established.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) . . . . . ±100mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC} (Note 4)
AC Types. . . . . 1.5V to 5.5V
ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 160
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

15. For up to 4 outputs per device, add ±25mA for each additional output.
16. Unless otherwise specified, all voltages are referenced to ground.
17. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

18. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
19. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
Dn	0.58
$\overline{MR}$	0.67
CP	0.92

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
AC TYPES							
Data to CP Set-Up Time	t_{SU}	1.5	2	-	2	-	ns
		3.3 (Note 8)	2	-	2	-	ns
		5 (Note 9)	2	-	2	-	ns
Hold Time	t_H	1.5	2	-	2	-	ns
		3.3	2	-	2	-	ns
		5	2	-	2	-	ns
Removal Time, $\overline{MR}$ to CP	t_{REM}	1.5	1	-	1	-	ns
		3.3	1	-	1	-	ns
		5	1	-	1	-	ns
$\overline{MR}$ Pulse Width	t_W	1.5	44	-	50	-	ns
		3.3	4.9	-	5.6	-	ns
		5	3.5	-	4	-	ns
CP Pulse Width	t_W	1.5	55	-	63	-	ns
		3.3	6.1	-	7	-	ns
		5	4.4	-	5	-	ns
CP Frequency	f_{MAX}	1.5	9	-	8	-	MHz
		3.3	81	-	71	-	MHz
		5	114	-	100	-	MHz
ACT TYPES							
Data to CP Set-Up Time	t_{SU}	5 (Note 9)	2	-	2	-	ns
Hold Time	t_H	5	2	-	2	-	ns
Removal Time, $\overline{MR}$ to CP	t_{REM}	5	1	-	1	-	ns
$\overline{MR}$ Pulse Width	t_W	5	3.5	-	4	-	ns
Clock Pulse Width	t_W	5	4.4	-	5	-	ns
CP Frequency	f_{MAX}	5	114	-	114	-	MHz

NOTES:

20. 3.3V Min is at 3V.

21. 5V Min is at 4.5V.

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, CP to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	1.5	-	-	139	-	-	153	ns
		3.3 (Note 11)	4.4	-	15.5	4.3	-	17.1	ns
		5 (Note 12)	3.2	-	11.1	3.1	-	12.2	ns

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case) **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, $\overline{MR}$ to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	1.5	-	-	139	-	-	153	ns
		3.3	4.4	-	15.5	4.3	-	17.1	ns
		5	3.2	-	11.1	3.1	-	12.2	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 13)	-	-	55	-	-	55	-	pF
ACT TYPES									
Propagation Delay, CP to Qn	t_{PLH}, t_{PHL}	5 (Note 12)	3	-	10.5	2.9	-	11.5	ns
Propagation Delay, $\overline{MR}$ to Qn	t_{PLH}, t_{PHL}	5	3.3	-	11.8	3.3	-	13	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 13)	-	-	55	-	-	55	-	pF

NOTES:

22. Limits tested 100%.
23. 3.3V Min is at 3.6V, Max is at 3V.
24. 5V Min is at 5.5V, Max is at 4.5V.
25. C_{PD} is used to determine the dynamic power consumption per flip-flop. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + V_{CC}2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

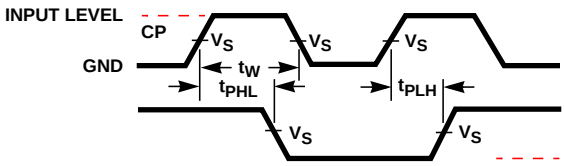


FIGURE 5. PROPAGATION DELAYS

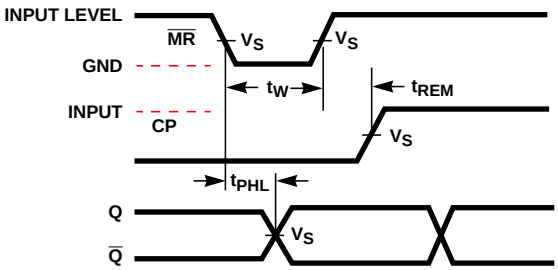


FIGURE 6. $\overline{RESET}$ OR $\overline{SET}$ PREREQUISITE AND PROPAGATION DELAYS

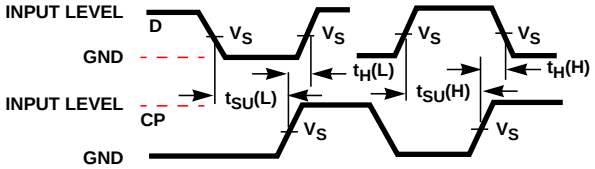
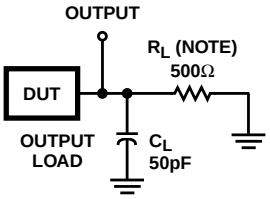


FIGURE 7.



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

	CD74AC	CD74ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

FIGURE 8. PROPAGATION DELAY TIMES

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