

### Features

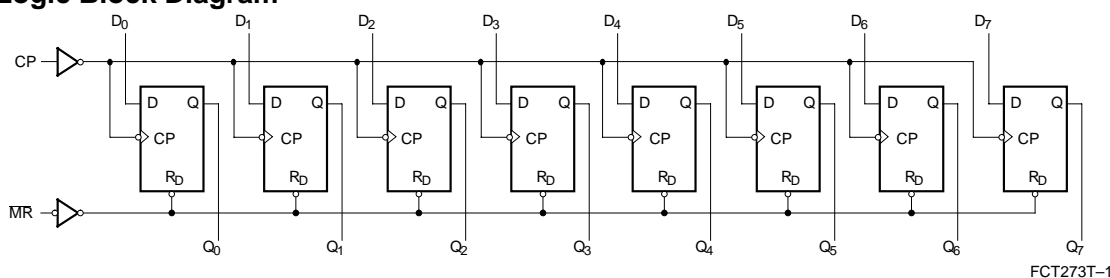
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.8 ns max. (Com'l)  
FCT-A speed at 7.2 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Sink current                    64 mA (Com'l), 32 mA (Mil)  
Source current                 32 mA (Com'l), 12 mA (Mil)

### Functional Description

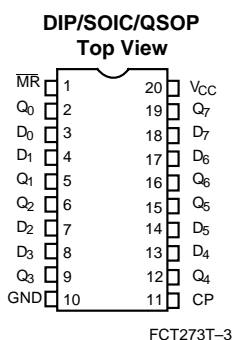
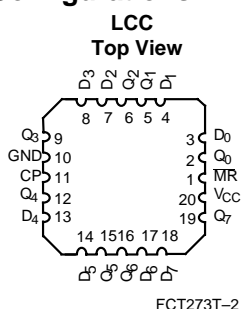
The FCT273T consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset (MR) load and reset all flip-flops simultaneously. The FCT273T is an edge-triggered register. The state of each D input (one set-up time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flop's Q output. All outputs will be forced LOW by a low voltage level on the  $\overline{\text{MR}}$  input.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

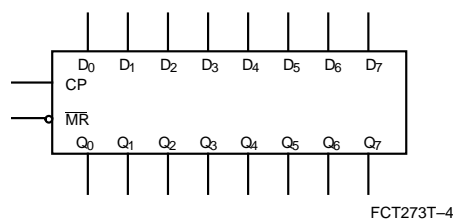
### Logic Block Diagram



### Pin Configurations



### Logic Symbol



### Function Table<sup>[1]</sup>

Operating Mode	Inputs			Output
	$\overline{\text{MR}}$	CP	D	Q
Reset (clear)	L	X	X	L
Load '1'	H	┐	h	H
Load '0'	H	┐	l	L

#### Note:

1. H = HIGH Voltage Level steady state  
h = HIGH Voltage Level one set-up time prior to LOW-to-HIGH clock transition  
L = LOW Voltage Level steady state  
l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH transition  
X = Don't Care  
┐ = LOW-to-HIGH clock transition

**Maximum Ratings**<sup>[2, 3]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-65°C to +135°C
Supply Voltage to Ground Potential.....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage .....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin).....	120 mA
Power Dissipation .....	0.5W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	All	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	Com'l	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =32mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA			-0.7	-1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V				±1	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V		-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V				±1	μA

**Capacitance**<sup>[6]</sup>

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN} \leq 0.2V, V_{IN} \geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}, V_{IN}=3.4V, f_1=0, \text{Outputs Open}^{[8]}$	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[9]</sup>	$V_{CC}=\text{Max.}, \text{One Bit Toggling, 50\% Duty Cycle, Outputs Open, } \overline{MR}=V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
$I_C$	Total Power Supply Current <sup>[10]</sup>	$V_{CC}=\text{Max.}, f_0=10 \text{ MHz, 50\% Duty Cycle, Outputs Open, One Bit Toggling at } f_1=5 \text{ MHz, } \overline{MR}=V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz, 50\% Duty Cycle, Outputs Open, One Bit Toggling at } f_1=5 \text{ MHz, } \overline{MR}=V_{CC}, V_{IN}=3.4V \text{ or } V_{IN}=\text{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz, 50\% Duty Cycle, Outputs Open, Eight Bits Toggling at } f_1=2.5\text{MHz, } \overline{MR}=V_{CC}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	1.6	3.2 <sup>[11]</sup>	mA
		$V_{CC}=\text{Max.}, f_0=10 \text{ MHz, 50\% Duty Cycle, Outputs Open, Eight Bits Toggling at } f_1=2.5 \text{ MHz, } \overline{MR}=V_{CC}, V_{IN}=3.4V \text{ or } V_{IN}=\text{GND}$	3.9	12.2 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	FCT273T		FCT273AT				Unit	Fig. No. <sup>[13]</sup>
		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Output	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{MR}$ to Output	2.0	13.0	2.0	8.3	2.0	7.2	ns	1, 6
$t_S$	Set-Up Time HIGH or LOW D to Clock	2.0		2.0		2.0		ns	4
$t_H$	Hold Time HIGH or LOW D to Clock	1.5		1.5		1.5		ns	4
$t_W$	Clock Pulse Width HIGH or LOW	6.0		6.0		6.0		ns	5
$t_W$	$\overline{MR}$ Pulse Width LOW	6.0		6.0		6.0		ns	6
$t_{REC}$	Recovery Time $\overline{MR}$ to Clock	2.0		2.5		2.0		ns	6

Parameter	Description	FCT273CT		Unit	Fig. No. <sup>[13]</sup>
		Commercial			
		Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Output	2.0	5.8	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{MR}$ to Output	2.0	6.1	ns	1, 6
$t_S$	Set-Up Time HIGH or LOW D to Clock	2.0		ns	4
$t_H$	Hold Time HIGH or LOW D to Clock	1.5		ns	4
$t_W$	Clock Pulse Width HIGH or LOW	6.0		ns	5
$t_W$	$\overline{MR}$ Pulse Width LOW	6.0		ns	6
$t_{REC}$	Recovery Time $\overline{MR}$ to Clock	2.0		ns	6

**Ordering Information**

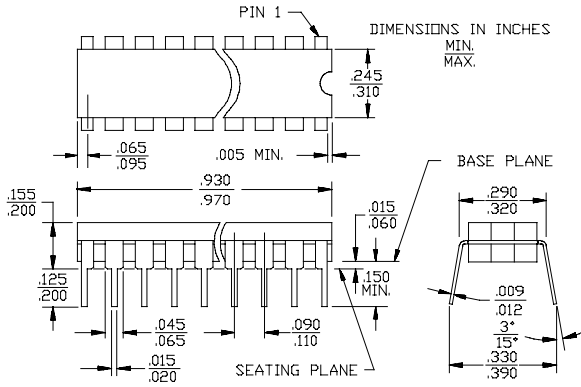
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT273CTQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT273CTSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY74FCT273ATQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT273ATSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
8.3	CY54FCT273ATLMB	L61	20-Square Leadless Chip Carrier	Military
	CY54FCT273ATDMB	D6	20-Lead (300-Mil) CerDIP	
13.0	CY74FCT273TQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT273TSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	

**Notes:**

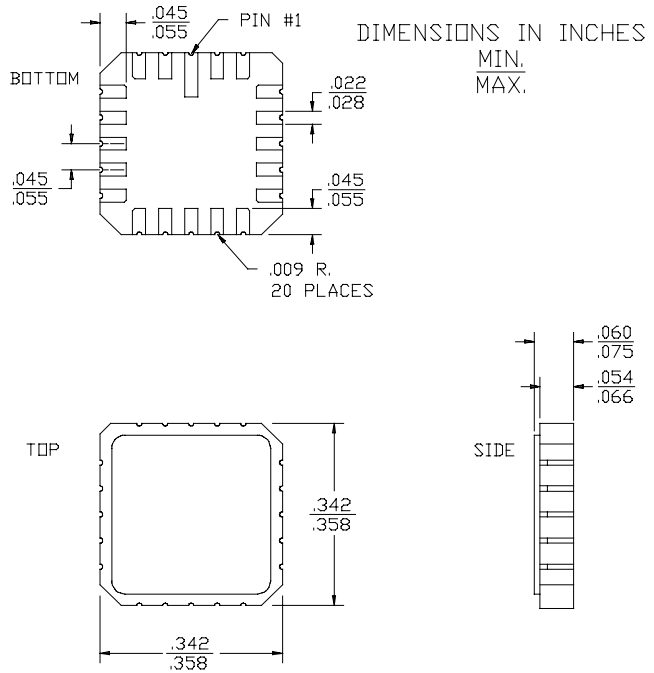
12. Minimum limits are specified but not tested on Propagation Delays.  
13. See "Parameter Measurement Information" in the General Information section.

**Package Diagrams**

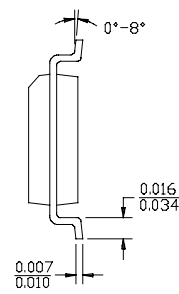
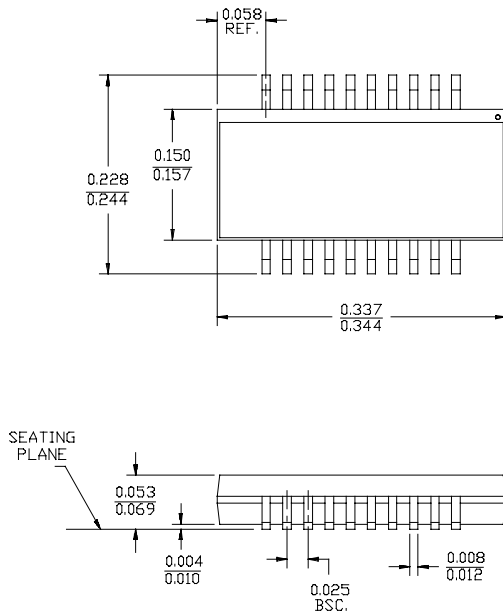
**20-Lead (300-Mil) CerDIP D6**  
MIL-STD-1835 D- 8 Config.A



**20-Pin Square Leadless Chip Carrier L61**  
MIL-STD-1835 C-2A



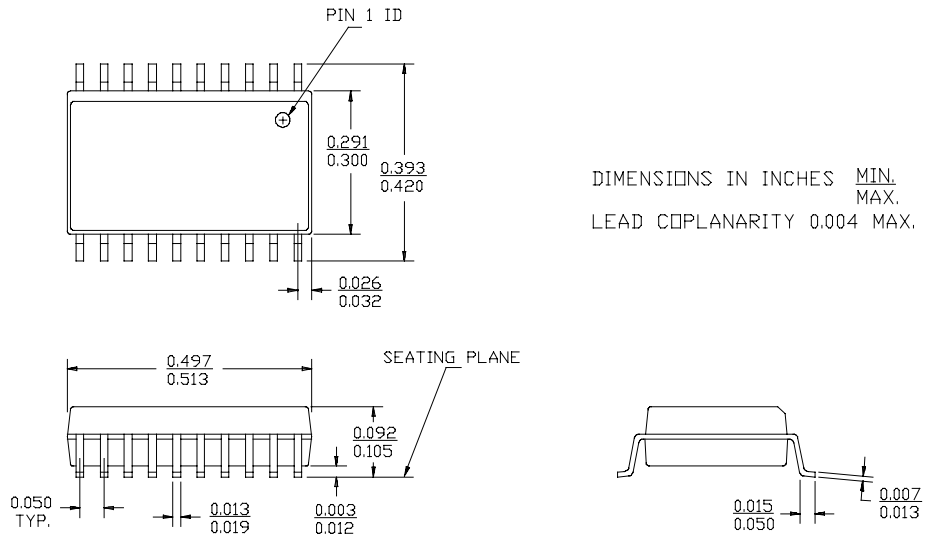
**20-Lead Quarter Size Outline Q5**



DIMENSIONS IN INCHES MIN. MAX.  
LEAD COPLANARITY 0.004 MAX.

Package Diagrams (continued)

20-Lead (300-Mil) Molded SOIC S5



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