## - Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ( $\overline{\mathrm{PRE})}$ or clear ( $\overline{\mathrm{CLR})}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and $\overline{C L R}$ are inactive (high), data at the $J$ and $\overline{\mathrm{K}}$ input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{\mathrm{K}}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{\mathrm{K}}$ and trying J high. They also can perform as D-type flip-flops if $J$ and $\bar{K}$ are tied together.
The SN54F109 is characterized for operation over the full military temperature range of $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$. The SN74F109 is characterized for operation from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.

## SN54F109 . . . J PACKAGE SN74F109... D OR N PACKAGE (TOP VIEW)

| $1 \overline{\mathrm{CLR}}$ | U |  |
| :---: | :---: | :---: |
|  | 16 |  |
| 1J 2 | 215 | 2CLR |
| 1 K [ 3 | 314 | 2 J |
| 1CLK 4 | 413 | $2 \bar{K}$ |
| 1PRE 5 | 512 | 2CLK |
| 1Q 6 | 611 | $2 \overline{\text { PRE }}$ |
| 1 $\bar{Q}$ | 710 | 2Q |
| GND [8 | 89 | $2 \bar{Q}$ |

SN54F109... FK PACKAGE (TOP VIEW)


NC - No internal connection

FUNCTION TABLE

| INPUTS |  |  |  |  | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\text { PRE }}$ | $\overline{\text { CLR }}$ | CLK | J | $\overline{\text { K }}$ | Q | $\overline{\mathbf{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | $\mathrm{H}^{\dagger}$ | $\mathrm{H}^{\dagger}$ |
| H | H | $\uparrow$ | L | L | L | H |
| H | H | $\uparrow$ | H | L | Toggle |  |
| H | H | $\uparrow$ | L | H | $\mathrm{Q}_{0}$ | $\bar{Q}_{0}$ |
| H | H | $\uparrow$ | H | H | H | L |
| H | H | L | X | X | $\mathrm{Q}_{0}$ | $\bar{Q}_{0}$ |

$\dagger$ The output levels are not guaranteed to meet the minimum levels for $\mathrm{V}_{\mathrm{OH}}$. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{P R E}$ or $\overline{C L R}$ returns to its inactive (high) level.

## logic symbol $\dagger$


$\dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the $\mathrm{D}, \mathrm{J}$, and N packages.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\ddagger$

| Supply voltage range, $\mathrm{V}_{\mathrm{CC}}$ | -0.5 V to 7 V |
| :---: | :---: |
| Input voltage range, $\mathrm{V}_{1}$ (see Note 1) | -1.2 V to 7 V |
| Input current range | -30 mA to 5 mA |
| Voltage range applied to any output in the high state | -0.5 V to $\mathrm{V}_{\mathrm{CC}}$ |
| Current into any output in the low state | 40 mA |
| Operating free-air temperature range: SN54F109 | $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ |
| SN74F109 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |

$\ddagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.
recommended operating conditions

|  |  | SN54F109 |  |  | SN74F109 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  | 0.8 |  |  | 0.8 | V |
| IIK | Input clamp current |  |  | -18 |  |  | -18 | mA |
| ${ }^{\text {IOH }}$ | High-level output current |  |  | -1 |  |  | -1 | mA |
| ${ }^{\text {IOL }}$ | Low-level output current |  |  | 20 |  |  | 20 | mA |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

# SN54F109, SN74F109 <br> DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET <br> SDFS047A - MARCH 1987 - REVISED OCTOBER 1993 

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS |  | SN54F109 |  |  | SN74F109 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP $\dagger$ | MAX | MIN | TYP† | MAX |  |
| VIK |  |  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$, | $1 \mathrm{l}=-18 \mathrm{~mA}$ |  |  | -1.2 |  |  | -1.2 | V |
| $\mathrm{V}_{\mathrm{OH}}$ |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$, | $\mathrm{IOH}=-1 \mathrm{~mA}$ | 2.5 | 3.4 |  | 2.5 | 3.4 |  | V |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}$, | $\mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA}$ |  |  |  | 2.7 |  |  |  |
| $\mathrm{V}_{\text {OL }}$ |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$, | $\mathrm{l} \mathrm{OL}=20 \mathrm{~mA}$ |  | 0.3 | 0.5 |  | 0.3 | 0.5 | V |
| 1 |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  | 0.1 |  |  | 0.1 | mA |
| ${ }^{\text {IIH }}$ |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  | 20 |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | J, $\overline{\mathrm{K}}, \mathrm{CLK}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}$ | -0.6 |  |  | -0.6 |  |  | mA |
|  | $\overline{\text { PRE }}$ or $\overline{\mathrm{CLR}}$ |  |  |  |  | -1.8 |  |  | -1.8 |  |
| los ${ }^{\ddagger}$ |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{O}}=0$ | -60 |  | -150 | -60 |  | -150 | mA |
| ICC |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | See Note 2 |  | 11.7 | 17 |  | 11.7 | 17 | mA |

$\dagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
$\ddagger$ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: ICC is measured with $\mathrm{J}, \overline{\mathrm{K}}, \mathrm{CLK}$, and $\overline{\mathrm{PRE}}$ grounded then with $\mathrm{J}, \overline{\mathrm{K}}, \mathrm{CLK}$, and $\overline{\mathrm{CLR}}$ grounded.
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

|  |  |  | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \hline \text { 'F74 } \end{gathered}$ |  | SN54F109 |  | SN74F109 |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {clock }}$ | Clock frequency |  | 0 | 100 | 0 | 70 | 0 | 90 | MHz |
| $\mathrm{t}_{\text {w }}$ | Pulse duration | CLK high, $\overline{\text { PRE }}$ or $\overline{\mathrm{CLR}}$ low | 4 |  | 4 |  | 4 |  | ns |
|  |  | CLK low | 5 |  | 5 |  | 5 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time, data before CLK $\uparrow$ | High | 3 |  | 3 |  | 3 |  | ns |
|  |  | Low | 3 |  | 3 |  | 3 |  |  |
|  | Setup time, inactive-state before CLK $\uparrow \S$ | $\overline{\text { PRE }}$ or $\overline{C L R}$ to CLK | 2 |  | 2 |  | 2 |  |  |
|  | Hold time, data after CLK $\uparrow$ | High | 1 |  | 1 |  | 1 |  | ns |
|  |  | Low | 1 |  | 1 |  | 1 |  |  |

§ Inactive-state setup time is also referred to as recovery time.
switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | то (OUTPUT) | $$ |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \\ & \mathrm{R}_{\mathrm{L}}=500 \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{MIN} \text { to MAXII } \end{aligned}$ |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | SN5 | 109 | SN74 | 109 |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX | MIN | MAX |  |
| $f_{\text {max }}$ |  |  | 100 | 150 |  | 70 |  | 90 |  | MHz |
| tPLH | CLK | Q or $\overline{\mathrm{Q}}$ | 3 | 4.9 | 7 | 3 | 9 | 3 | 8 | ns |
| tPHL |  |  | 3.6 | 5.8 | 8 | 3.6 | 10.5 | 3.6 | 9.2 |  |
| tPLH | $\overline{\text { PRE or }} \overline{\text { CLR }}$ | Q or $\overline{\mathrm{Q}}$ | 2.4 | 4.8 | 7 | 2.4 | 9 | 2.4 | 8 | ns |
| tPHL |  |  | 2.7 | 6.6 | 9 | 2.7 | 11.5 | 2.7 | 10.5 |  |

[^0]
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[^0]:    II For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.

