

# SN54HC174, SN74HC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS119B – DECEMBER 1982 – REVISED MAY 1997

- Contain Six Flip-Flops With Single-Rail Outputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

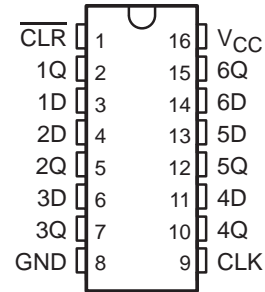
## description

These monolithic positive-edge-triggered D-type flip-flops have a direct clear ( $\overline{\text{CLR}}$ ) input.

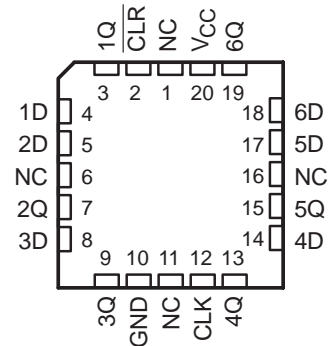
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54HC174 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC174 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC174 . . . J OR W PACKAGE  
SN74HC174 . . . D OR N PACKAGE  
(TOP VIEW)



SN54HC174 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

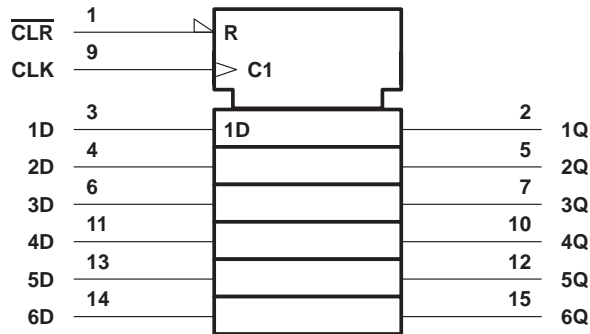
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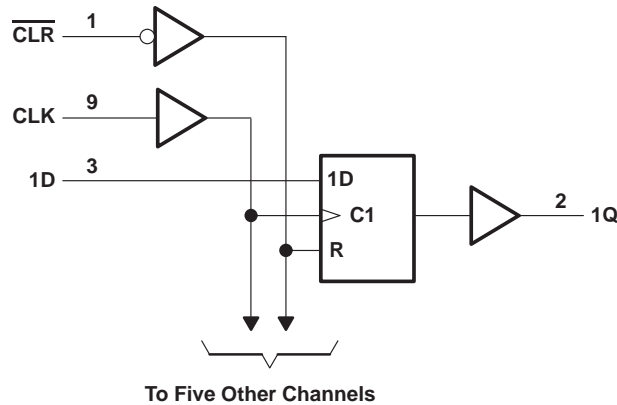
SCLS119B – DECEMBER 1982 – REVISED MAY 1997

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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SCLS119B – DECEMBER 1982 – REVISED MAY 1997

## recommended operating conditions

		SN54HC174			SN74HC174			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0	0.5	0	0.5	V
		V <sub>CC</sub> = 4.5 V		0	1.35	0	1.35	
		V <sub>CC</sub> = 6 V		0	1.8	0	1.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V		0	1000	0	1000	ns
		V <sub>CC</sub> = 4.5 V		0	500	0	500	
		V <sub>CC</sub> = 6 V		0	400	0	400	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF



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SCLS119B – DECEMBER 1982 – REVISED MAY 1997

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC174		SN74HC174		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t <sub>w</sub>	Pulse duration	CLR low	2 V	80		120		100	ns
			4.5 V	16		24		20	
			6 V	14		20		17	
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t <sub>su</sub>	Data	Data	2 V	100		150		125	ns
			4.5 V	20		30		25	
			6 V	17		25		21	
	CLR inactive	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t <sub>h</sub>	Hold time, data after CLK↑		2 V	0		0		0	ns
			4.5 V	0		0		0	
			6 V	0		0		0	

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	9		4.2		5	MHz	
			4.5 V	31	44		21		25		
			6 V	36	50		25		29		
t <sub>pd</sub>	CLR	Any	2 V		58	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	CLK	Any	2 V		58	160		240		200	
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t <sub>t</sub>		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

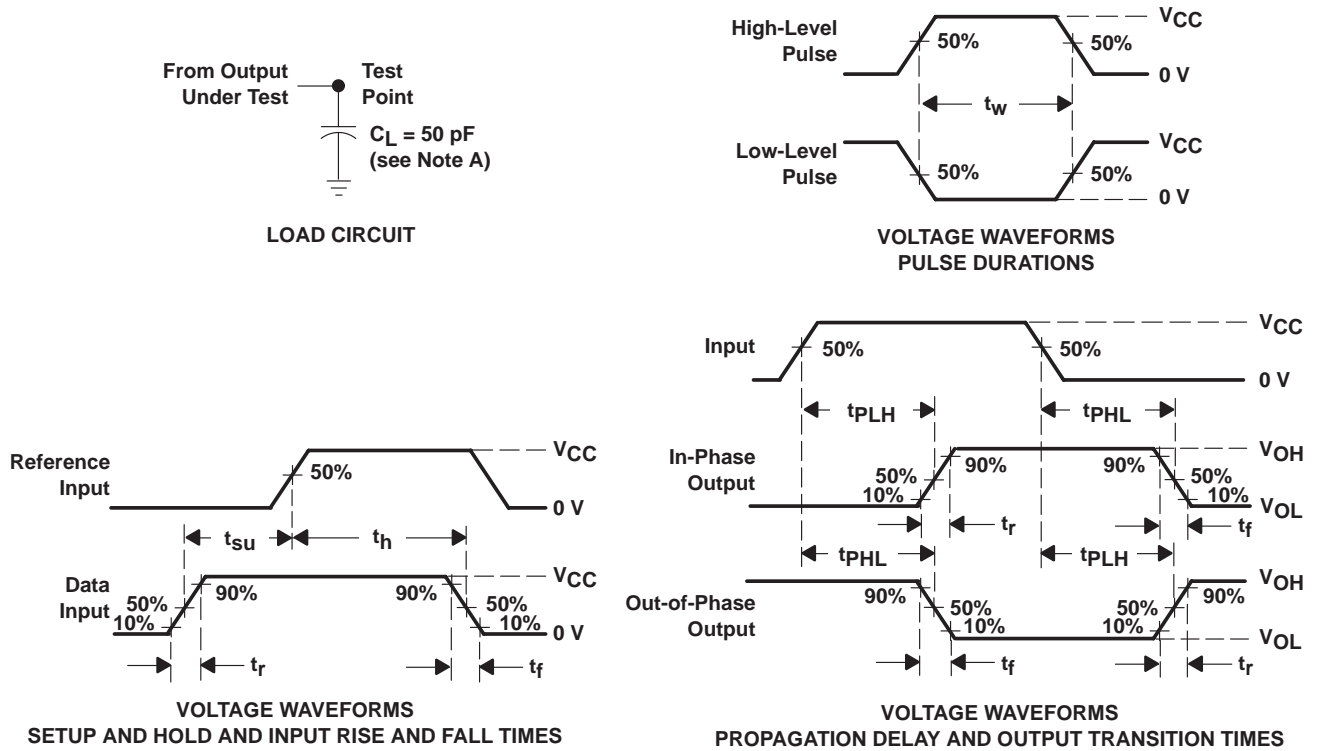
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per flip-flop	No load	27	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .  
 C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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