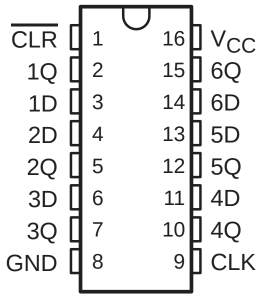
SN74F174A
HEX D-TYPE FLIP-FLOP
WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Contains Six Flip-Flops With Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Fully Buffered Outputs for Maximum Isolation From External Disturbances**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

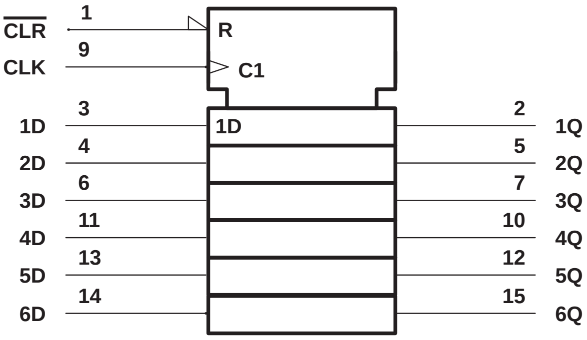
This monolithic, positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

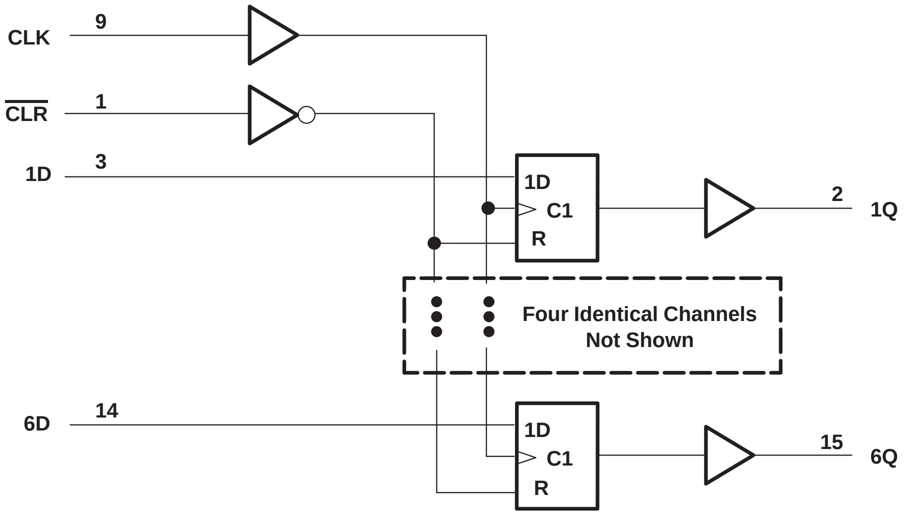
INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
H	L	X	Q_0
H	↑	H	H
H	↑	L	L
L	X	X	L

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 1 mA	2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = – 1 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	– 60		– 150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 2		30	45	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 3		39	55	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTES: 2. I_{CCH} is measured with all outputs open, all data inputs and enable input at 4.5 V, and the clock input at 4.5 V after being momentarily grounded.

3. I_{CCL} is measured with all outputs open, all data inputs and enable input at 0 V, and the clock input at 4.5 V after being momentarily grounded.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	80	MHz
t_w	Pulse duration	CLK high	4		4		ns
		CLK low	6		6		
		$\overline{\text{CLR}}$ low	5		5		
t_{su}	Setup time before CLK↑	Data high or low	4.5		4.5		ns
		$\overline{\text{CLR}}$ high¶	5		5		
t_h	Hold time after CLK↑	Data high or low	0.5		1		ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

¶ Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	140		80		MHz
t_{PLH}	CLK	Any Q	2.7	4.5	8	2.7	9	ns
t_{PHL}			3.4	4.2	10	3.3	11	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	4.2	6.3	14	4.2	15	ns

NOTE 4: Load circuits and waveforms are shown in Section 1.

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