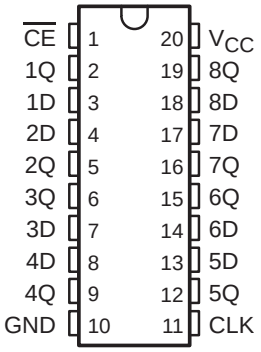
SN74F377A
OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE

SDFS018D – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Contains Eight D-Type Flip-Flops With Single-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Buffered Common Enable Input**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The SN74F377A is a monolithic, positive-edge-triggered, octal, D-type flip-flop with clock enable inputs. The SN74F377A features a latched clock enable ($\overline{CE}$) input.

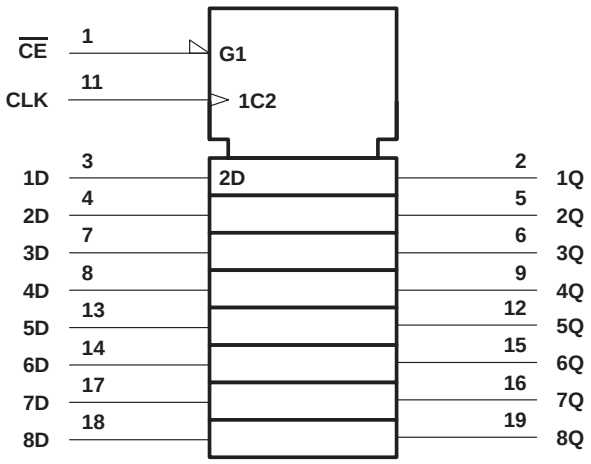
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{CE}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{CE}$ input.

The SN74F377A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

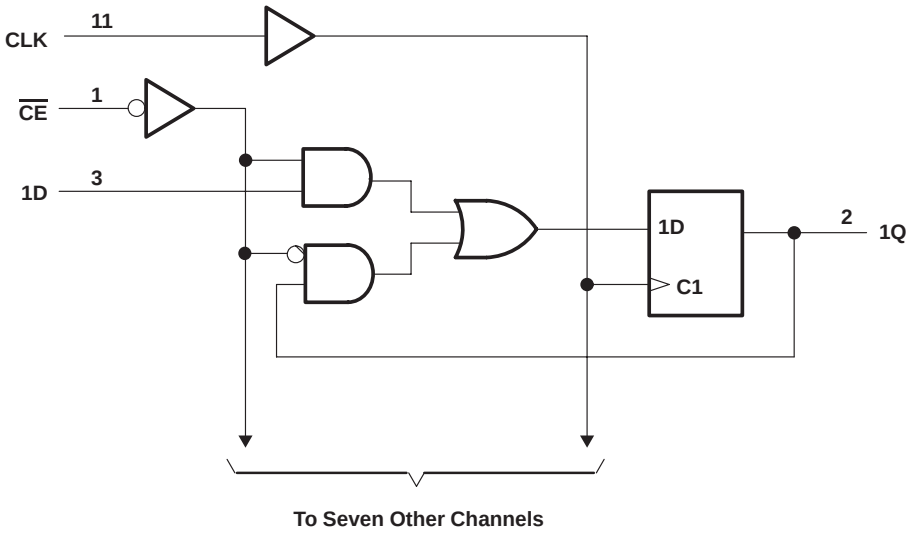
INPUTS			OUTPUT
$\overline{CE}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			– 18	mA
I_{OH}	High-level output current			– 1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 1 mA	2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = – 1 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I	V_{CC} = 0,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	– 60		– 150	mA
I_{CCH}	V_{CC} = 5.5 V,	See Note 2		55	72	mA
I_{CCL}	V_{CC} = 5.5 V,	See Note 3		70	90	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTES: 2. I_{CCH} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the enable input at GND.
3. I_{CCL} is measured after applying a momentary ground, then 4.5 V, to the clock input with all data and enable inputs at GND.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	110	0	110	MHz
t_w	Pulse duration		4		5		ns
t_{su}	Setup time before CLK↑	Data high or low	2		2		ns
		$\overline{CE}$ high	2.5		2.5		
		$\overline{CE}$ low	4		4.5		
t_h	Hold time after CLK↑	Data high or low	1		1		ns
		$\overline{CE}$ high or low	0		0		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			110	125		110		MHz
t_{PLH}	CLK	Any Q	4	6.5	8.5	4	10	ns
t_{PHL}			4	7	9	4	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: Load circuit and waveforms are shown in Section 1.

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