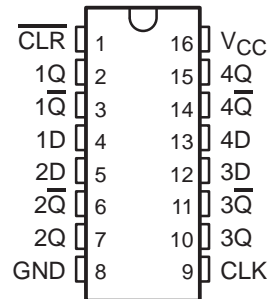


SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

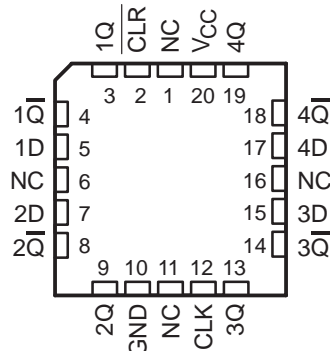
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- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Applications Include:**
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV175A . . . J OR W PACKAGE
SN74LV175A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV175A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LV175A devices are quadruple D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices have a direct clear ($\overline{\text{CLR}}$) input and feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54LV175A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV175A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\overline{Q}_0



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 **TEXAS
INSTRUMENTS**

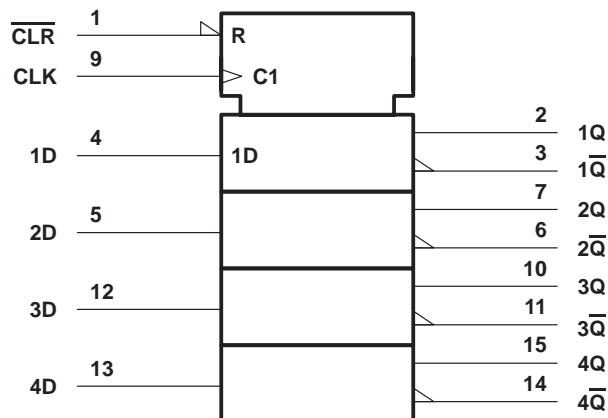
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SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

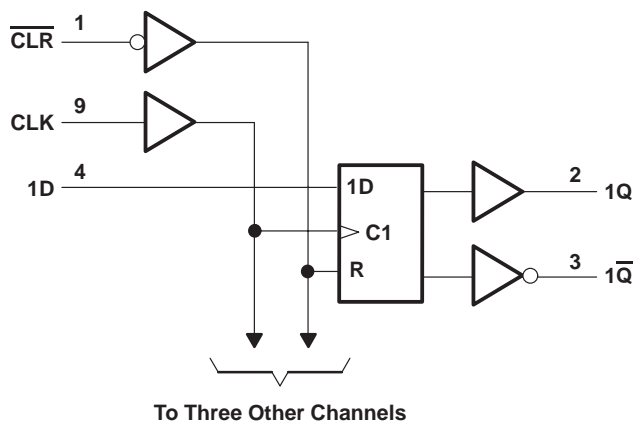
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
NS package	111°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LV175A		SN74LV175A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2	5.5	2	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5		V	
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V	
I_{OH}	High-level output current	$V_{CC} = 2$ V	–50	–50		μ A	
		$V_{CC} = 2.3$ V to 2.7 V	–2	–2		mA	
		$V_{CC} = 3$ V to 3.6 V	–6	–6			
		$V_{CC} = 4.5$ V to 5.5 V	–12	–12			
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	50		μ A	
		$V_{CC} = 2.3$ V to 2.7 V	2	2		mA	
		$V_{CC} = 3$ V to 3.6 V	6	6			
		$V_{CC} = 4.5$ V to 5.5 V	12	12			
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature	–55	125	–40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV175A			SN74LV175A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	1.4			1.4			pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	6	6	6	6	6	ns
		CLK high or low	6.5	7	7	7		
t _{su}	Setup time before CLK↑	Data	7	7.5	7.5	7.5	ns	
		CLR inactive	7	7.5	7.5	7.5		
t _h	Hold time, data after CLK↑	0.5	1	1	1	ns		

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5	5	5	5	ns	
		CLK high or low	5	5	5	5		
t _{su}	Setup time before CLK↑	Data	5	5	5	5	ns	
		CLR inactive	5	5	5	5		
t _h	Hold time, data after CLK↑	1	1	1	1	ns		

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SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time before CLK \uparrow	Data	4		4		4		ns
		CLR inactive	5		5		5		
t_h	Hold time, data after CLK \uparrow		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	50	105		45		45	MHz	
			$C_L = 50\text{ pF}$	40	80		35		35		
t_{pd}^*	CLR	Any	$C_L = 15\text{ pF}$	7.9	16.6		1	20	1	20	ns
	CLK	Any		9.3	18.8		1	22	1	22	
t_{pd}	CLR	Any	$C_L = 50\text{ pF}$	10.4	21.6		1	25.5	1	25.5	ns
	CLK	Any		12	23.3		1	27	1	27	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	90	155		75		75	MHz	
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}^*	CLR	Any	$C_L = 15\text{ pF}$	5.5	10.1		1	12	1	12	ns
	CLK	Any		6.5	11.5		1	13.5	1	13.5	
t_{pd}	CLR	Any	$C_L = 50\text{ pF}$	7.4	13.6		1	15.5	1	15.5	ns
	CLK	Any		8.4	15		1	17	1	17	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}^*$	150	215		125		125	MHz	
			$C_L = 50\text{ pF}$	85	165		75		75		
t_{pd}^*	CLR	Any	$C_L = 15\text{ pF}$	3.7	6.4		1	7.5	1	7.5	ns
	CLK	Any		4.6	7.3		1	8.5	1	8.5	
t_{pd}	CLR	Any	$C_L = 50\text{ pF}$	5.3	8.4		1	9.5	1	9.5	ns
	CLK	Any		6	9.3		1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV175A, SN74LV175A
QUADRUPLE D-TYPE FLIP-FLOPS
WITH CLEAR

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74LV175A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$ High-level dynamic input voltage	2.3			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.97	V

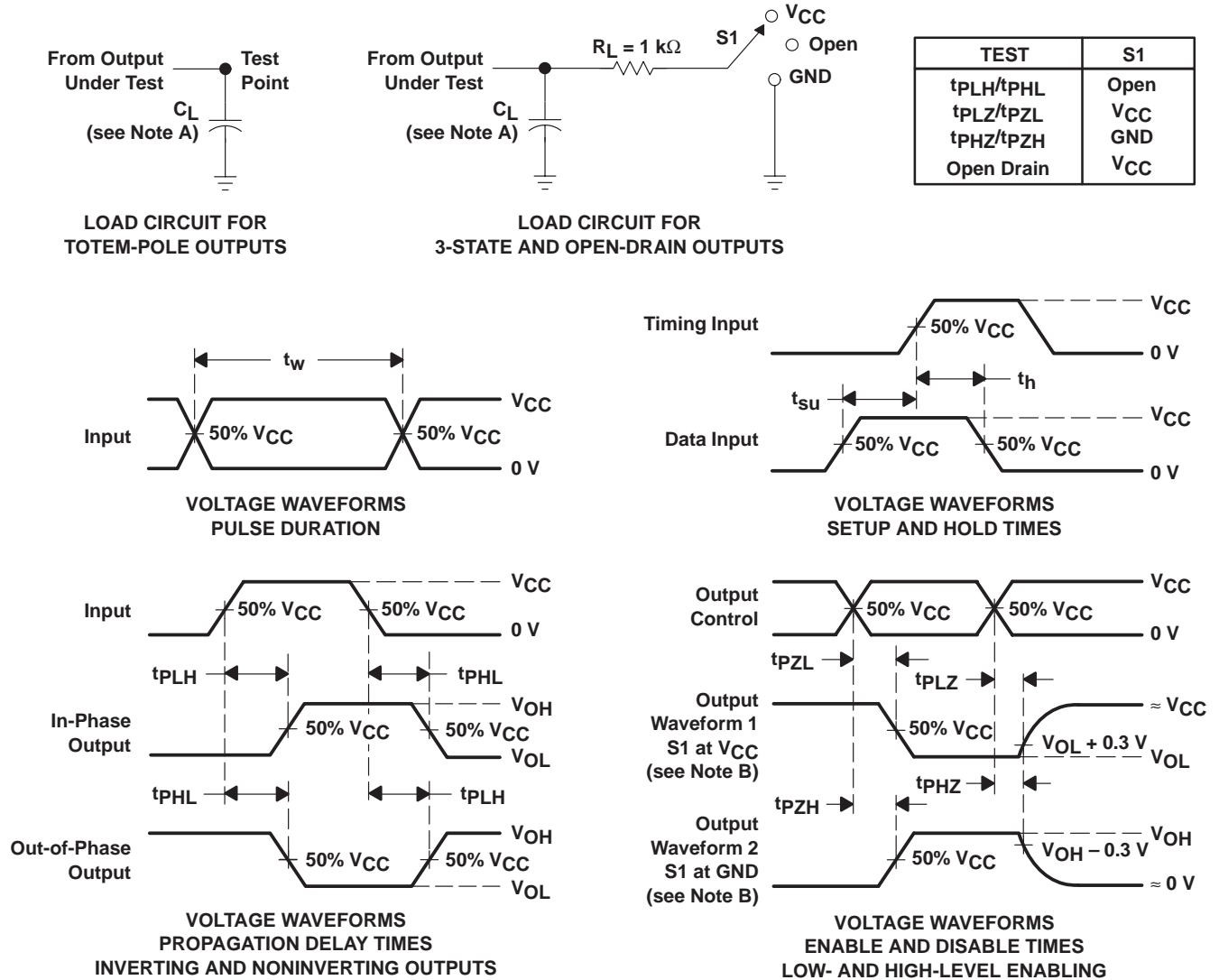
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	13.6	pF
		5 V	14.5	



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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