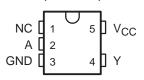
- EPIC[™] (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline Transistor (DBV, DCK) Packages

DBV OR DCK PACKAGES (TOP VIEW)



NC - No internal connection

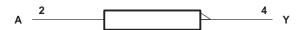
description

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$. The SN74AHC1G04 is characterized for operation from -40° C to 85° C.

FUNCTION TABLE

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.



SCLS318I - MARCH 1996 - REVISED JANUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	347°C/W
DCK package	389°C/W
Storage temperature range, T _{sto}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V
		V _{CC} = 5.5 V		1.65	
VI	Input voltage		0	5.5	V
VO	Output voltage		0	Vcc	V
		V _{CC} = 2 V		-50	μΑ
loh	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	IIIA
		V _{CC} = 2 V		50	μΑ
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8	mA
A+/A>r	Input transition rise or fall rate $ \frac{\text{V}_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}}{\text{V}_{CC} = 5 \text{ V} \pm 0.5 \text{ V}} $			100	20/1/
Δt/Δv				20	ns/V
TA	Operating free-air temperature		-40	85	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vee	T _A = 25°C			MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	WAX	UNIT
		2 V	1.9	2		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
	$I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$	2 V			0.1		0.1	
		3 V			0.1		0.1	
VOL		4.5 V			0.1		0.1	V
		3 V			0.36		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44	
IĮ	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
C _i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	TO LOAD	T _A = 25°C			MIN	MAX	UNIT																				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT																				
^t PLH	۸	Y	C: 45 pF		5	8.9	1	10.5	ne																				
t _{PHL}	A		'	'	'	'	'	'	'	'	'	'	ı	'	•	Į.	·	ı	'	'	'	ı	Γ	$C_L = 15 pF$		5	8.9	1	10.5
^t PLH	Δ.	Y	0. 50-5		7.5	11.4	1	13	no																				
t _{PHL}	A		ľ	Y	Y	Y	Y	Y	Y	C _L = 50 pF		7.5	11.4	1	13	ns													

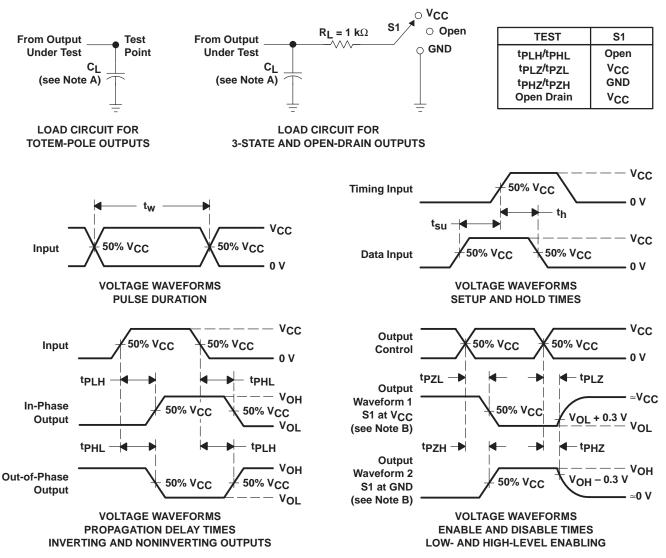
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	FROM TO	LOAD	T _A = 25°C			MIN	MAX	UNIT																					
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT																					
tPLH		Y	0: 45 = 5		3.8	5.5	1	6.5	20																					
t _{PHL}	A		'	'	Ĭ	'	T	'	'	'	'	ı	ľ	ľ	'	'	ľ	ı	ı	ı	ı	ı	T	T C	C _L = 15 pF		3.8	5.5	1	6.5
t _{PLH}		Y	C. 50 pF		5.3	7.5	1	8.5	20																					
tPHL] ^		i i	Ť	T T	A Y	C _L = 50 pF		5.3	7.5	1	8.5	ns																	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 3 \ ns$, $t_f \leq 3 \ ns$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated