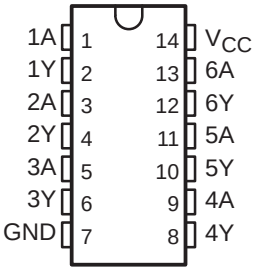
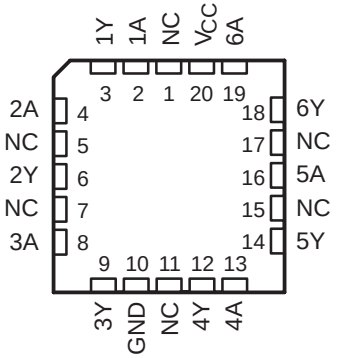
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

SN54LVC06A . . . J OR W PACKAGE
SN74LVC06A . . . D, DGV, OR PW PACKAGE
(TOP VIEW)



SN54LVC06A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex inverter buffers/drivers are designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the ’LVC06A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

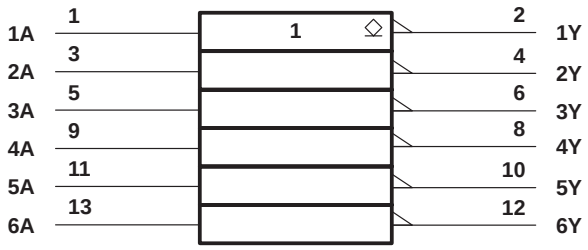
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC06A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVC06A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

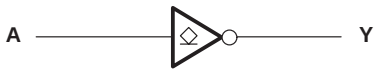
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DGV, and PW packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Output voltage range, V_O . . . . . –0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 80°C/W
DGV package . . . . . 127°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC06A		SN74LVC06A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	5.5	1.65	5.5	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	5.5	0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4	mA
		V_{CC} = 2.3 V		8		8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC06A			SN74LVC06A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V			0.2			0.2	V
	I_{OL} = 4 mA	1.65 V			0.45			0.45	
	I_{OL} = 8 mA	2.3 V			0.7			0.7	
	I_{OL} = 12 mA	2.7 V			0.4			0.4	
	I_{OL} = 24 mA	3 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5			±5	μA
I_{off}	V_I or V_O = 5.5 V	0						±10	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			10			10	μA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		5			5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC06A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.4	3.9	1	3.1		3.9	1	3.7	ns

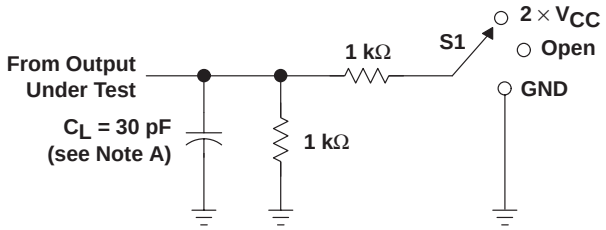
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC06A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.4	3.9	1	3.1		3.9	1	3.7	ns

operating characteristics, T_A = 25°C

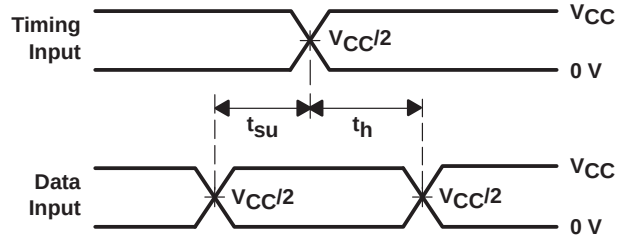
PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	2.1	2.3	2.5	pF

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V ± 0.15 V

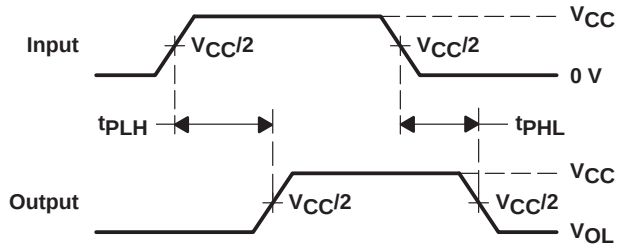


TEST	S1
t_{PZL} (see Note F)	2 × V_{CC}
t_{PLZ} (see Note G)	2 × V_{CC}
t_{PHZ}/t_{PZH}	2 × V_{CC}

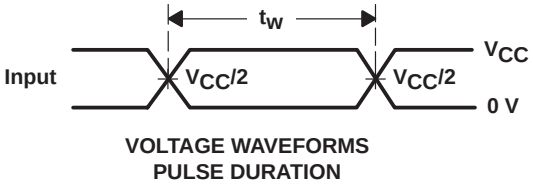
LOAD CIRCUIT



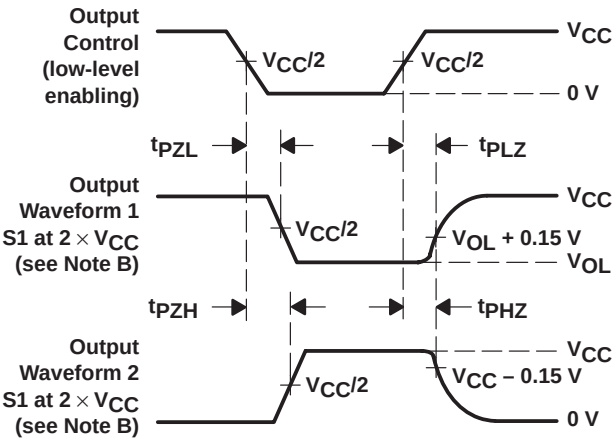
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

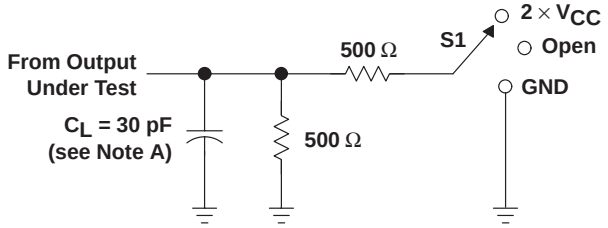


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at $V_{CC}/2$.
G. t_{PLZ} is measured at V_{OL} + 0.15 V.

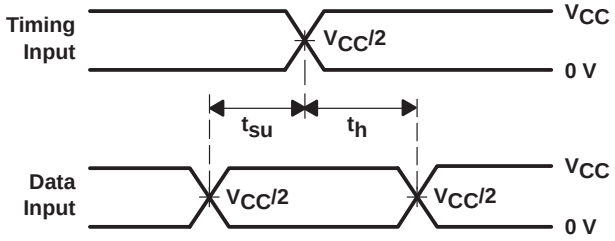
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

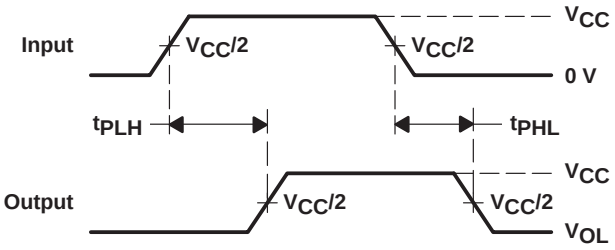


TEST	S1
t_{PZL} (see Note F)	2 × V_{CC}
t_{PLZ} (see Note G)	2 × V_{CC}
t_{PHZ}/t_{PZH}	2 × V_{CC}

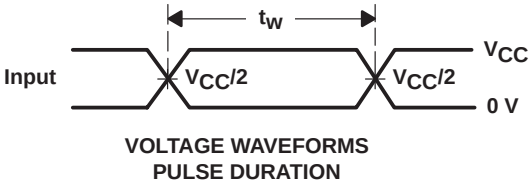
LOAD CIRCUIT



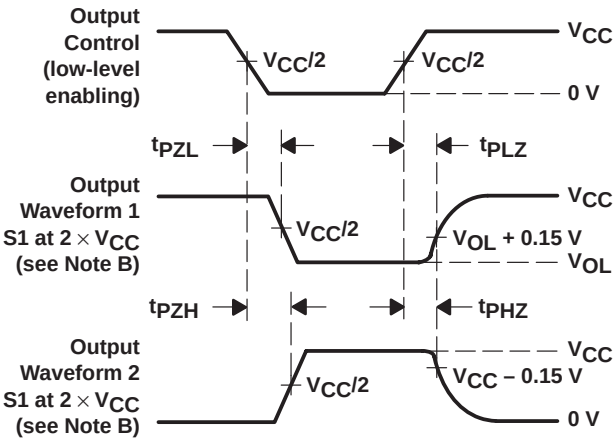
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

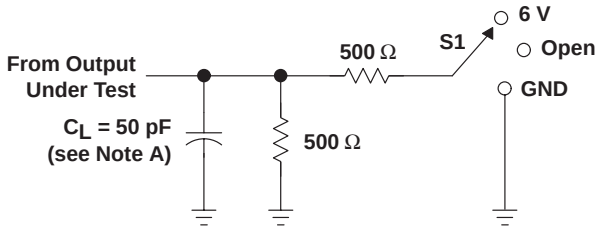


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at $V_{CC}/2$.
G. t_{PLZ} is measured at V_{OL} + 0.15 V.

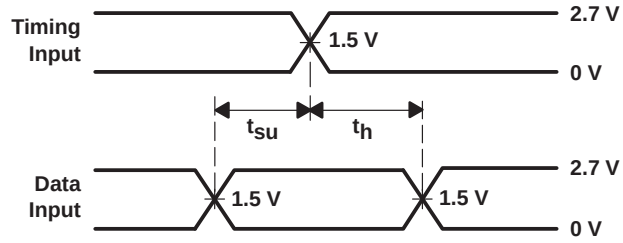
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 AND 3.3 V ± 0.3 V

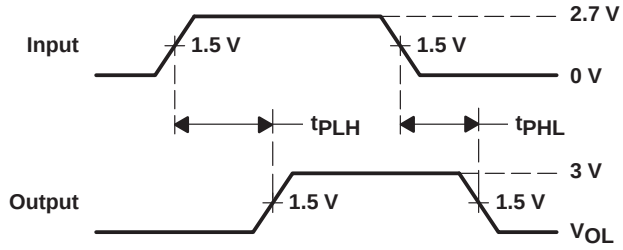


TEST	S1
t_{PZL} (see Note F)	6 V
t_{PLZ} (see Note G)	6 V
t_{PHZ}/t_{PZH}	6 V

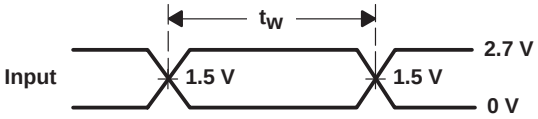
LOAD CIRCUIT



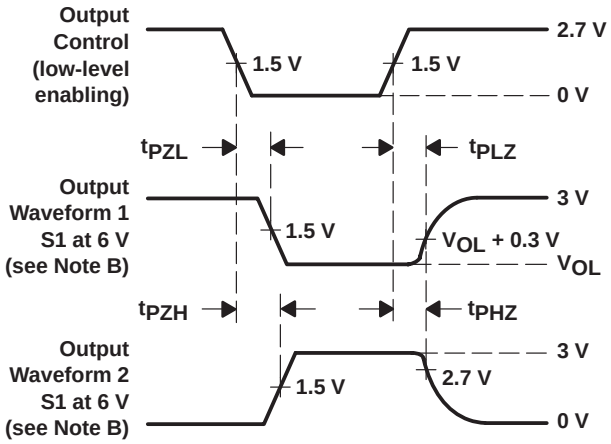
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at 1.5 V.
G. t_{PLZ} is measured at V_{OL} + 0.3 V.

Figure 3. Load Circuit and Voltage Waveforms

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