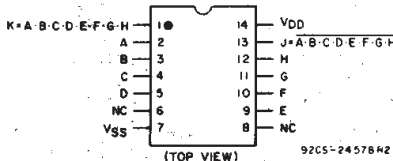


CMOS 8-Input NAND/AND Gate

High-Voltage Types (20-Volt Rating)

■ CD4068B NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of CMOS gates.

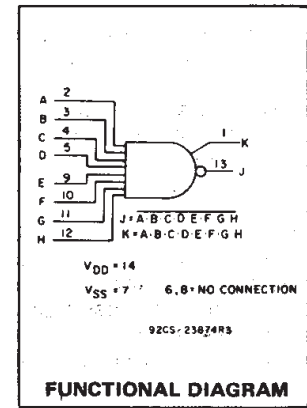
The CD4068B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes); 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



NC = NO CONNECTION
TERMINAL ASSIGNMENT

Features:

- Medium-Speed Operation:
t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- Buffered inputs and outputs
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V
2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T _A = Full Package Temperature Range)	3	18	V

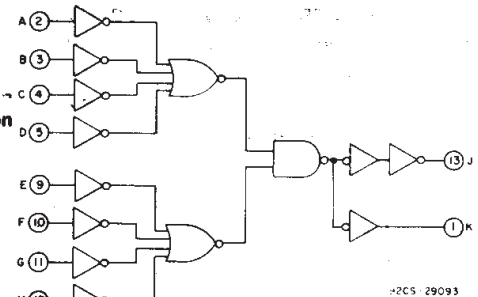


Fig. 1 - Logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0.15	15	1	1	30	30	-	0.01	1	
	-	0.20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5	0.05			-	0	0.05	-	V
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5	4.95			4.95	5	-	-	V
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	V
	1.9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5			3.5	-	-	-	V
	1.9	-	10	7			7	-	-	-	
	1.5, 13.5	-	15	11			11	-	-	-	
Input Current I _{IN} Max.		0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

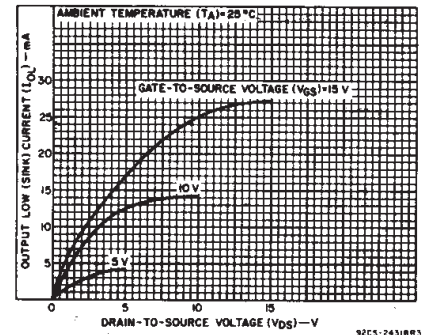


Fig. 2 - Typical output low (sink) current characteristics.

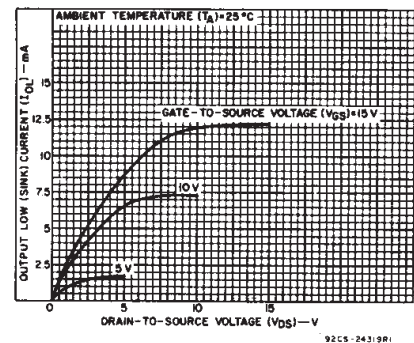


Fig. 3 - Minimum output low (sink) current characteristics.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4068B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max	$+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V_{DD} VOLTS	TYP.		MAX.
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF	

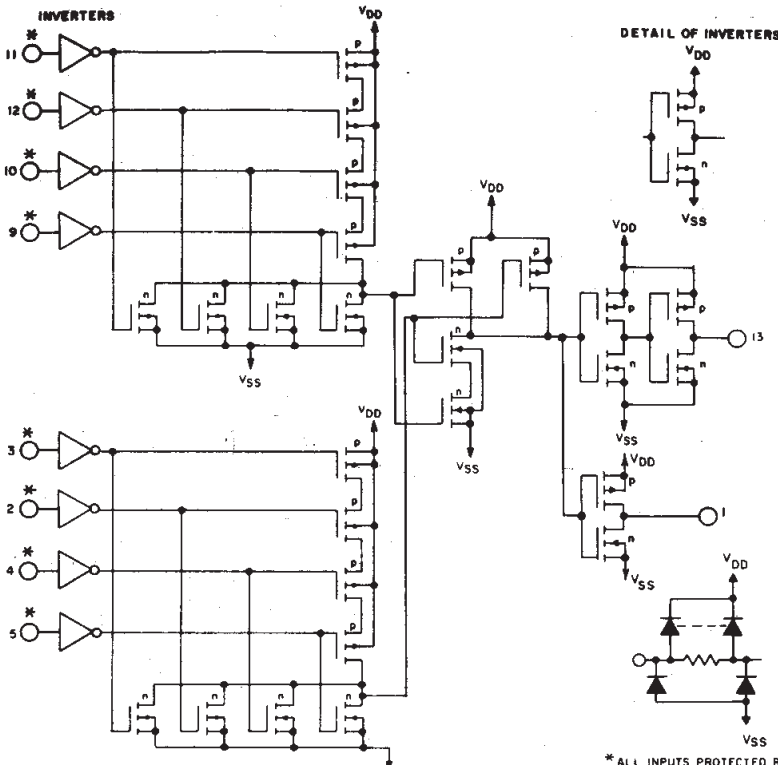


Fig. 7 - Schematic diagram.

* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK 92CM-29094

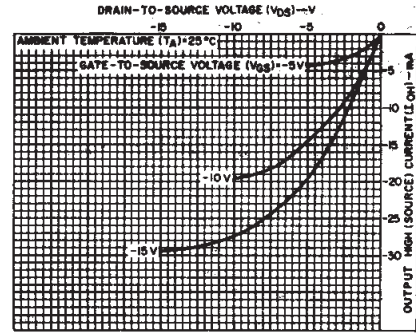


Fig. 4 - Typical output high (source) current characteristics.

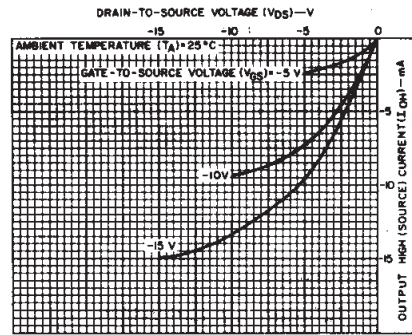


Fig. 5 - Minimum output high (source) current characteristics.

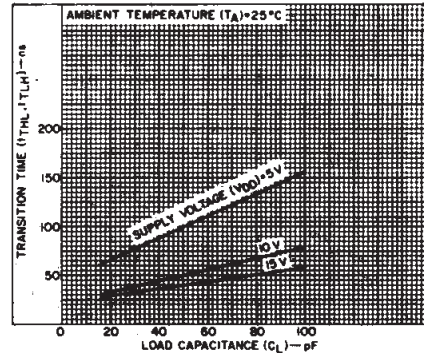


Fig. 6 - Typical transition time as a function of load capacitance.

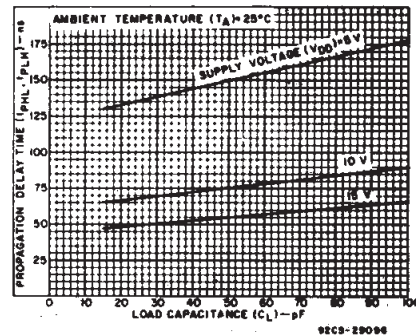


Fig. 8 - Typical propagation delay time as a function of load capacitance.

CD4068B Types

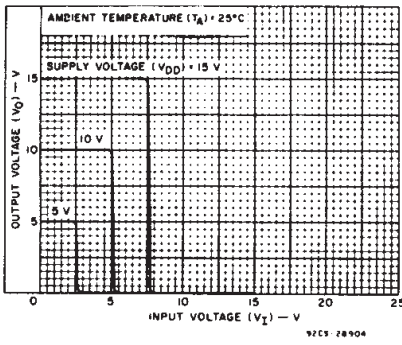


Fig. 9 - Typical voltage transfer characteristics (NAND output).

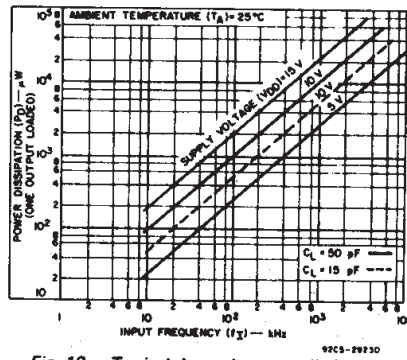


Fig. 10 - Typical dynamic power dissipation as a function of frequency.

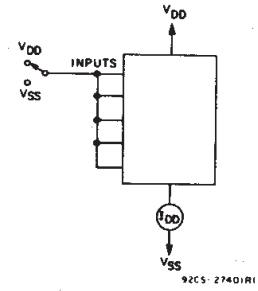


Fig. 11 - Quiescent-device-current test circuit.

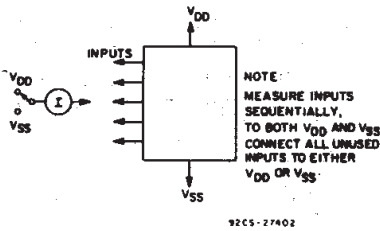


Fig. 12 - Input current test circuit.

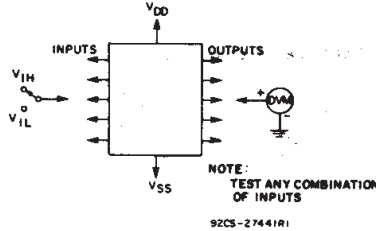


Fig. 13 - Input-voltage test circuit.

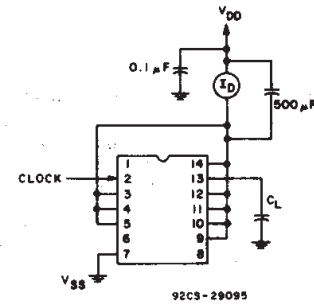
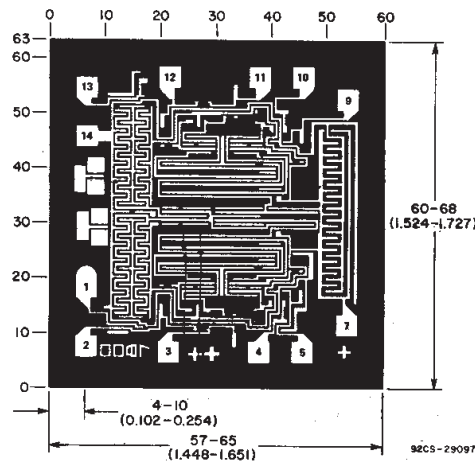


Fig. 14 - Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4068BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

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