

CD74AC10, CD74ACT10

September 1998

Triple 3-Input NAND Gate

Features

- **Typical Propagation Delay**
 - 6ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$ Output Drive Current
 - Fanout to 15 FAST™ ICs
 - Drives 50Ω Transmission Lines

Description

The CD74AC10 and CD74ACT10 are triple 3-input NAND gates that utilize the Harris Advanced CMOS Logic technology.

Ordering Information

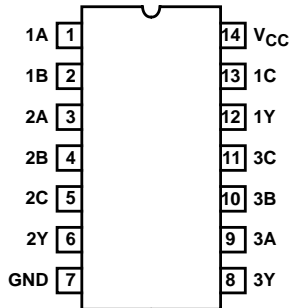
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74AC10E	-55 to 125	14 Ld PDIP	E14.3
CD74ACT10E	-55 to 125	14 Ld PDIP	E14.3
CD74AC10M	-55 to 125	14 Ld SOIC	M14.15
CD74ACT10M	-55 to 125	14 Ld SOIC	M14.15

NOTES:

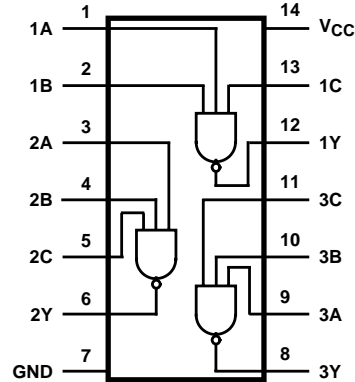
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74AC10, CD74ACT10
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number **1977.1**

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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 6V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 50mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3)	$\pm 100mA$

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
SOIC Package	175
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC} (Note 4)	
AC Types	1.5V to 5.5V
ACT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V	50ns (Max)
AC Types, 3.6V to 5.5V	20ns (Max)
ACT Types, 4.5V to 5.5V	10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	12	3	-	0.36	-	0.44	-	0.5	V
			24	24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	75	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	50	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA	
Quiescent Supply Current, SSI	I _{CC}	V _{CC} or GND	0	5.5	-	4	-	40	-	80	μA	
ACT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V	
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V	
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75	-75	5.5	-	-	3.85	-	-	-	V
			-50	-50	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	75	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	50	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA	
Quiescent Supply Current, SSI	I _{CC}	V _{CC} or GND	0	5.5	-	4	-	40	-	80	μA	
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA	

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
All	0.19

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

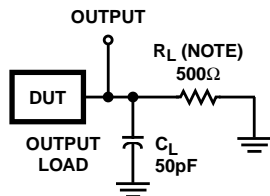
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Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, Input to Output	t_{PLH}, t_{PHL}	1.5	-	-	139	-	-	153	ns
		3.3 (Note 9)	4.4	-	15.5	4.3	-	17.1	ns
		5 (Note 10)	3.1	-	11.1	3.1	-	12.2	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	50	-	-	50	-	pF
ACT TYPES									
Propagation Delay, Input to Output	t_{PHL}	5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	50	-	-	50	-	pF

NOTES:

8. Limits tested at 100%.
9. 3.3V Min at 3.6V, Max at 3V.
10. 5V Min at 5.5V, Max at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per gate.
 AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
 ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.



NOTE: For AC Series Only: When $V_{CC} = 1.5\text{V}$, $R_L = 1\text{k}\Omega$.

	CD74AC	CD74ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

FIGURE 1. PROPAGATION DELAY TIMES

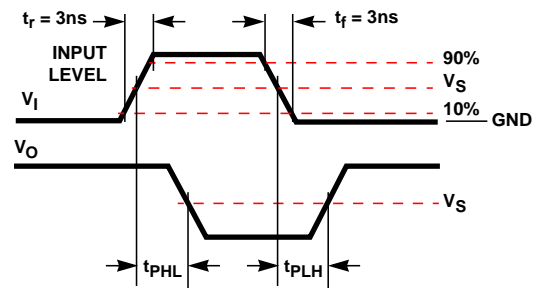


FIGURE 2. PROPAGATION DELAY TIMES

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