

SN54HC132, SN74HC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS034C – DECEMBER 1982 – REVISED MAY 1997

- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC00
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

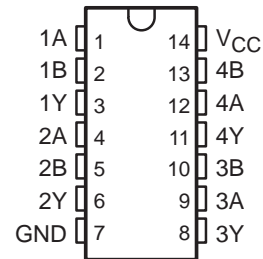
description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'HC132 perform the Boolean function $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

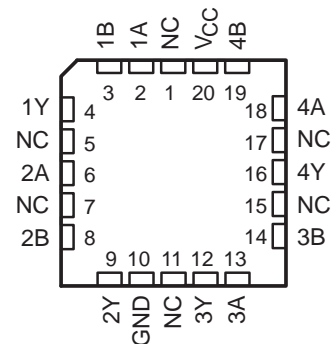
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC132 is characterized for operation from -40°C to 85°C .

SN54HC132 . . . J OR W PACKAGE
SN74HC132 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC132 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

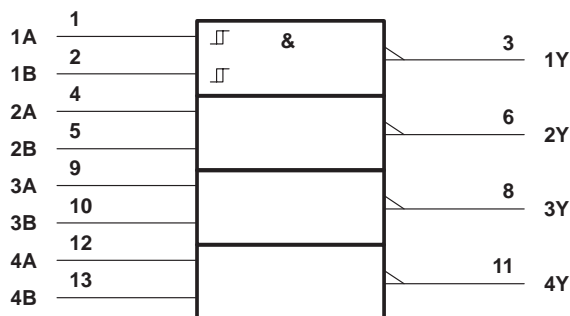
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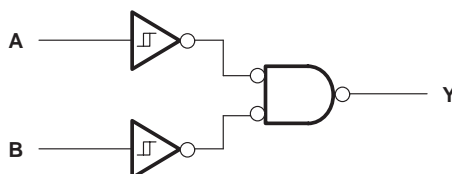
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
DB package	158°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

		SN54HC132			SN74HC132			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	2	5	6	2	5	6	V		
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V			
		V _{CC} = 4.5 V	3.15		3.15					
		V _{CC} = 6 V	4.2		4.2					
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0	0.5	0	0.5	V			
		V _{CC} = 4.5 V	0	1.35	0	1.35				
		V _{CC} = 6 V	0	1.8	0	1.8				
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V		
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V		
T _A	Operating free-air temperature	-55			125			-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC132		SN74HC132		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
			6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
			6 V		0.15	0.26		0.4		0.33	
V _{T+}		2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V	
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15		
		6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2		
V _{T-}		2 V	0.3	0.6	1	0.3	1	0.3	1	V	
		4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45		
		6 V	1.2	2	3.2	1.2	3.2	1.2	3.2		
V _{T+} - V _{T-}		2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V	
		4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1		
		6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5		
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			2		40		20	μA	
C _i		2 V to 6 V		3	10		10		10	pF	



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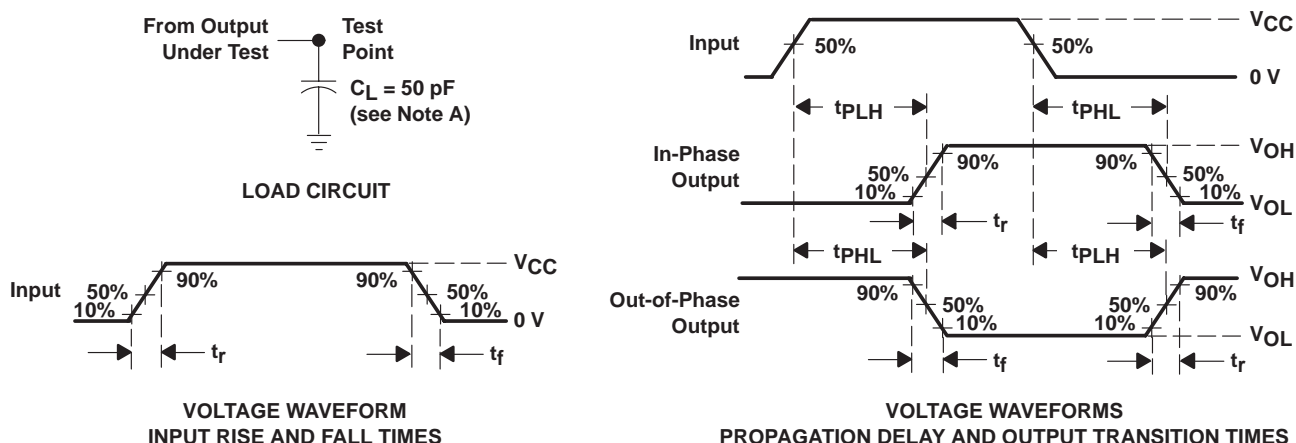
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	120		186		156	ns
			4.5 V		18	25		37		31	
			6 V		14	21		32		27	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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