SN74ALVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

SCES106D - JULY 1997 - REVISED OCTOBER 1998

- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

D, DGV, OR PW PACKAGE (TOP VIEW) 14 🛮 V_{CC} 1A [1B 🛮 2 13 🛮 1C 2A Π 3 12 **∏** 1Y 2B **∏**4 11 3C 2C [5 10 3B 9 3A 2Y 🛮 6 GND [∏ 3Y 8

description

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

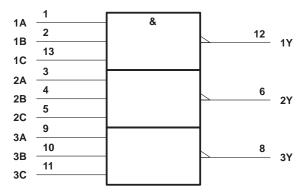
The SN74ALVC10 performs the Boolean function $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN74ALVC10 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

| | INPUTS | OUTPUT | | | |
|---|--------|--------|---|--|--|
| Α | В | С | Υ | | |
| Н | Н | Н | L | | |
| L | X | Χ | н | | |
| Х | L | Χ | н | | |
| Х | Χ | L | Н | | |

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

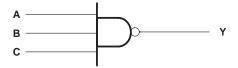


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logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | | -0.5 V to 4.6 V |
|------------------------------------------------------------|-------------|-----------------------|
| Input voltage range, V _I (see Note 1) | | -0.5 V to 4.6 V |
| Output voltage range, VO (see Notes 1 and 2) | | to V_{CC} + 0.5 V |
| Input clamp current, I_{IK} ($V_I < 0$) | | –50 mA |
| Output clamp current, I _{OK} (V _O < 0) | | –50 mA |
| Continuous output current, IO | | ±50 mA |
| Continuous current through V _{CC} or GND | | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): | : D package | 127°C/W |
| | DGV package | 182°C/W |
| | PW package | 170°C/W |
| Storage temperature range, T _{stg} | | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

 2. This value is limited to 4.6 V maximum.

 - 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|----------|--------------------------------------------|----------------------------------------------|------------------------|----------------------|------|
| VCC | Supply voltage | y voltage | | 3.6 | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | |
| V_{IH} | High-level input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2 | | |
| | | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | | $0.35 \times V_{CC}$ | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | | 0.7 | V |
| | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | | | 0.8 | |
| VI | Input voltage | | 0 | VCC | V |
| ٧o | Output voltage | | 0 | VCC | V |
| | | V _{CC} = 1.65 V | | -4 | |
| la | High-level output current | V _{CC} = 2.3 V | | -12 | mA |
| IOH | riigii-ievei output current | V _{CC} = 2.7 V | | -12 | IIIA |
| | | V _{CC} = 3 V | | -24 | |
| | | V _{CC} = 1.65 V | 4 | | mA |
| loi | Low-level output current | $V_{CC} = 2.3 \text{ V}$ 12 | | 12 | |
| lOL | Low-level output current | $V_{CC} = 2.7 \text{ V}$ | 12 | | |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δν | Input transition rise or fall rate | | 0 | 5 | ns/V |
| TA | Operating free-air temperature | | -40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CON | IDITIONS | vcc | MIN | TYP [†] | MAX | UNIT |
|-----------|-----------------------------------------|----------------------------------------|-----------------|---------------------|------------------|------|------|
| | I _{OH} = -100 μA | | 1.65 V to 3.6 V | V _{CC} -0. | 2 | | |
| | I _{OH} = -4 mA | | 1.65 V | 1.2 | | | |
| | I _{OH} = -6 mA | | 2.3 V | 2 | | | |
| Voн | | | 2.3 V | 1.7 | | | V |
| | I _{OH} = -12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | 3 V | 2 | | | |
| | I _{OL} = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | |
| | I _{OL} = 4 mA | | 1.65 V | | | 0.45 | |
| \/o. | $I_{OL} = 6 \text{ mA}$ | | 2.3 V | | | 0.4 | V |
| VOL | I _{OL} = 12 mA | | 2.3 V | | | 0.7 | V |
| | IOL = 12 IIIA | | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | | 3 V | | | 0.55 | |
| lį | V _I = V _{CC} or GND | | 3.6 V | | | ±5 | μΑ |
| lcc | $V_I = V_{CC}$ or GND, | I _O = 0 | 3.6 V | | | 10 | μΑ |
| ΔlCC | One input at V _{CC} – 0.6 V, | Other inputs at V _{CC} or GND | 3 V to 3.6 V | | | 750 | μΑ |
| Ci | V _I = V _{CC} or GND | | 3.3 V | | 4 | · | pF |

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

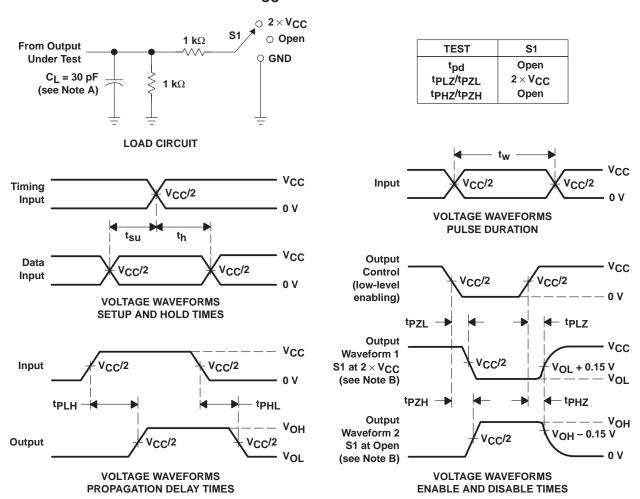
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = | | V _{CC} = | | V _{CC} = | 2.7 V | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|-----------------|----------------|-------------------|-----|-------------------|-----|-------------------|-------|------------------------------------|-----|------|
| | (INFOT) | (001101) | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A, B, or C | Y | 1.1 | 4.8 | 1 | 3 | | 3.3 | 1 | 3 | ns |

operating characteristics, $T_A = 25^{\circ}C$

| ſ | PARAMETER | | TEST CONDITIONS | | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------|-----------------|----------------------------------------|---------------------|------------|-------------------------|-------------------------|-------------------------|------|
| PARAMETER | | TEST CONDITIONS | | TYP | TYP | TYP | UNIT | |
| ſ | C _{pd} | Power dissipation capacitance per gate | C _L = 0, | f = 10 MHz | 23 | 24 | 26 | pF |

PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V \pm 0.15 V

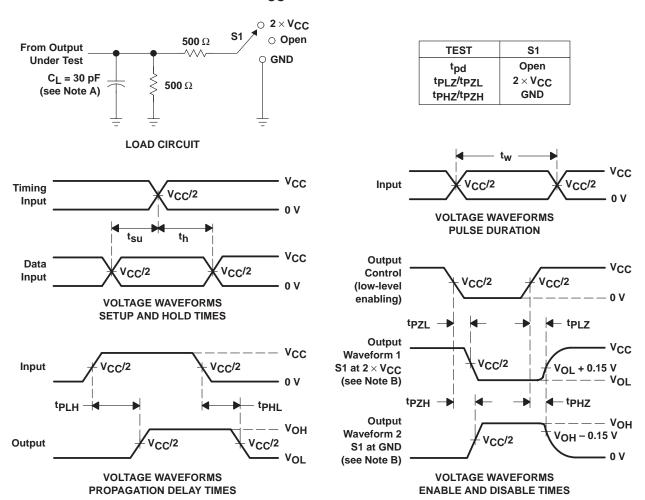


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

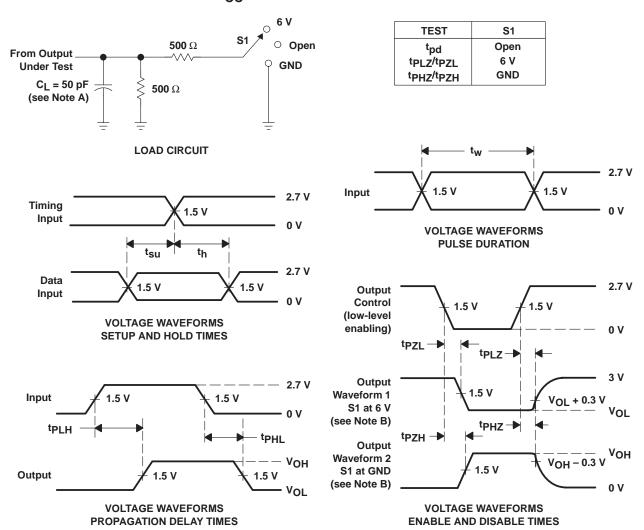
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \le 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f \le 2 \text{ ns}$, $t_f \le 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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