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- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 > 2 V at V_{CC}, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

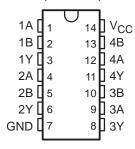
description

These quadruple 2-input positive-OR gates are designed for 2-V to 5.5-V V_{CC} operation.

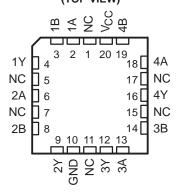
The 'LV32A devices perform the Boolean function Y = A + B or $Y = \overline{A \bullet B}$ in positive logic.

The SN54LV32A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LV32A is characterized for operation from -40°C to 85°C.

SN54LV32A . . . J OR W PACKAGE SN74LV32A . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



SN54LV32A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	Н
Х	Н	Н
L	L	L



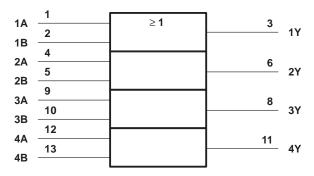
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	D package DB package DGV package	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
	N package	80°C/W
Storage temperature range, T _{stg}	, -	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 7 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 4)

			SN54L	SN54LV32A		V32A	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V _{CC} × 0.7		$V_{CC} \times 0.7$		V
۷IH	r light-level lilput voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		ď
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5		0.5	
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V	CC × 0.3	V	CC×0.3	V
۷IL	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	V	CC×0.3	V	CC×0.3	ľ
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V	CC×0.3	V	CC×0.3	
٧ _I	Input voltage		0	5.5	0	5.5	V
۷o	Output voltage		0 2	Vcc	0	VCC	V
		V _{CC} = 2 V	3	- 50		-50	μΑ
lou	High-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	90	-2		-2	
ЮН	riigii-ievei output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	Q	-6		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		-12	
		V _{CC} = 2 V		50		50	μΑ
lOL	Low-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
IOL	Low-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$		6		6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	200	0	200	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3 V \text{ to } 3.6 V$	0	100	0	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0	20	0	20	
T_A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LV32A	SN74LV32A	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN TYP MAX	MIN TYP MAX	UNII
	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1	V _{CC} -0.1	
Vari	$I_{OH} = -2 \text{ mA}$	2.3 V	2	2	V
VOH	I _{OH} = -6 mA	3 V	2.48	2.48	V
	I _{OH} = -12 mA	4.5 V	3.8	3.8	
	I _{OL} = 50 μA	2 V to 5.5 V	0.1	0.1	
V _{OL}	I _{OL} = 2 mA	2.3 V	0.4	0.4	V
VOL VOL	I _{OL} = 6 mA	3 V	0.44	0.44	V
	I _{OL} = 12 mA	4.5 V	0.55	0.55	
lį	$V_I = V_{CC}$ or GND	5.5 V	±1	±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	20	20	μΑ
l _{off}	V_I or $V_O = 0$ to 5.5 V	0 V	5	5	μΑ
C.	VI = Voc or GND	3.3 V	3.4	3.4	pF
C _i	$V_I = V_{CC}$ or GND	5 V	3.4	3.4	PΓ

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	Δ = 25°C	;	SN54LV32A	SN74I	_V32A	UNIT
PARAMETER	(INPUT)	(INPUT) (OUTPUT) CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT	
^t pd	A or B	Υ	C _L = 15 pF		7.1*	12.8*	10 16	1	15	ns
t _{pd}	A or B	Υ	C _L = 50 pF		9.6	16.2	1 20) 1	19	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO LOAD		LOAD	T,	4 = 25°C	;	SN54LV32A	SN74L	.V32A	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A or B	Y	C _L = 15 pF		5*	7.9*	1 9.5*	1	9.5	ns
t _{pd}	A or B	Y	$C_L = 50 pF$		6.9	11.4	1 13	1	13	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	4 = 25°C	;	SN54LV32A	SN74L	.V32A	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A or B	Υ	C _L = 15 pF		3.6*	5.5*	1* 6.5*	1	6.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		4.9	7.5	1 8.5	1	8.5	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 5)

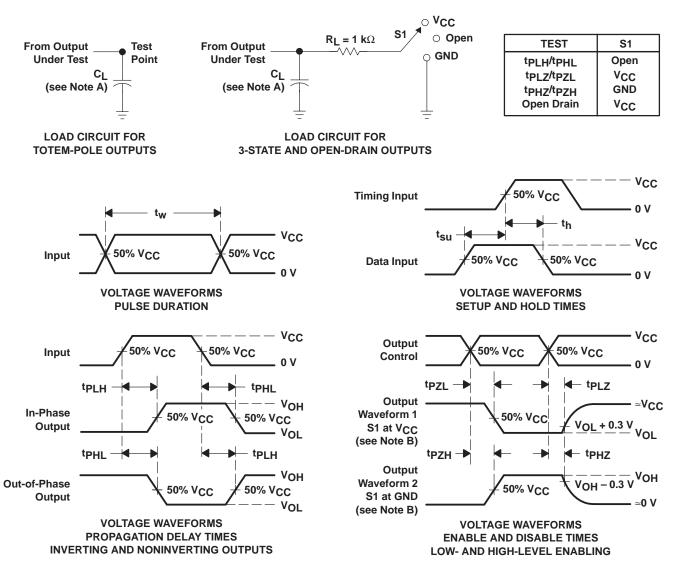
	PARAMETER		SN74LV32A			
	PARAMETER	MIN	TYP	0.8 -0.8	UNIT	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	V	
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.1	-0.8	V	
VOH(V)	Quiet output, minimum dynamic VOH		3.1		V	
VIH(D)	High-level dynamic input voltage	2.31			V	
V _{IL(D)}	Low-level dynamic input voltage			0.99	V	

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST COI	VCC	TYP	UNIT	
C _{pd}	Power dissipation capacitance	$C_1 = 50 pF$	f = 10 MHz	3.3 V	9.5	ηF
		CL = 50 pr,	1 - 10 1011 12	5 V	11	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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