

CD74HC373, CD74HCT373, CD54HC573, CD74HC573, CD74HCT573

High Speed CMOS Logic Octal Transparent Latch, Three-State Output

Features

- Common Latch Enable Control
- Common Three-State Output Enable Control
- Buffered Inputs
- Three-State Outputs
- Bus Line Driving Capacity
- Typical Propagation Delay = 12ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$ (Data to Output for HC373)
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The Harris CD74HC373, CD74HCT373, CD54HC573, CD74HC573, and CD74HCT573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD74HCT373 and CD74HCT573 are functionally as well as pin compatible with the standard 74LS373 and 74LS573.

The outputs are transparent to the inputs when the latch enable (\overline{LE}) is high. When the latch enable (\overline{LE}) goes low the data is latched. The output enable (\overline{OE}) controls the three-state outputs. When the output enable (\overline{OE}) is high the outputs are in the high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pinout arrangements.

Ordering Information

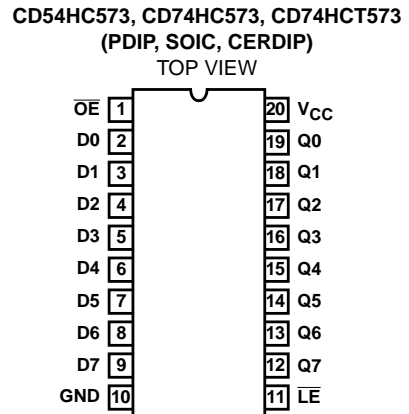
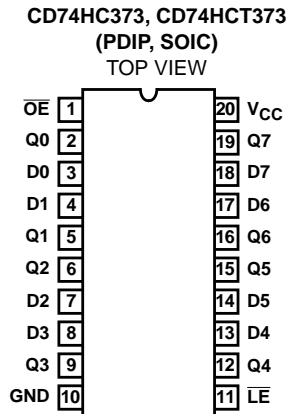
| PART NUMBER | TEMP. RANGE ($^\circ C$) | PACKAGE | PKG. NO. |
|-------------|-------------------------------|--------------|-------------|
| CD54HC573F | -55 to 125 | 20 Ld CERDIP | F20.3 |
| CD74HC373E | -55 to 125 | 20 Ld PDIP | F20.3 |
| CD74HCT373E | -55 to 125 | 20 Ld PDIP | E20.3 |
| CD74HC573E | -55 to 125 | 20 Ld PDIP | E20.3 |
| CD74HCT573E | -55 to 125 | 20 Ld PDIP | E20.3 |
| CD74HC373M | -55 to 125 | 20 Ld SOIC | M20.3 |
| CD74HCT373M | -55 to 125 | 20 Ld SOIC | M20.3 |
| CD74HC573M | -55 to 125 | 20 Ld SOIC | M20.3 |
| CD74HCT573M | -55 to 125 | 20 Ld SOIC | M20.3 |

NOTES:

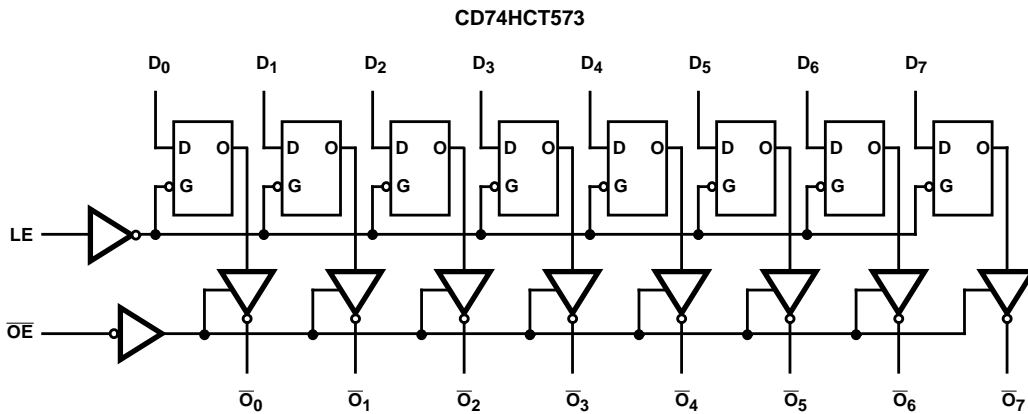
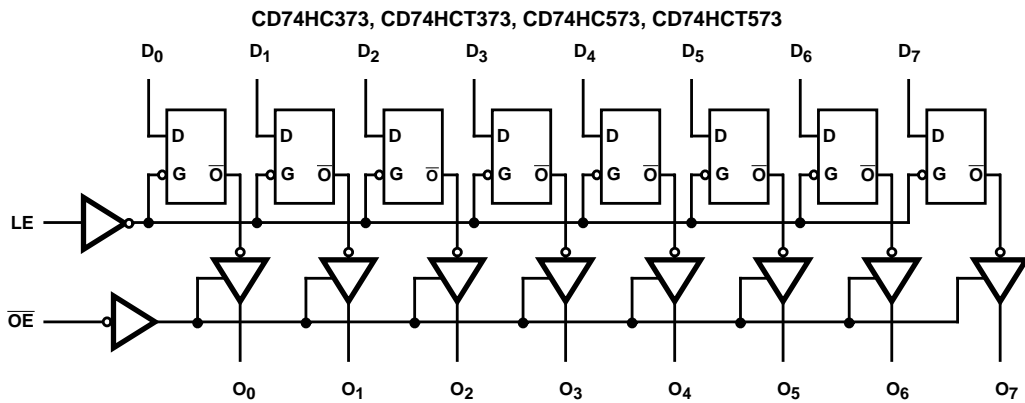
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number are available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

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Pinout



Functional Block Diagrams



TRUTH TABLE

| OUTPUT ENABLE | LATCH ENABLE | DATA | OUTPUT |
|---------------|--------------|------|--------|
| L | H | H | H |
| L | H | L | L |
| L | L | l | L |
| L | L | h | H |
| H | X | X | Z |

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance State, l = Low voltage level one set-up time prior to the high to low latch enable transition, h = High voltage level one set-up time prior to the high to low latch enable transition.

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Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Drain Current, per Output, I_O | |
| For $-0.5V < V_O < V_{CC} + 0.5V$ | $\pm 35mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 50mA$ |

Thermal Information

| | | |
|--|--|---------------------------------|
| Thermal Resistance (Typical, Note 3) | θ_{JA} ($^{\circ}C/W$) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | 125 | N/A |
| CERDIP Package | 85 | 24 |
| SOIC Package | 120 | N/A |
| Maximum Junction Temperature (Plastic Package) | 150 $^{\circ}C$ | |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ | |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|--|------------------------------------|
| Temperature Range, T_A | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | .4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---|----------|-------------------------|------------|--------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |

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DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|------------------------------------|---|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | - | V _{IL} or V _{IH} | V _O = V _{CC} or GND | 6 | - | - | ±0.5 | - | ±5 | - | ±10 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} to GND | - | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Three-State Leakage Current | - | V _{IL} or V _{IH} | V _O = V _{CC} or GND | 6 | - | - | ±0.5 | - | ±5 | - | ±10 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4) | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS | |
|-----------------|------------|--------|
| | HCT373 | HCT573 |
| \overline{OE} | 1.5 | 1.25 |
| Dn | 0.4 | 0.3 |
| \overline{LE} | 0.6 | 0.65 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

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Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|-----------------------------|-----------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| LE Pulse Width | t _w | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Set-up Time Data to LE | t _{SU} | - | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| Hold Time, Data to LE (573) | t _H | - | 2 | 40 | - | - | 50 | - | 60 | - | ns |
| | | | 4.5 | 8 | - | - | 10 | - | 12 | - | ns |
| | | | 6 | 7 | - | - | 9 | - | 10 | - | ns |
| Hold Time, Data to LE (373) | t _H | - | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | | 6 | 5 | - | - | 5 | - | 5 | - | ns |
| HCT TYPES | | | | | | | | | | | |
| LE Pulse Width | t _w | - | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| Set-up Time Data to LE | t _w | - | 4.5 | 13 | - | - | 16 | - | 20 | - | ns |
| Hold Time, Data to LE | t _H | - | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | | |
| Propagation Delay, Data to Qn (HC/HCT373) | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | 6 | - | 26 | 33 | 38 | ns | |
| | | C _L = 15pF | 5 | 12 | - | - | - | ns |
| Propagation Delay, Data to Qn (HC/HCT573) | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | 6 | - | 30 | 37 | 45 | ns | |
| | | C _L = 15pF | 5 | 14 | - | - | - | ns |
| Propagation Delay, LE to Qn | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | 6 | - | 30 | 37 | 45 | ns | |
| | | C _L = 15pF | 5 | 14 | - | - | - | ns |

CD74HC373, CD74HCT373, CD54HC573, CD74HC573, CD74HCT573

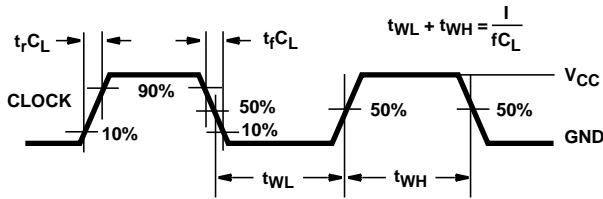
Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| Output Enabling Time | t _{PZL} , t _{PZH} | C _L = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | C _L = 15pF | 5 | 12 | - | - | - | ns |
| Output Disabling Time | t _{PLZ} , t _{PHZ} | C _L = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | C _L = 15pF | 5 | 12 | - | - | - | ns |
| Output Transition Time | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | 60 | 75 | 90 | ns |
| | | | 4.5 | - | 12 | 15 | 18 | ns |
| | | | 6 | - | 10 | 13 | 15 | ns |
| Input Capacitance | C _I | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | C _O | - | - | - | 20 | 20 | 20 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C _{PD} | - | 5 | 51 | - | - | - | pF |
| HCT TYPES | | | | | | | | |
| Propagation Delay, Data to Qn (HC/HCT373) | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | 32 | 40 | 48 | ns |
| | | C _L = 15pF | 5 | 13 | - | - | - | ns |
| Propagation Delay, Data to Qn (HC/HCT573) | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | C _L = 15pF | 5 | 17 | - | - | - | ns |
| Propagation Delay, $\overline{\text{LE}}$ to Qn | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | C _L = 15pF | 5 | 14 | - | - | - | ns |
| Output Enabling Time | t _{PZL} , t _{PZH} | C _L = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | C _L = 15pF | 5 | 14 | - | - | - | ns |
| Output Disabling Time | t _{PLZ} , t _{PHZ} | C _L = 50pF | 4.5 | - | 35 | 44 | 53 | ns |
| | | C _L = 15pF | 5 | 14 | - | - | - | ns |
| Output Transition Time | t _{TLH} , t _{THL} | C _L = 50pF | 4.5 | - | 12 | 15 | 18 | ns |
| Input Capacitance | C _I | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | C _O | - | - | - | 20 | 20 | 20 | pF |
| Power Dissipation Capacitance (Notes 5, 6) | C _{PD} | - | 5 | 53 | - | - | - | pF |

NOTES:

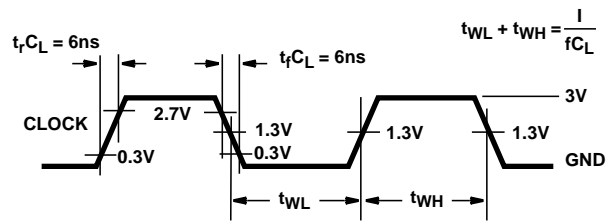
- C_{PD} is used to determine the no-load dynamic power consumption, per latch.
- P_D (total power per latch) = V_{CC}² f_i (C_{PD} + C_L) where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

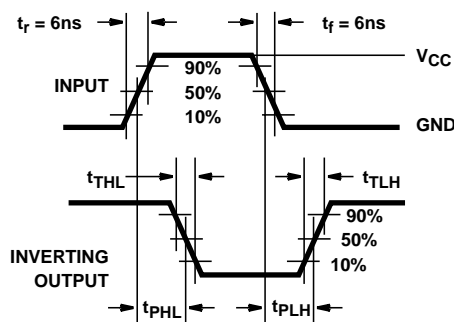


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

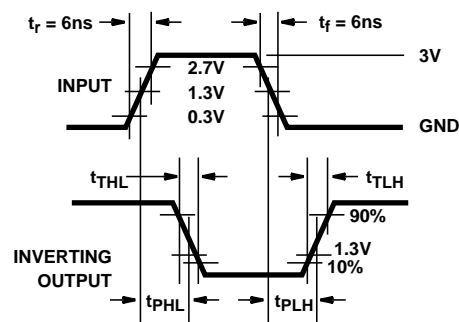


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

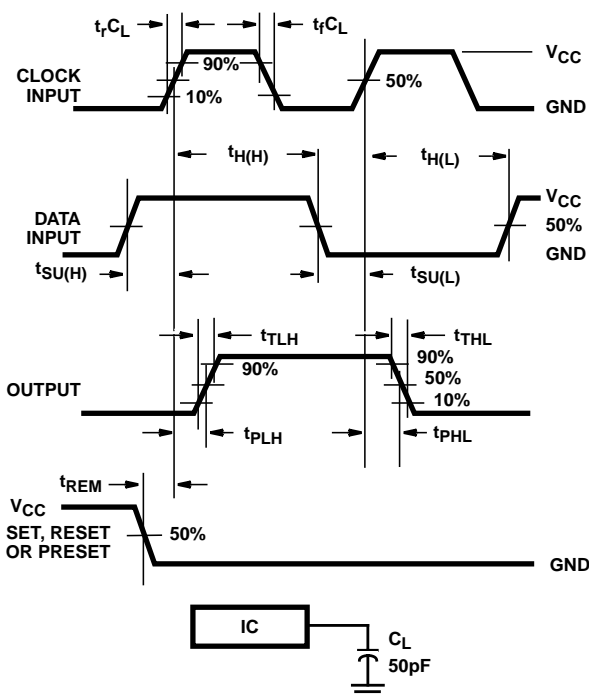


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

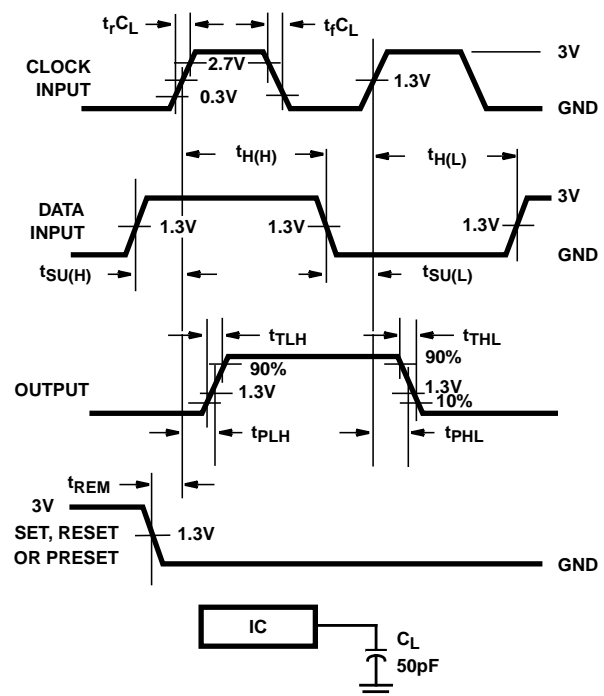


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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Test Circuits and Waveforms (Continued)

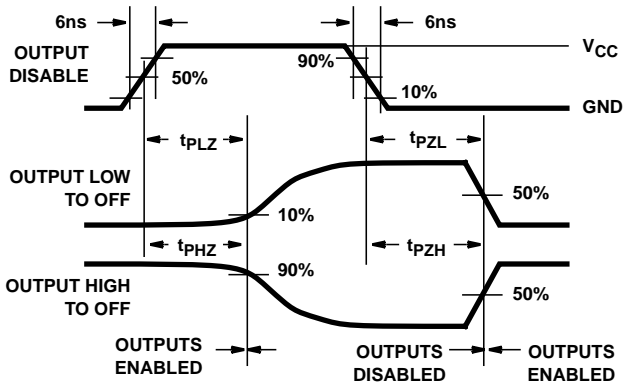


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

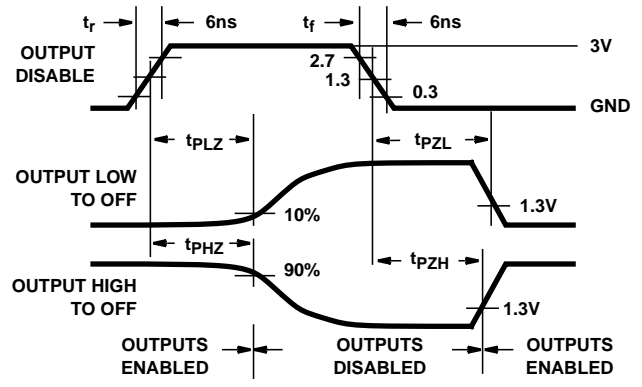
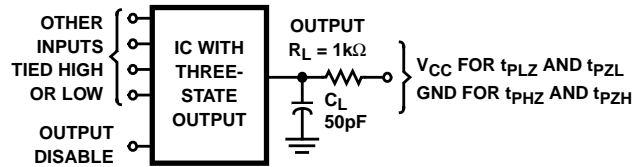


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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