

# CD74FCT843A, CD74FCT844A

## BiCMOS FCT Interface Logic, 9-Bit Transparent Latches, Three-State

**NOT RECOMMENDED  
FOR NEW DESIGNS**  
Use CMOS Technology

### Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$  (FCT843A)
- CD74FCT843A
  - Noninverting
- CD74FCT844A
  - Inverting
- SCR Latchup Resistant BiCMOS Process and

### Circuit Design

- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at  $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to  $V_{CC}$
- BiCMOS Technology with Low Quiescent Power

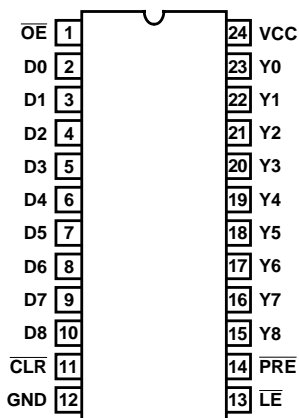
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT844AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT843AM	0 to 70	24 Ld SOIC	M24.3

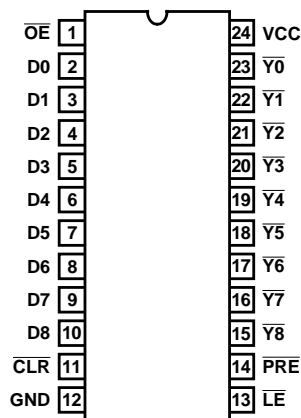
NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Pinouts

CD74FCT843A  
(SOIC)  
TOP VIEW

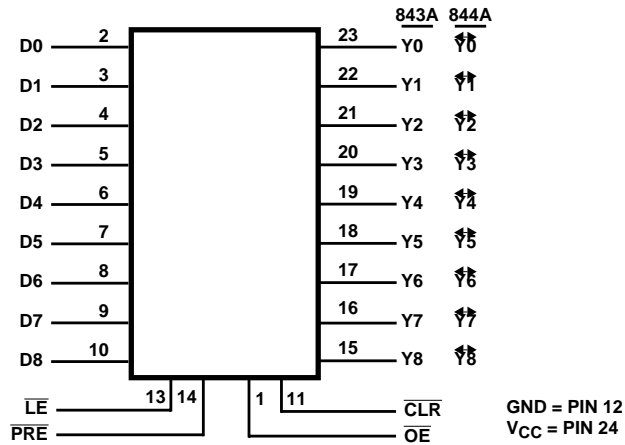


CD74FCT844A  
(PDIP)  
TOP VIEW



## CD74FCT843A, CD74FCT844A

### Functional Diagram



TRUTH TABLE (Note 1)

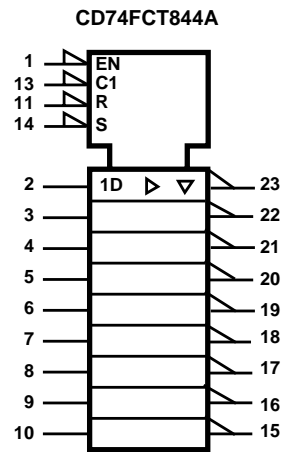
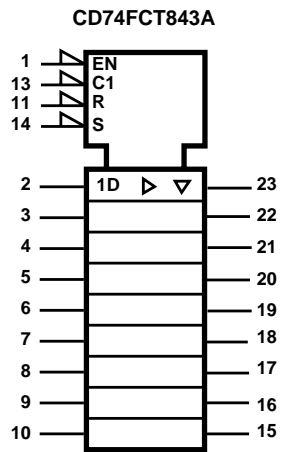
INPUTS						OUTPUTS	FUNCTION
CLR	PRE	OE	LE	843A Dn	844A Dn	Yn	
H	H	H	X	X	X	Z	High Z
H	H	H	L	X	X	Z	Latched (High Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	X	NC	Latched
H	L	L	X	X	X	H	Preset
L	H	L	X	X	X	L	Clear
L	L	L	X	X	X	H	Preset
L	H	H	L	X	X	Z	Latched (High Z)
H	L	H	L	X	X	Z	Latched (High Z)

NOTE:

1. H= HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- NC = No Change
- Z = High Impedance

# CD74FCT843A, CD74FCT844A

## IEC Logic Symbol



## CD74FCT843A, CD74FCT844A

### Absolute Maximum Ratings

DC Supply Voltage ( $V_{CC}$ )	-0.5V to 6V
DC Diode Current, $I_{IK}$ (For $V_I < -0.5V$ )	-20mA
DC Output Diode Current, $I_{OK}$ (for $V_O < -0.5V$ )	-50mA
DC Output Sink Current per Output Pin, $I_O$	70mA
DC Output Source Current per Output Pin, $I_O$	-30mA
DC $V_{CC}$ Current ( $I_{CC}$ )	.237mA
DC Ground Current ( $I_{GND}$ )	.453mA

### Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	75
SOIC Package	75
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s) (SOIC-Lead Tips Only)	300 $^{\circ}C$

### Operating Conditions

Operating Temperature Range, $T_A$	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	4.75V to 5.25V
DC Input Voltage, $V_I$	0 to $V_{CC}$
DC Output Voltage, $V_O$	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	0 to 10ns/V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$ , $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ )				UNITS
		$V_I$ (V)	$I_O$ (mA)		25 $^{\circ}C$		0 $^{\circ}C$ TO 70 $^{\circ}C$		
					MIN	MAX	MIN	MAX	
High Level Input Voltage	$V_{IH}$			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	48	Min	-	0.55	-	0.55	V
High Level Input Current	$I_{IH}$	$V_{CC}$		Max	-	0.1	-	1	$\mu A$
Low Level Input Current	$I_{IL}$	GND		Max	-	-0.1	-	-1	$\mu A$
Three-State Leakage Current	$I_{OZH}$	$V_{CC}$		Max	-	0.5	-	10	$\mu A$
	$I_{OZL}$	GND		Max	-	-0.5	-	-10	$\mu A$
Input Clamp Voltage	$V_{IK}$	$V_{CC}$ or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	$I_{OS}$	$V_O = 0$ $V_{CC}$ or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	Max	-	8	-	80	$\mu A$
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	$\Delta I_{CC}$	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

#### NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at  $V_{CC}$  or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 1.6mA Max. @ 70 $^{\circ}C$ .

## CD74FCT843A, CD74FCT844A

### Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$ , $C_L = 50\text{pF}$ , $R_L$ (Figure 1)

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays						
Data to Outputs	CD74FCT843A	5 (Note 6)	6.8	1.5	9	ns
	CD74FCT844A	5	7.5	1.5	10	ns
$\overline{LE}$ to Outputs	$t_{PLH}, t_{PHL}$	5	9	1.5	12	ns
$\overline{PRE}$ to Outputs	$t_{PLH}$	5	9	1.5	12	ns
$\overline{CLR}$ to Outputs	$t_{PHL}$	5	9.8	1.5	13	ns
Output Enable Times	$t_{PZL}, t_{PZH}$	-	10.5	1.5	14	ns
Output Disable Times	$t_{PLZ}, t_{PHZ}$	-	6	1.5	8	ns
Power Dissipation Capacitance	$C_{PD}$ (Note 7)	-	-	-	-	pF
Minimum (Valley) $V_{OHV}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$	5	0.5	-	-	V
Maximum (Peak) $V_{OLP}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$	5	1	-	-	V
Input Capacitance	$C_I$	-	-	-	10	pF
Three-State Output Capacitance	$C_O$	-	-	-	15	pF

**NOTES:**

- 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
- $C_{PD}$ , measured per flip-flop, is used to determine the dynamic power consumption.  
 $P_D$  (per package) =  $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$  where:  
 $V_{CC}$  = supply voltage  
 $\Delta I_{CC}$  = flow through current x unit load  
 $C_L$  = output load capacitance  
 $D$  = duty cycle of input high  
 $f_O$  = output frequency  
 $f_I$  = input frequency

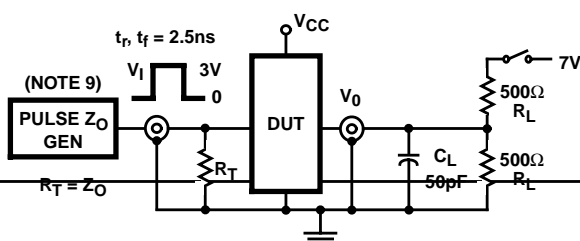
### Prerequisite for Switching

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Setup Time, Data to $\overline{LE}$	$t_{SU}$	5 (Note 8)	-	2.5	-	ns
Hold Time, Data to $\overline{LE}$	$t_H$	5	-	2.5	-	ns
$\overline{LE}$ Pulse Width	$t_W$	5	-	4	-	ns
$\overline{PRE}, \overline{CLR}$ Pulse Width	$t_W$	5	-	8	-	ns
$\overline{PRE}, \overline{CLR}$ Recovery Time	$t_{REC}$	5	-	14	-	ns

**NOTE:**

- Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

### Test Circuits and Waveforms



#### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}, t_{PZL}, \text{Open Drain}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

**DEFINITIONS:**

$C_L$  = Load capacitance, includes jig and probe capacitance.

$R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

**NOTE:**

- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;

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