Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

# CY74FCT2373T
# CY74FCT2573T

SCCS039 - September 1994 - Revised March 2000

## 8-Bit Latches

### Features

- **Function and pinout compatible with the fastest bipolar logic**
- **25Ω output series resistors to reduce transmission line refelection noise**
- **FCT-C speed at 4.7 ns max.**
- **Reduced $V_{OH}$ (typically=3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **ESD > 2000V**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 12 mA**
  **Source current 15 mA**
- **Extended commercial temp. range of –40˚C to +85˚C**

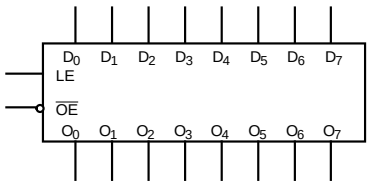
### Functional Description

The FCT2373T and FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. FCT2373T can be used to replace FCT373T, and FCT2573T to replace FCT573T to reduce noise in an existing design.

When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

### Logic Symbol

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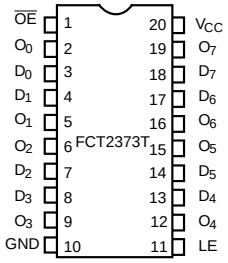
### Pin Configurations

**SOIC/QSOP**
**Top View**

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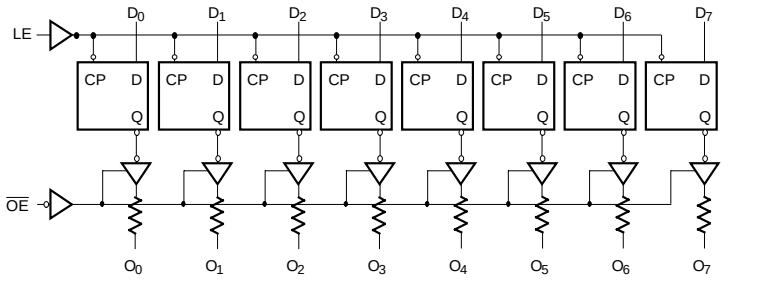
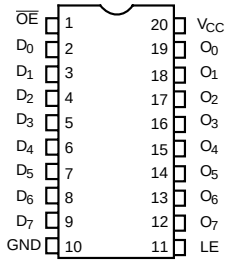
### Logic Block Diagram




FCT2373T-2

**SOIC/QSOP**
**Top View**




FCT2373T-6

## Function Table[1]

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | LE | D | O |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation .....0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | –40°C to +85°C | 5V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=–15 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=12 mA | | 0.3 | 0.55 | V |
| $R_{OUT}$ | Output Resistance | $V_{CC}$=Min., $I_{OL}$=12 mA | 20 | 28 | 40 | Ω |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_H$ | Hysteresis[6] | All inputs | | 0.2 | | V |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$=Min., $I_{IN}$=–18 mA | | –0.7 | –1.2 | V |
| $I_I$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=$V_{CC}$ | | | 5 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=2.7V | | | ±1 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$=Max., $V_{IN}$=0.5V | | | ±1 | µA |
| $I_{OZH}$ | Off State HIGH-Level Output Current | $V_{CC}$=Max., $V_{OUT}$=2.7V | | | 10 | µA |
| $I_{OZL}$ | Off State LOW-Level Output Current | $V_{CC}$=Max., $V_{OUT}$=0.5V | | | –10 | µA |
| $I_{OS}$ | Output Short Circuit Current[7] | $V_{CC}$=Max., $V_{OUT}$=0.0V | –60 | –120 | –225 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$=0V, $V_{OUT}$=4.5V | | | ±1 | µA |

**Notes:**

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = HIGH Impedance
   $Q_n$ = Previous state of flip flops ($Q_{n-1}$)
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.
4. $T_A$ is the "instant on" case temperature.
5. Typical values are at $V_{CC}$=5.0V, $T_A$=+25°C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## Capacitance[6]

| Parameter | Description | Typ.[5] | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | 8 | 12 | pF |

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$ | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs) | $V_{CC}$=Max., $V_{IN}$=3.4V,[8] $f_1$=0, Outputs Open | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[9] | $V_{CC}$=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 0.06 | 0.12 | mA/ MHz |
| $I_C$ | Total Power Supply Current[10] | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=10 MHz, $\overline{OE}$=GND, LE=$V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 0.7 | 1.4 | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=10 MHz, $\overline{OE}$=GND, LE=$V_{CC}$, $V_{IN}$=3.4V or $V_{IN}$=GND | 1.0 | 2.4 | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=2.5 MHz, $\overline{OE}$=GND, LE=$V_{CC}$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 1.3 | 2.6[11] | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=2.5 MHz, $\overline{OE}$=GND, LE=$V_{CC}$, $V_{IN}$=3.4V or $V_{IN}$=GND | 3.3 | 10.6[11] | mA |

**Notes:**

8. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    $I_{CC}$ = Quiescent Current with CMOS input levels
    $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input ($V_{IN}$=3.4V)
    $D_H$ = Duty Cycle for TTL inputs HIGH
    $N_T$ = Number of TTL inputs at $D_H$
    $I_{CCD}$ = Dynamic Current caused by an input transition pair (HLH or LHL)
    $f_0$ = Clock frequency for registered devices, otherwise zero
    $f_1$ = Input signal frequency
    $N_1$ = Number of inputs changing at $f_1$
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the $I_{CC}$ formula. These limits are specified but not tested.

## Switching Characteristics Over the Operating Range[12]

| Parameter | Description | CY74FCT2373T CY74FCT2573T | | CY74FCT2373AT CY74FCT2573AT | | CY74FCT2373CT CY74FCT2573CT | | Unit | Fig. No.[13] |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay D to O | 1.5 | 8.0 | 1.5 | 5.2 | 1.5 | 4.2 | ns | 1, 3 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay LE to O | 2.0 | 13.0 | 2.0 | 8.5 | 2.0 | 5.5 | ns | 1, 5 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time | 1.5 | 11.0 | 1.5 | 6.5 | 1.5 | 5.5 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time | 1.5 | 7.0 | 1.5 | 5.5 | 1.5 | 5.0 | ns | 1, 7, 8 |
| $t_S$ | Set-Up Time, HIGH to LOW D to LE | 2.0 | | 2.0 | | 2.0 | | ns | 9 |
| $t_H$ | Hold Time, HIGH to LOW D to LE | 1.5 | | 1.5 | | 1.5 | | ns | 9 |
| $t_W$ | LE Pulse Width HIGH | 6.0 | | 5.0 | | 5.0 | | ns | 5 |

12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 4.2 | CY74FCT2373CTQCT | Q5 | 20-Lead (150-Mil) QSOP | Commercial |
| | CY74FCT2373CTSOC/SOCT | S5 | 20-Lead (300-Mil) Molded SOIC | |
| 5.2 | CY74FCT2373ATQCT | Q5 | 20-Lead (150-Mil) QSOP | Commercial |
| | CY74FCT2373ATSOC/SOCT | S5 | 20-Lead (300-Mil) Molded SOIC | |
| 8.0 | CY74FCT2373TQCT | Q5 | 20-Lead (150-Mil) QSOP | Commercial |

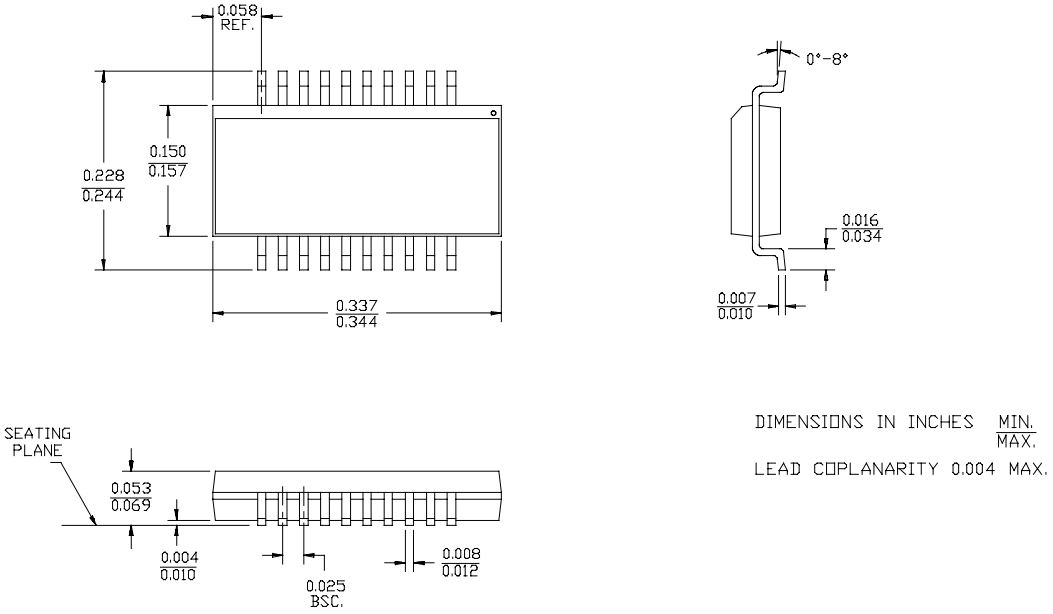
## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 4.2 | CY74FCT2573CTQCT | Q5 | 20-Lead (150-Mil) QSOP | Commercial |
| | CY74FCT2573CTSOC/SOCT | S5 | 20-Lead (300-Mil) Molded SOIC | |
| 5.2 | CY74FCT2573ATQCT | Q5 | 20-Lead (150-Mil) QSOP | Commercial |
| 8.0 | CY74FCT2573TSOC/SOCT | S5 | 20-Lead (300-Mil) Molded SOIC | Commercial |

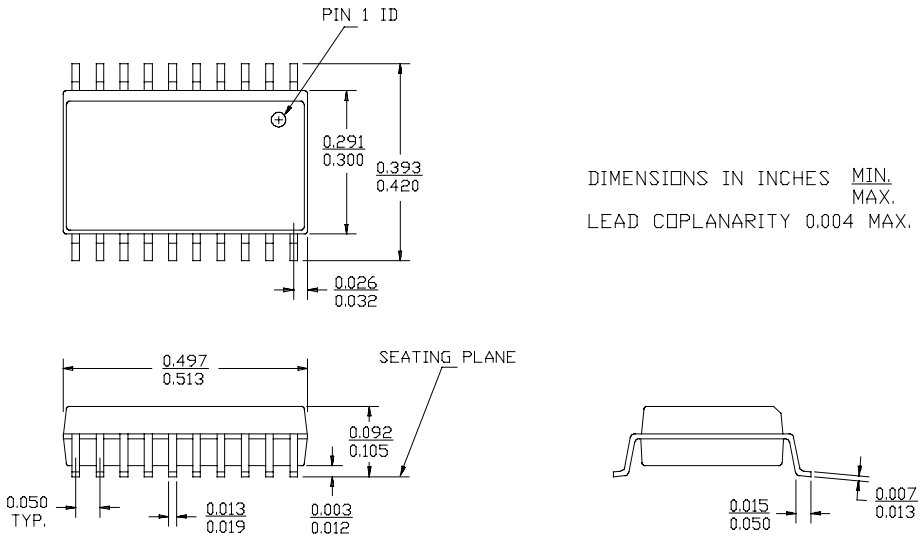
Document #: 38–00338–B

## Package Diagrams

**20-Lead Quarter Size Outline Q5**




**20-Lead (300-Mil) Molded SOIC S5**



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