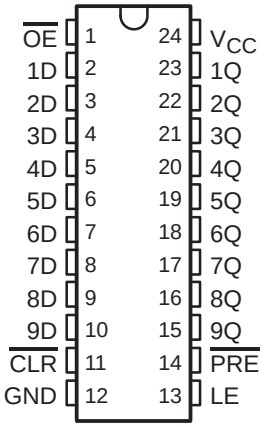
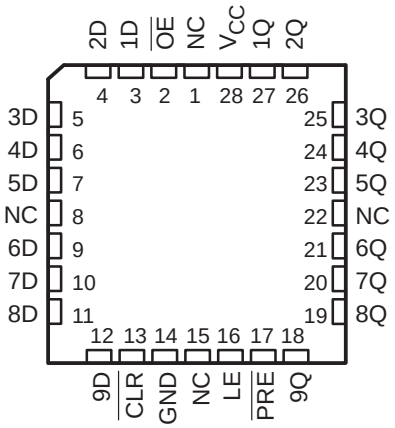
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT843 . . . JT OR W PACKAGE
SN74ABT843 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT843 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABT843 9-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine transparent D-type latches provide true data at the outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

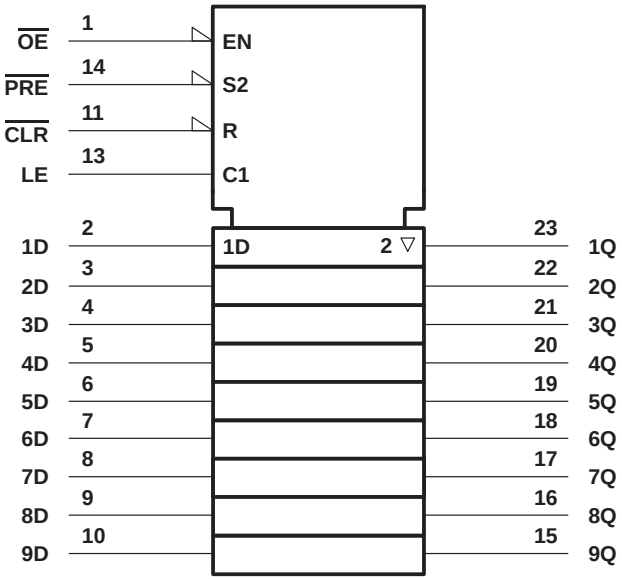
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT843 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT843 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

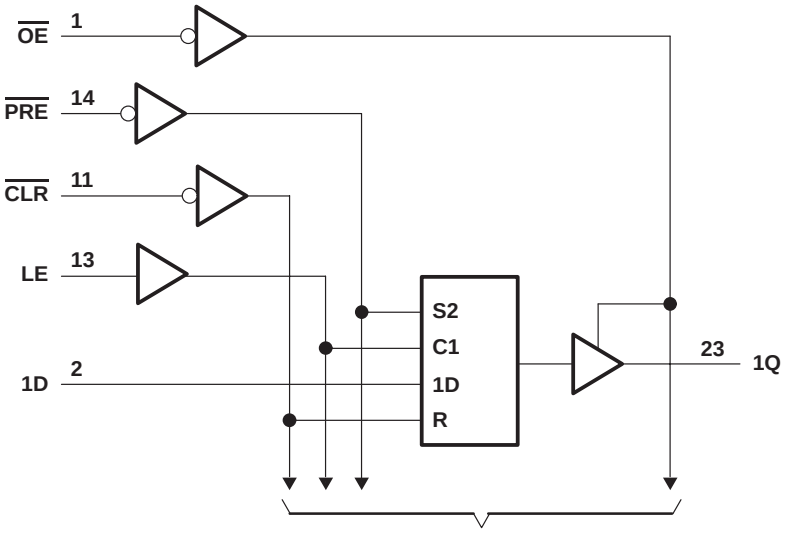
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT843 . . . . . 96 mA
SN74ABT843 . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
NT package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT843		SN74ABT843		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT843		SN74ABT843		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA					2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA						0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
V_{hys}					100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				10		10		10	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–10		–10		–10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–140	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = Open, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	34		34		34	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				4						pF
C_o	V_O = 2.5 V or 0.5 V				7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

				V_{CC} = 5 V, T_A = 25°C		SN54ABT843		SN74ABT843		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low		5.5		5.5		5.5		ns
		$\overline{PRE}$ low		4.5		4.5		4.5		
		LE low		3.3		3.3		3.4		
t_{su}	Setup time	Data before LE↓	Low	2.5		2.5		2.5		ns
			High	3		3		3		
		$\overline{PRE}$ inactive		1.6		1.6		1.6		
		$\overline{CLR}$ inactive		2		2		2		
t_h	Hold time, data after LE↓	High		1		1		1		ns
		Low		1.5†		2.3†		1.5†		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT843		SN74ABT843		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.2†	3.8	5.2	1.2†	7.8	1.2†	6.7†	ns
t_{PHL}			1.5†	3.4	6.3	1.5†	7.3	1.5†	7.2	
t_{PLH}	LE	Q	1.7†	4.4	5.6	1.7†	8.3	1.7†	7.2†	ns
t_{PHL}			1.9†	4.1	6.3	1.3†	7.2	1.9†	6.9	
t_{PLH}	$\overline{PRE}$	Q	2.2	5	6.2	2.2	8.3	2.2	7.4	ns
t_{PHL}			2.1†	4.1	6.5	2.1†	7.5	2.1†	7.2	
t_{PLH}	$\overline{CLR}$	Q	2†	4.4	6.3	2†	7.6	2†	7.1	ns
t_{PHL}			1.9†	4.5	6.8	1.9†	8.1	1.9†	8	
t_{PZH}	$\overline{OE}$	Q	1	3.4	4.5†	1	6.4	1	5.7†	ns
t_{PZL}			2	4.3	5.7†	2	6.6	2	6.5	
t_{PHZ}	$\overline{OE}$	Q	2.4†	4.9	6.2	2.4†	7.3	2.4†	6.8	ns
t_{PLZ}			1.5†	4.2	6.3	1.5†	7	1.5†	5.9†	

† This data sheet limit may vary among suppliers.

recovery-time waveform

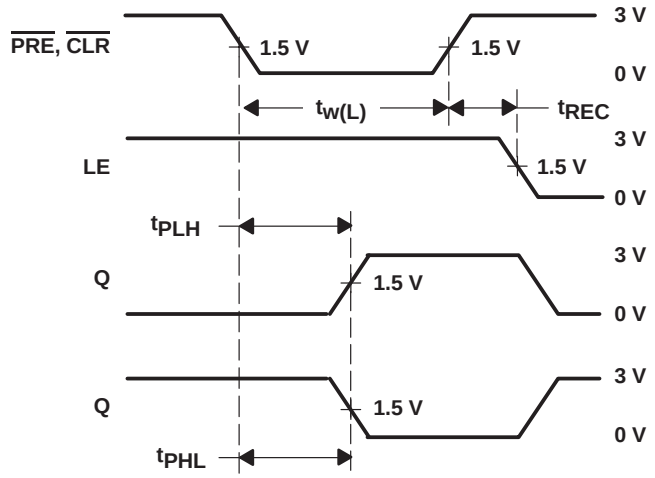
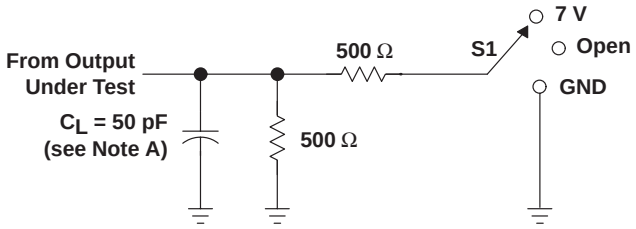


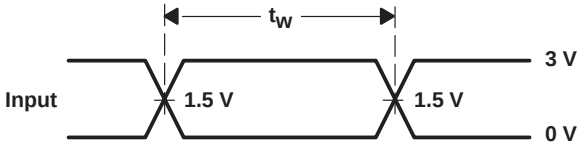
Figure 1. $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ Pulse Duration, $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ to Output Delay, and $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ to Latch-Enable Recovery Time

PARAMETER MEASUREMENT INFORMATION

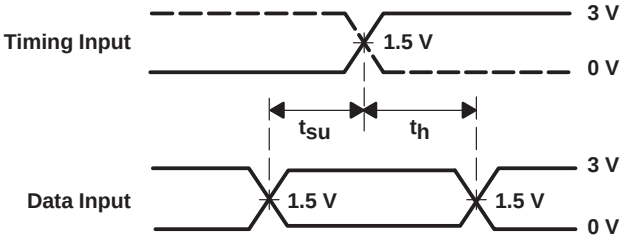


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

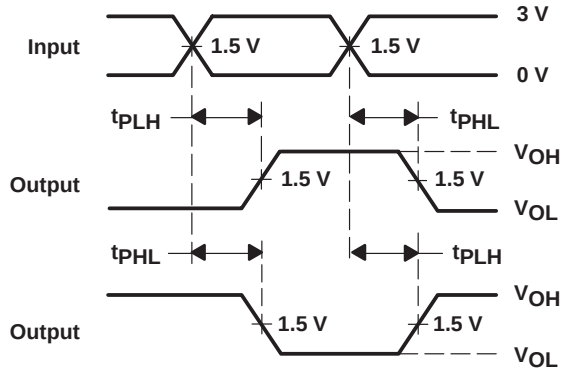
LOAD CIRCUIT



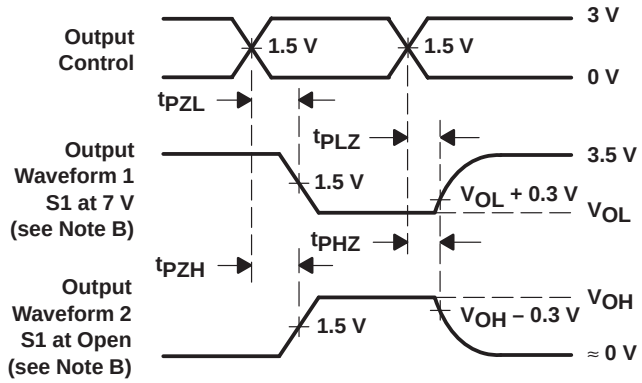
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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