

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art EPIC-II[™] BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

description

These octal transparent D-type latches with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the \bar{Q} outputs follow the complements of the data (D) inputs. When LE is taken low, the \bar{Q} outputs are latched at the inverse of the levels at the D inputs.

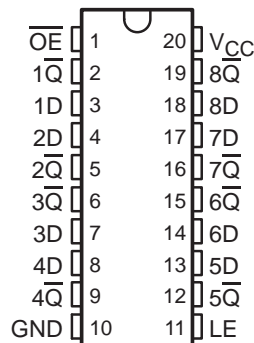
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

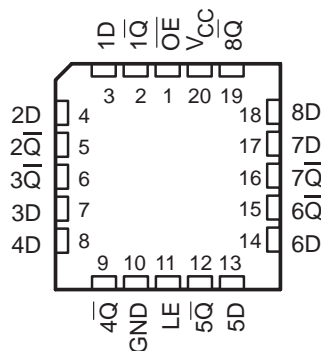
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT533 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT533A is characterized for operation from -40°C to 85°C .

SN54ABT533 . . . J OR W PACKAGE
SN74ABT533A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT533 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II[™] is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

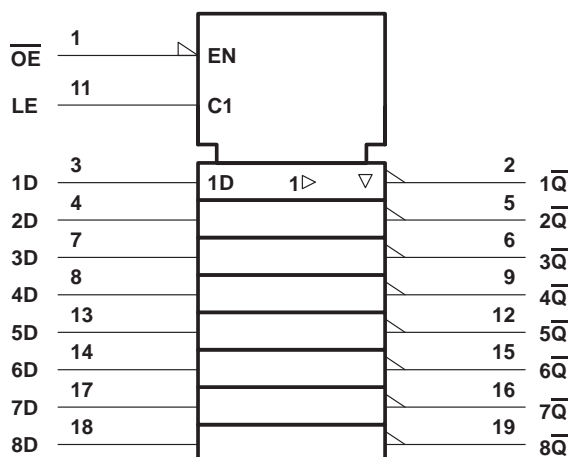
SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

FUNCTION TABLE
(each latch)

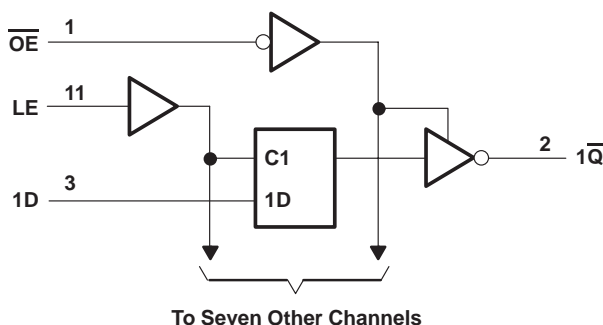
INPUTS			OUTPUT
\overline{OE}	LE	D	\overline{Q}
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT533	96 mA
SN74ABT533A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

recommended operating conditions (see Note 3)

		SN54ABT533		SN74ABT533A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT533		SN74ABT533A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2			
		I _{OH} = -32 mA	2*					2	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*			0.55		
V _{hys}			100						mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10		10		10	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10		-10		-10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±150				±150	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50	50	50	50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-140	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			1	250	250	250	μA
		Outputs low			24	30	30	30	mA
		Outputs disabled			0.5	250	250	250	μA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs high			1.5		1.5	1.5	mA
		Outputs low			1.5		1.5	1.5	
		Outputs disabled			1.5		1.5	1.5	
C _i	V _I = 2.5 V or 0.5 V			3.5					pF
C _o	V _O = 2.5 V or 0.5 V			6.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT533, SN74ABT533A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT533				UNIT	
		V _{CC} = 5 V, T _A = 25°C			MIN		MAX
		MIN	MAX				
t _w	Pulse duration, LE high		3.3		3.3	ns	
t _{su}	Setup time, data before LE↓	High or low	2.1		2.1	ns	
t _h	Hold time, data after LE↓	High or low	1.5		1.5	ns	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN74ABT533A				UNIT	
		V _{CC} = 5 V, T _A = 25°C			MIN		MAX
		MIN	MAX				
t _w	Pulse duration, LE high		3.3		3.3	ns	
t _{su}	Setup time, data before LE↓	High or low	2.1		2.1	ns	
t _h	Hold time, data after LE↓	High or low	2.1		2.1	ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT533					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	D	Q̄	1.9	4.2	5.4	1.9	6.7	ns
t _{PHL}			3.1	4.9	6.3	3.1	6.9	
t _{PLH}	LE	Q̄	2.7	4.9	6.2	2.7	7.6	ns
t _{PHL}			3.5	5.4	6.8	3.5	7.5	
t _{PZH}	OĒ	Q̄	1.6	3.7	4.8	1.6	5.8	ns
t _{PZL}			2.4	4.2	6.2	2.4	6.9	
t _{PHZ}	OĒ	Q̄	2.8	5.1	6.2	2.8	7.2	ns
t _{PLZ}			2	4.1	6	2	6.9	



SN54ABT533, SN74ABT533A
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

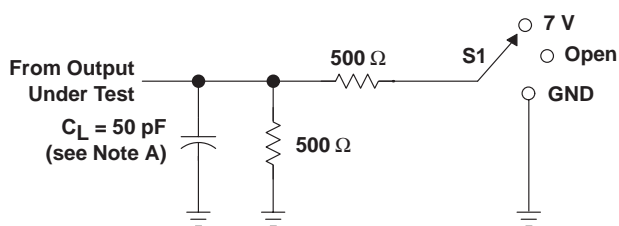
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT533A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	D	\bar{Q}	1.7	4.2	5.4	1.7	6.4	ns
t_{PHL}			2.6	4.9	6.3	2.6	6.6	
t_{PLH}	LE	\bar{Q}	2.7	4.9	6.2	2.7	7.3	ns
t_{PHL}			3.5	5.4	6.8	3.5	7.3	
t_{PZH}	\bar{OE}	\bar{Q}	1.6	3.7	4.8	1.6	5.7	ns
t_{PZL}			2.4	4.2	6.2	2.4	6.7	
t_{PHZ}	\bar{OE}	\bar{Q}	1.6	5.1	6.2	1.6	6.9	ns
t_{PLZ}			2	4.1	6	2	6.5	

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

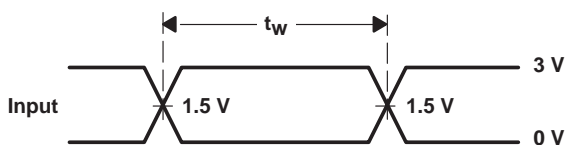
SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

PARAMETER MEASUREMENT INFORMATION

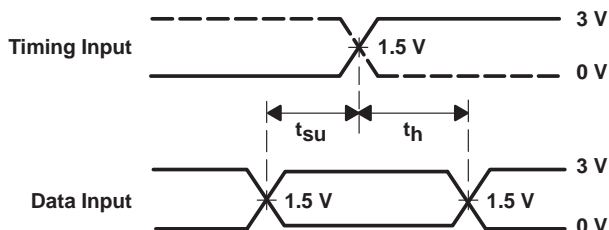


LOAD CIRCUIT

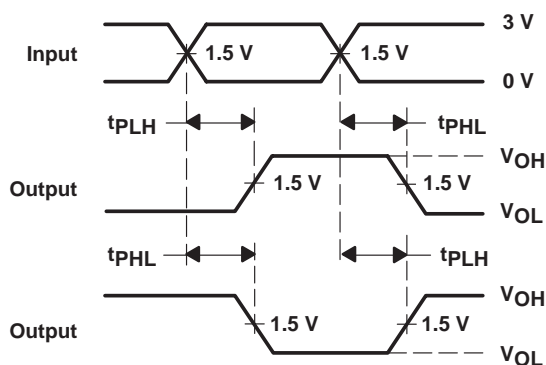
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



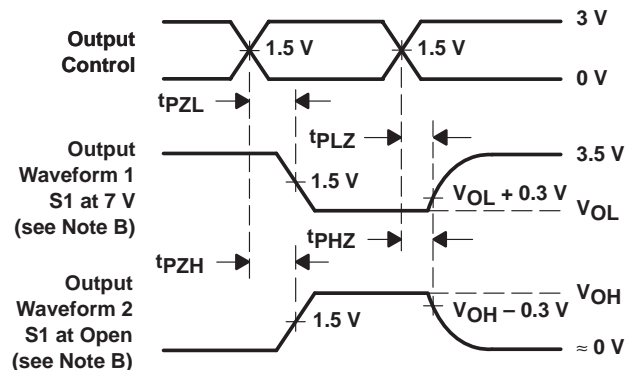
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.