

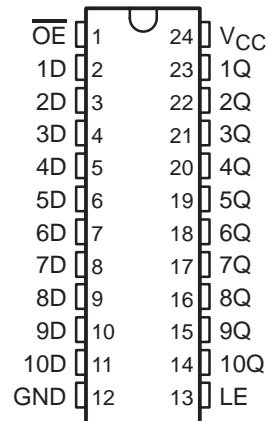
SN74ALS29841

10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS149A – JUNE 1988 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

This 10-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The SN74ALS29841 has noninverting data (D) inputs.

A buffered output-enable (\overline{OE}) input can place the ten outputs in either a normal logic state (high or low logic levels) or in a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS29841 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

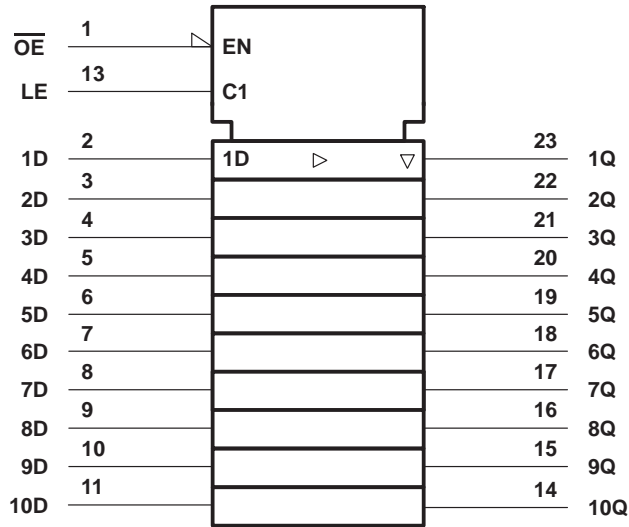
INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN74ALS29841

10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

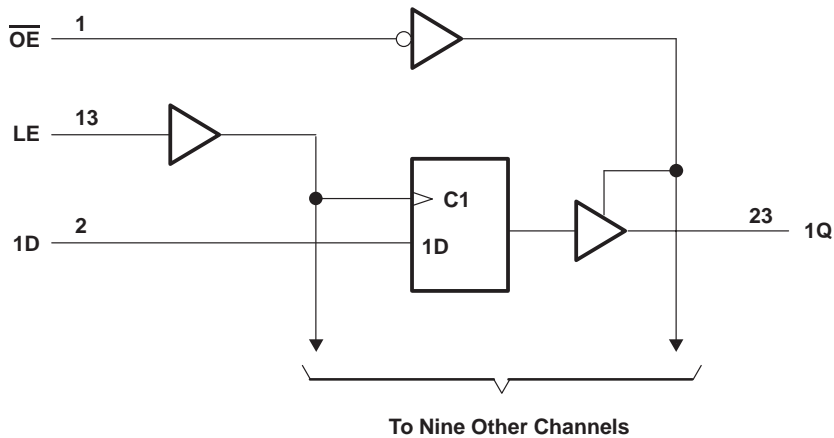
SDAS149A – JUNE 1988 – REVISED JANUARY 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS29841
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

SDAS149A – JUNE 1988 – REVISED JANUARY 1995

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, LE high	6			ns
t_{su}	Setup time, data before LE↓	2.5			ns
t_h	Hold time, data after LE↓	4.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.75\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.75\text{ V}$		2.4	3.3	V
			2	3.1	
V_{OL}	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 48\text{ mA}$		0.35	0.5	V
I_{OZH}	$V_{CC} = 5.25\text{ V}$, $V_O = 2.7\text{ V}$			20	μA
I_{OZL}	$V_{CC} = 5.25\text{ V}$, $V_O = 0.4\text{ V}$			-20	μA
I_I	$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.25\text{ V}$, $V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$			-0.2	mA
$I_{OS}‡$	$V_{CC} = 5.25\text{ V}$, $V_O = 0$	-75		-250	mA
I_{CC}	$V_{CC} = 5.25\text{ V}$, Outputs low		55	85	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN74ALS29841
10-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

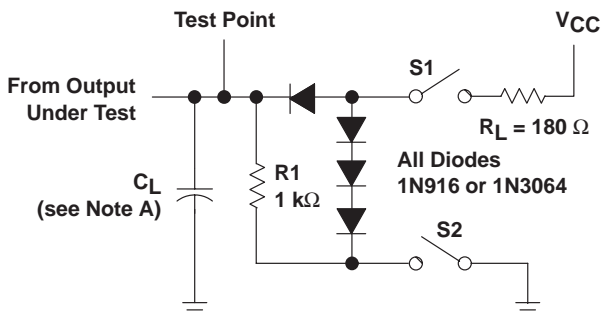
SDAS149A – JUNE 1988 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = MIN to MAX†, T _A = MIN to MAX†		UNIT
				MIN	MAX	
t _{PLH}	D	Any Q	C _L = 50 pF	2	9.5	ns
t _{PHL}				2	9.5	
t _{PLH}	D	Any Q	C _L = 300 pF		14	ns
t _{PHL}					14	
t _{PLH}	LE	Any Q	C _L = 50 pF		12	ns
t _{PHL}					12	
t _{PLH}	LE	Any Q	C _L = 300 pF		16	ns
t _{PHL}					16	
t _{PZH}	\overline{OE}	Any Q	C _L = 50 pF		14	ns
t _{PZL}					14	
t _{PZH}	\overline{OE}	Any Q	C _L = 300 pF		20	ns
t _{PZL}					23	
t _{PHZ}	\overline{OE}	Any Q	C _L = 50 pF		15	ns
t _{PLZ}					12	
t _{PHZ}	\overline{OE}	Any Q	C _L = 5 pF		9	ns
t _{PLZ}					9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

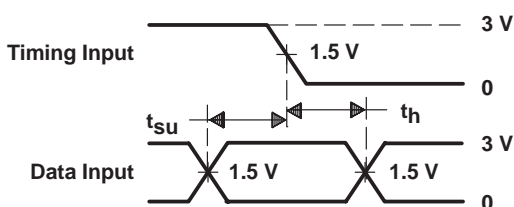
PARAMETER MEASUREMENT INFORMATION



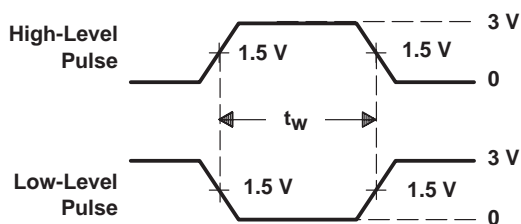
LOAD CIRCUIT

SWITCH POSITION TABLE

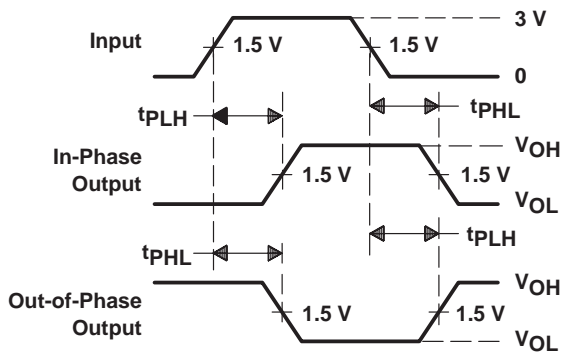
TEST	S1	S2
t _{PLH}	Closed	Closed
t _{PHL}	Closed	Closed
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed



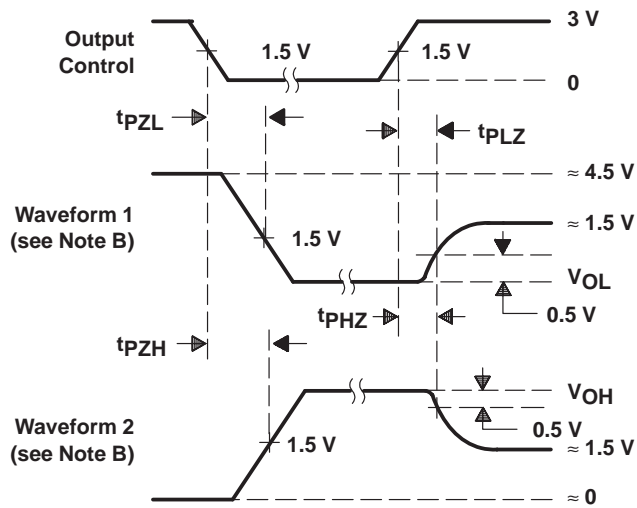
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.