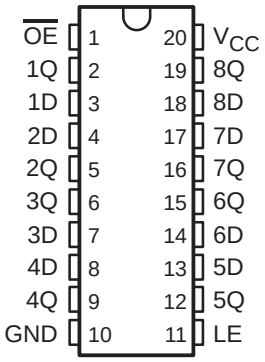
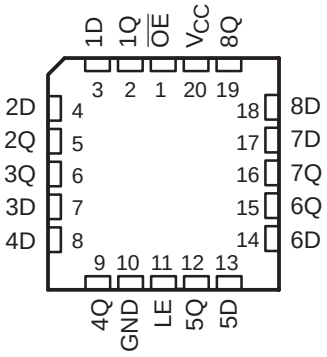
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV373A . . . J OR W PACKAGE
SN74LV373A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV373A . . . FK PACKAGE
(TOP VIEW)



description

The ’LV373A devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

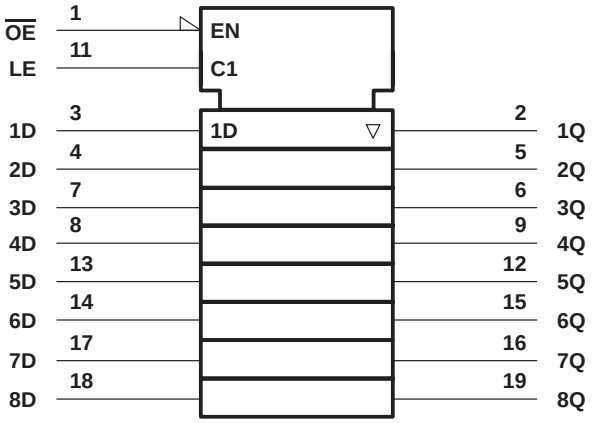
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV373A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV373A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

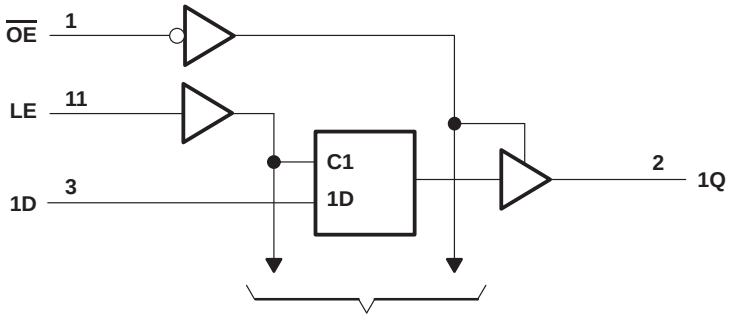
INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	–20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DGV package	146°C/W
DW package	97°C/W
NS package	100°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–8		–8	
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV373A			SN74LV373A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –8 mA	3 V	2.48			2.48			
	I_{OH} = –16 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	5.5 V			±1			±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.9			2.9		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		6		6.5		6.5		ns
t_{su}	Setup time, data before LE↓	High or low	4.5		5		5		ns
t_h	Hold time, data after LE↓	High or low	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE↓	High or low	4		4		4		ns
t_h	Hold time, data after LE↓	High or low	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE↓	High or low	4		4		4		ns
t_h	Hold time, data after LE↓	High or low	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}*	D	Q	C_L = 15 pF		8.3	15.2	1	17	1	17	ns
	LE	Q			9.1	15.7	1	19	1	19	
t_{en}*	$\overline{OE}$	Q			8.9	15.8	1	19	1	19	
t_{dis}*	$\overline{OE}$	Q			6.2	12.6	1	15	1	15	
t_{pd}	D	Q	C_L = 50 pF		10.4	18	1	21	1	21	ns
	LE	Q			11.1	18.6	1	22	1	22	
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	22	
t_{dis}	$\overline{OE}$	Q			8.3	17.4	1	19	1	19	
$t_{sk(o)}$†						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}*	D	Q	C_L = 15 pF		5.8	11.4	1	13.5	1	13.5	ns
	LE	Q			6.4	11	1	13	1	13	
t_{en}*	$\overline{OE}$	Q			6.3	11.4	1	13.5	1	13.5	
t_{dis}*	$\overline{OE}$	Q			4.7	10	1	12	1	12	
t_{pd}	D	Q	C_L = 50 pF		7.3	14.9	1	17	1	17	ns
	LE	Q			7.8	14.5	1	16.5	1	16.5	
t_{en}	$\overline{OE}$	Q			7.7	14.9	1	17	1	17	
t_{dis}	$\overline{OE}$	Q			6	13.2	1	15	1	15	
$t_{sk(o)}$†						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}*	D	Q	C_L = 15 pF		4.1	7.2	1	8.5	1	8.5	ns
	LE	Q			4.5	7.2	1	8.5	1	8.5	
t_{en}*	$\overline{OE}$	Q			4.5	8.1	1	9.5	1	9.5	
t_{dis}*	$\overline{OE}$	Q			3.3	7.2	1	8.5	1	8.5	
t_{pd}	D	Q	C_L = 50 pF		5.1	9.2	1	10.5	1	10.5	ns
	LE	Q			5.5	9.2	1	10.5	1	10.5	
t_{en}	$\overline{OE}$	Q			5.5	10.1	1	11.5	1	11.5	
t_{dis}	$\overline{OE}$	Q			4	9.2	1	10.5	1	10.5	
$t_{sk(o)}$†						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

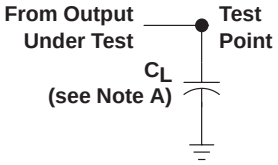
PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.58	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.56	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.86		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

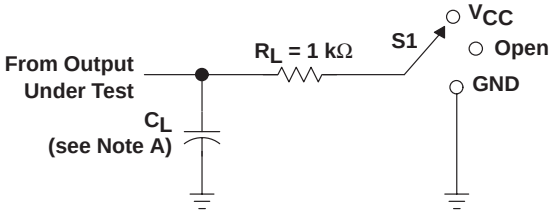
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	17.4	pF
					5 V	19.5	

PARAMETER MEASUREMENT INFORMATION

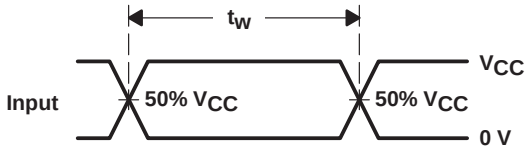


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

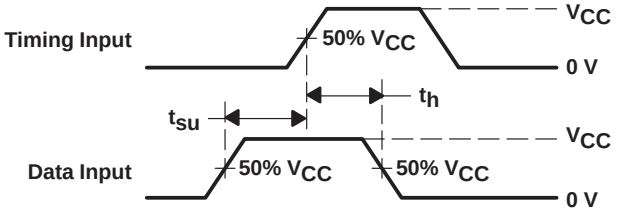


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

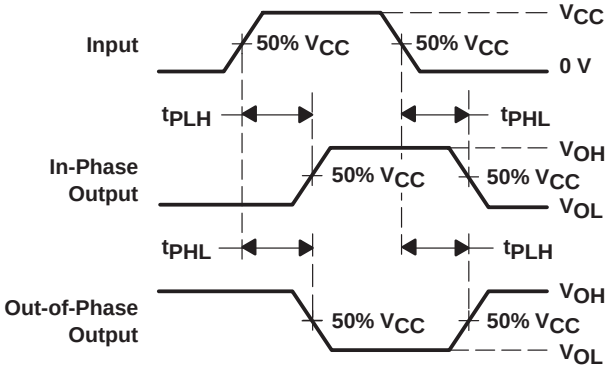
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



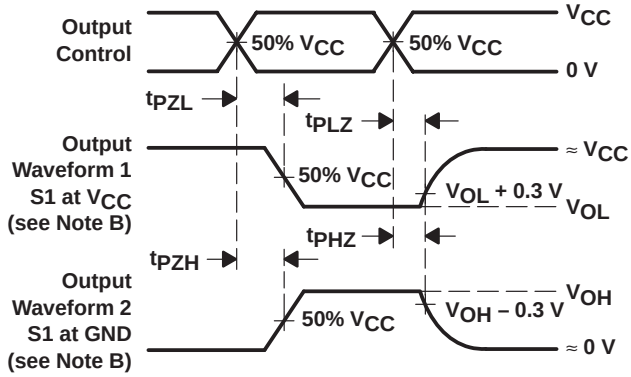
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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