SN74LVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC* ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2$\overline{OE}$	24	25	2LE

description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.
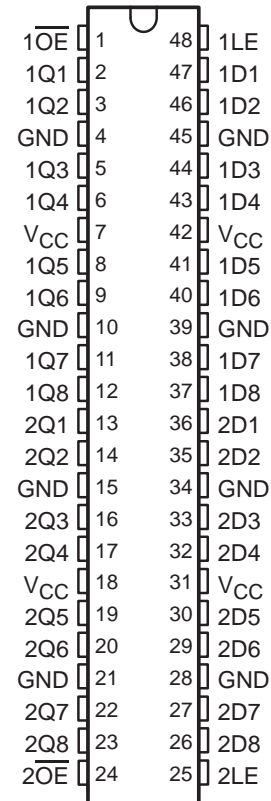
$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16373 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol[†]
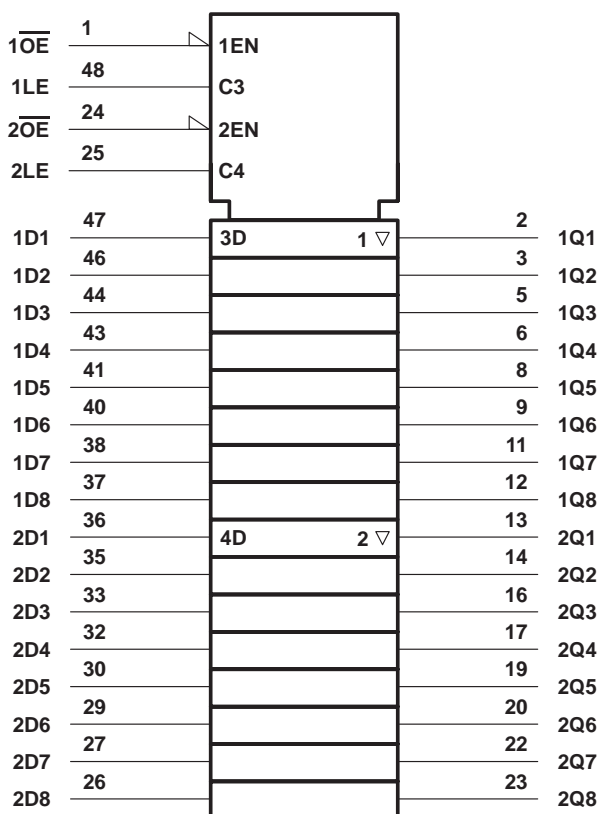
logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
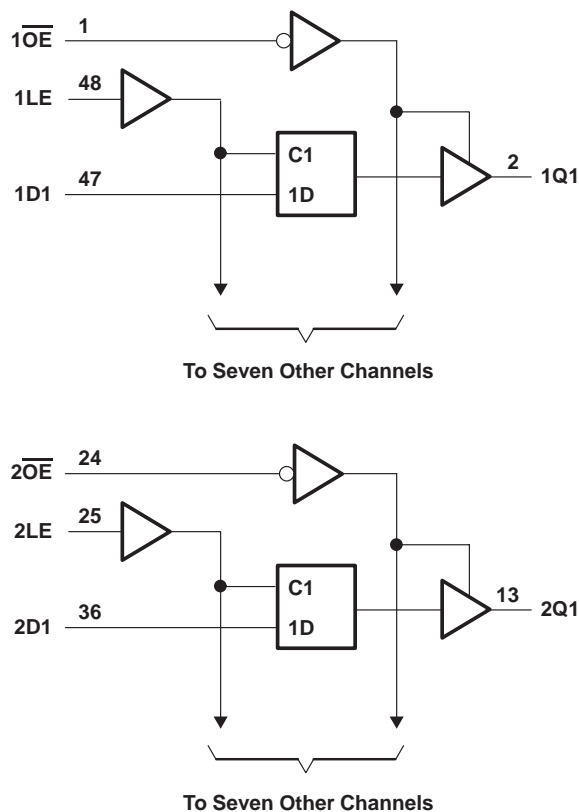
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 4.6 V

Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA

Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA

Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA

Continuous current through V_{CC} or GND .... ±100 mA

Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 3): DGG package .... 0.85 W

DL package .... 1.2 W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7$ V		−12	mA
		$V_{CC} = 3$ V		−24	
I_{OL}	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta V$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN TYP‡ MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		MIN to MAX	$V_{CC} - 0.2$	V
		$I_{OH} = -12\ mA$		2.7	2.2	
				3	2.4	
		$I_{OH} = -24\ mA$		3	2	
V_{OL}		$I_{OL} = 100\ \mu A$		MIN to MAX	0.2	V
		$I_{OL} = 12\ mA$		2.7	0.4	
		$I_{OL} = 24\ mA$		3	0.55	
I_I		$V_I = V_{CC}$ or GND		3.6	±5	μA
$I_{I(hold)}$	Data inputs	$V_I = 0.8\ V$		3	75	μA
		$V_I = 2\ V$			−75	
I_{OZ}		$V_O = V_{CC}$ or GND		3.6	±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6	40	μA
ΔI_{CC}		One input at $V_{CC} - 0.6\ V$,	Other inputs at V_{CC} or GND	3 V to 3.6 V	500	μA
C_i		$V_I = V_{CC}$ or GND		3.3	3.5	pF
C_o		$V_O = V_{CC}$ or GND		3.3	7	pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25°C$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\ V \pm 0.3\ V$		$V_{CC} = 2.7\ V$		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		4		ns
t_{su}	Setup time, data before LE↓	2		2		ns
t_h	Hold time, data after LE↓	2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\ pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\ V \pm 0.3\ V$		$V_{CC} = 2.7\ V$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	D	Q	1.5	7		8	ns
	LE		2	8		9	
t_{en}	$\overline{OE}$	Q	1.5	8		9	ns
t_{dis}	$\overline{OE}$	Q	1.5	7		8	ns

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	Outputs enabled	$C_L = 50\ pF$, f = 10 MHz	20	pF
	Outputs disabled		4	

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PARAMETER MEASUREMENT INFORMATION
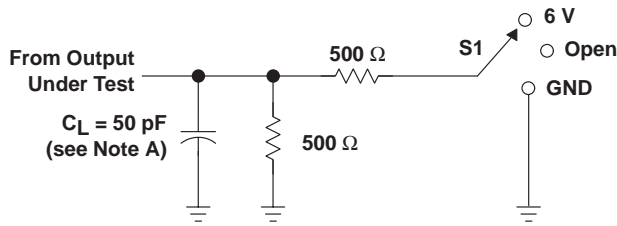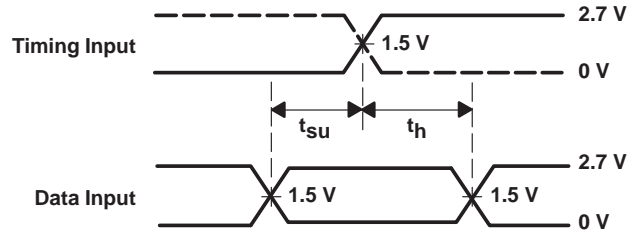
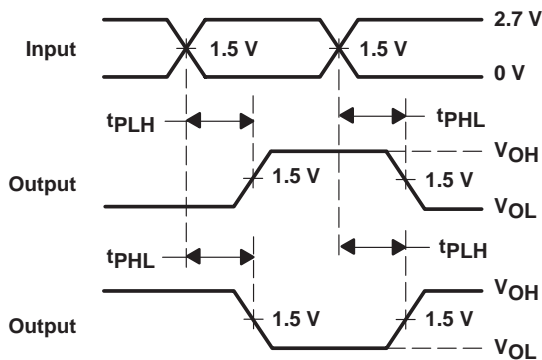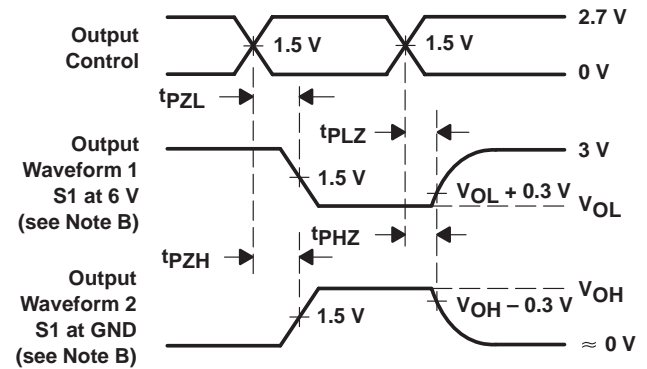| TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS
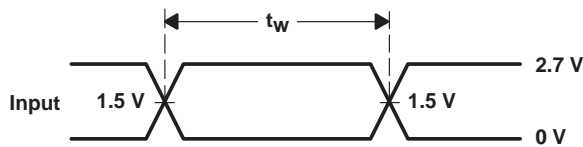
**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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