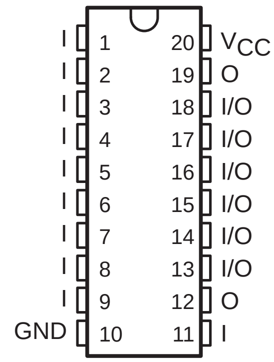
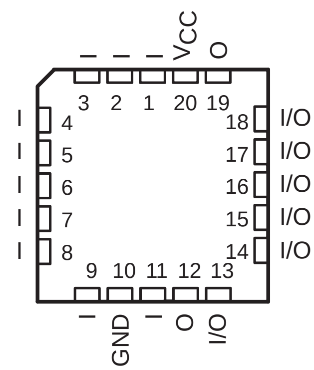
- **High-Performance Operation:**
  f_{max} (no feedback)
  TIBPAL16R’ -5C Series . . . 125 MHz Min
  TIBPAL16R’ -7M Series . . . 100 MHz Min
  f_{max} (internal feedback)
  TIBPAL16R’ -5C Series . . . 125 MHz Min
  TIBPAL16R’ -7M Series . . . 100 MHz Min
  f_{max} (external feedback)
  TIBPAL16R’ -5C Series . . . 117 MHz Min
  TIBPAL16R’ -7M Series . . . 74 MHz Min
  Propagation Delay
  TIBPAL16L8-5C Series . . . 5 ns Max
  TIBPAL16L8-7M Series . . . 7 ns Max
  TIBPAL16R’ -5C Series
  (CLK-to-Q) . . . 4 ns Max
  TIBPAL16R’ -7M Series
  (CLK-to-Q) . . . 6.5 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
’PAL16L8	10	2	0	6
’PAL16R4	8	0	4 (3-state buffers)	4
’PAL16R6	8	0	6 (3-state buffers)	2
’PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board.

The TIBPAL16’ C series is characterized from 0°C to 75°C. The TIBPAL16’ M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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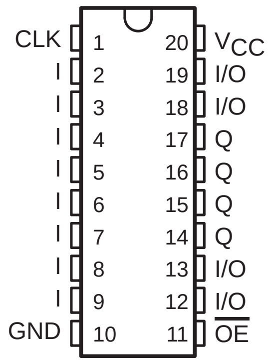
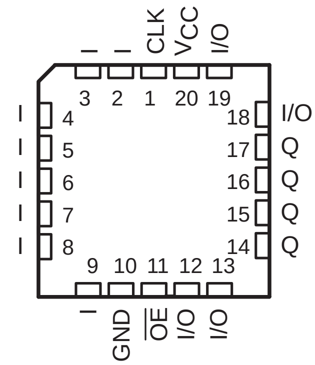
TIBPAL16R4’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



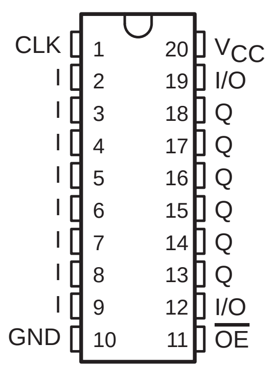
TIBPAL16R4’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



TIBPAL16R6’
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R6’
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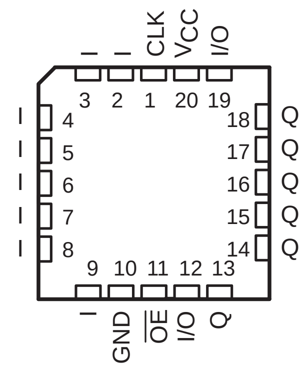
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



TIBPAL16R8’
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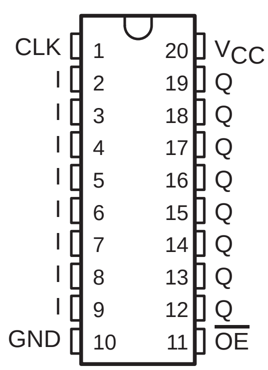
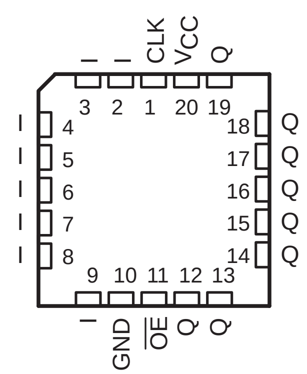
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R8’
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

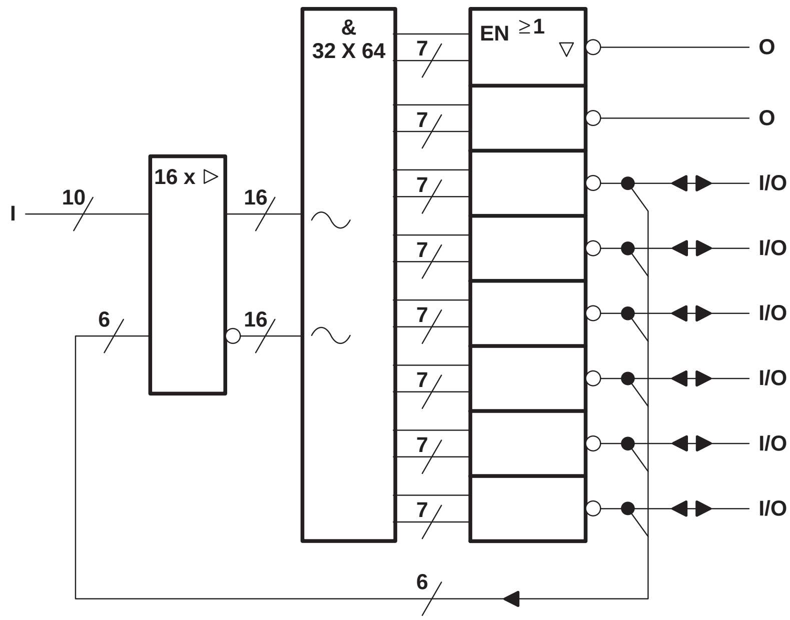
(TOP VIEW)



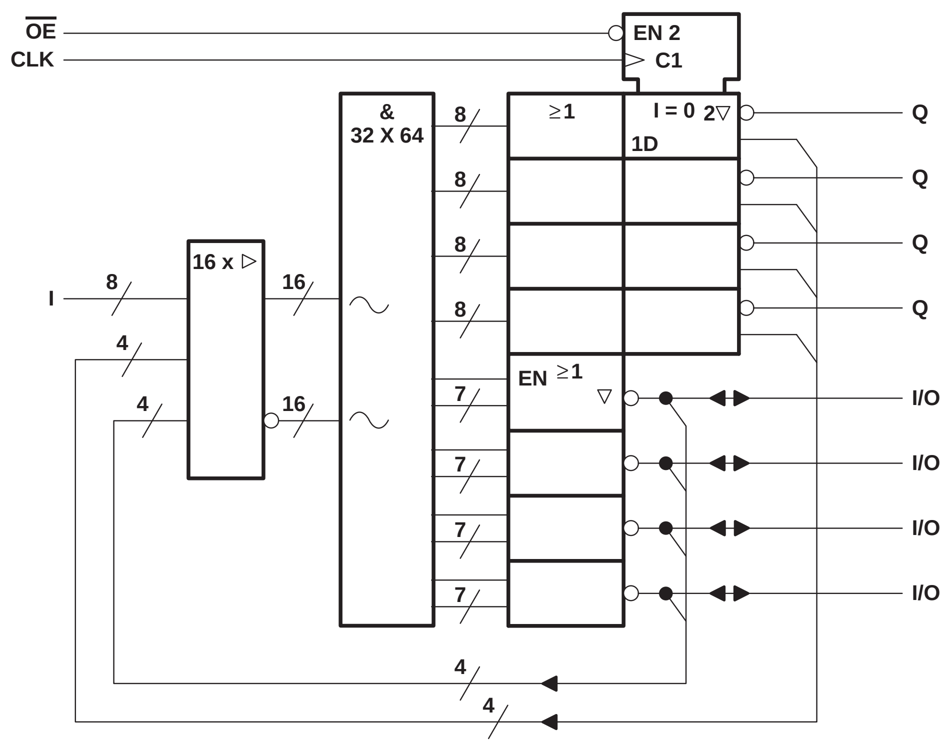
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8’



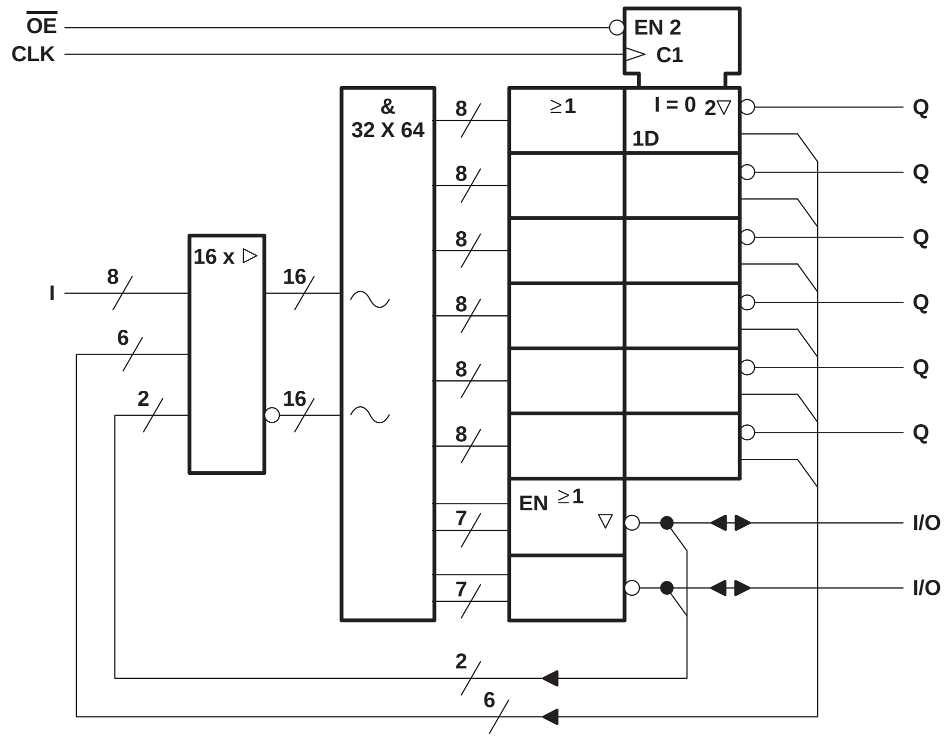
TIBPAL16R4’



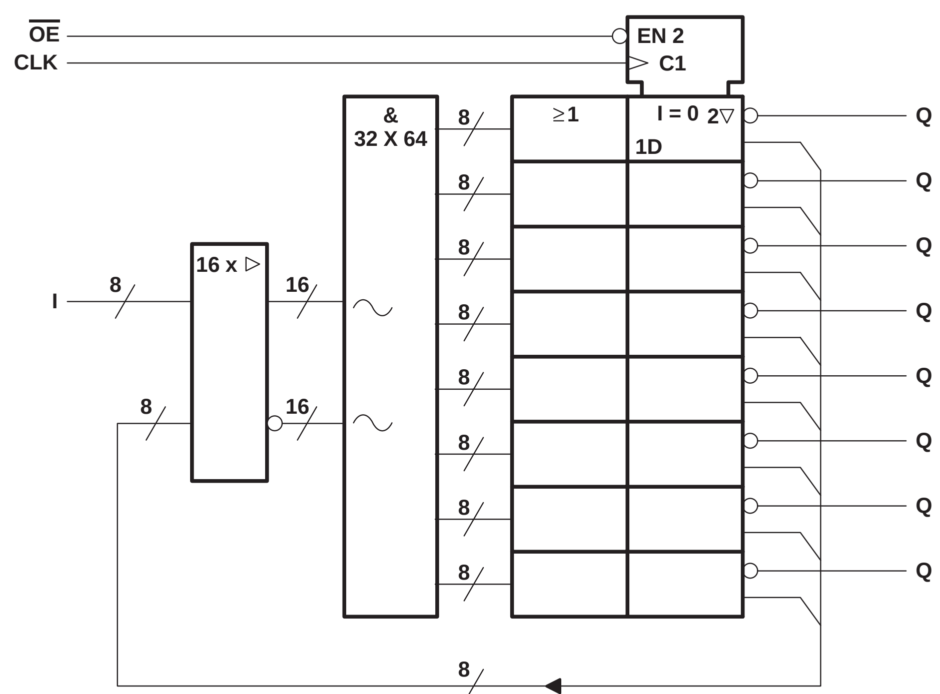
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6’

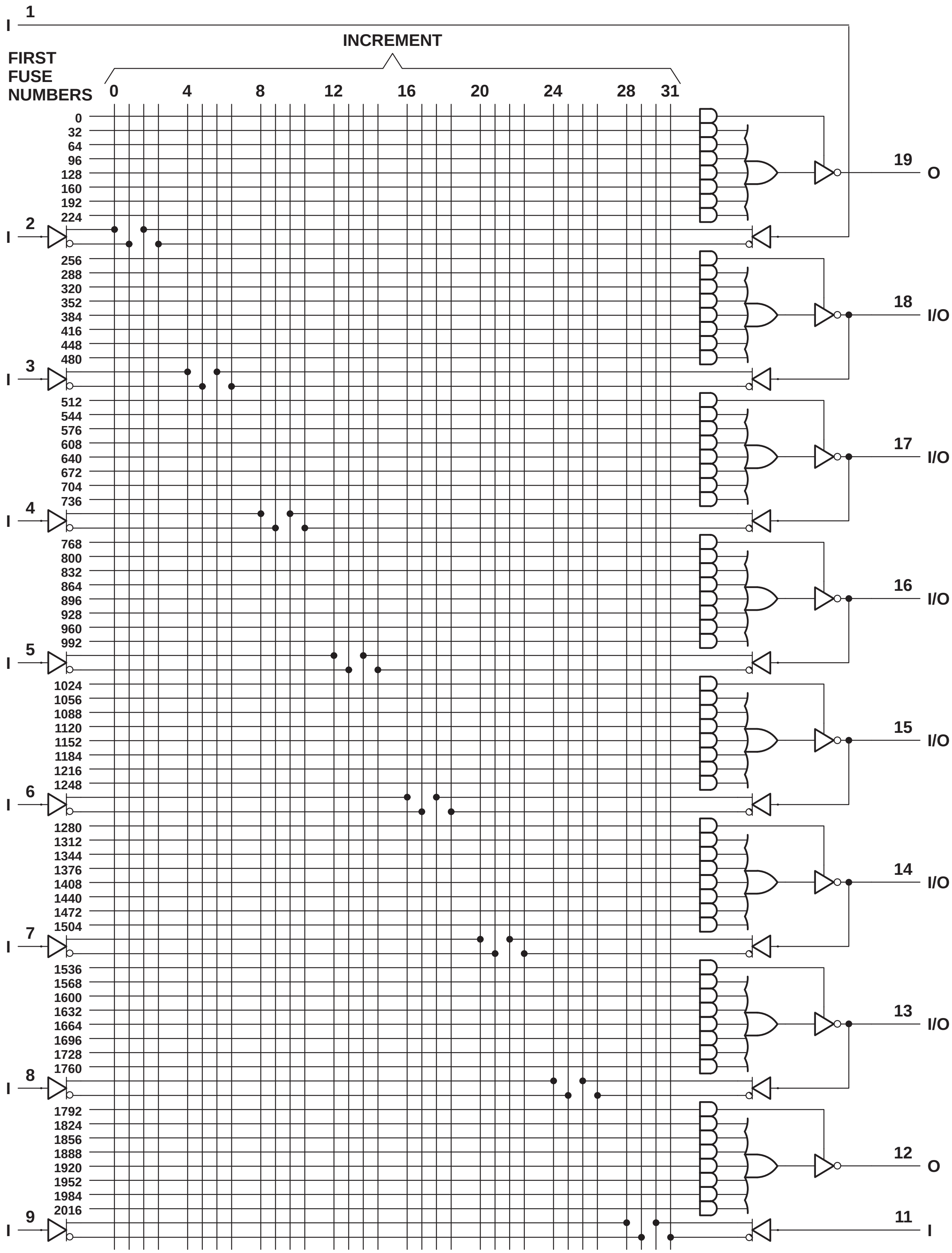


TIBPAL16R8’



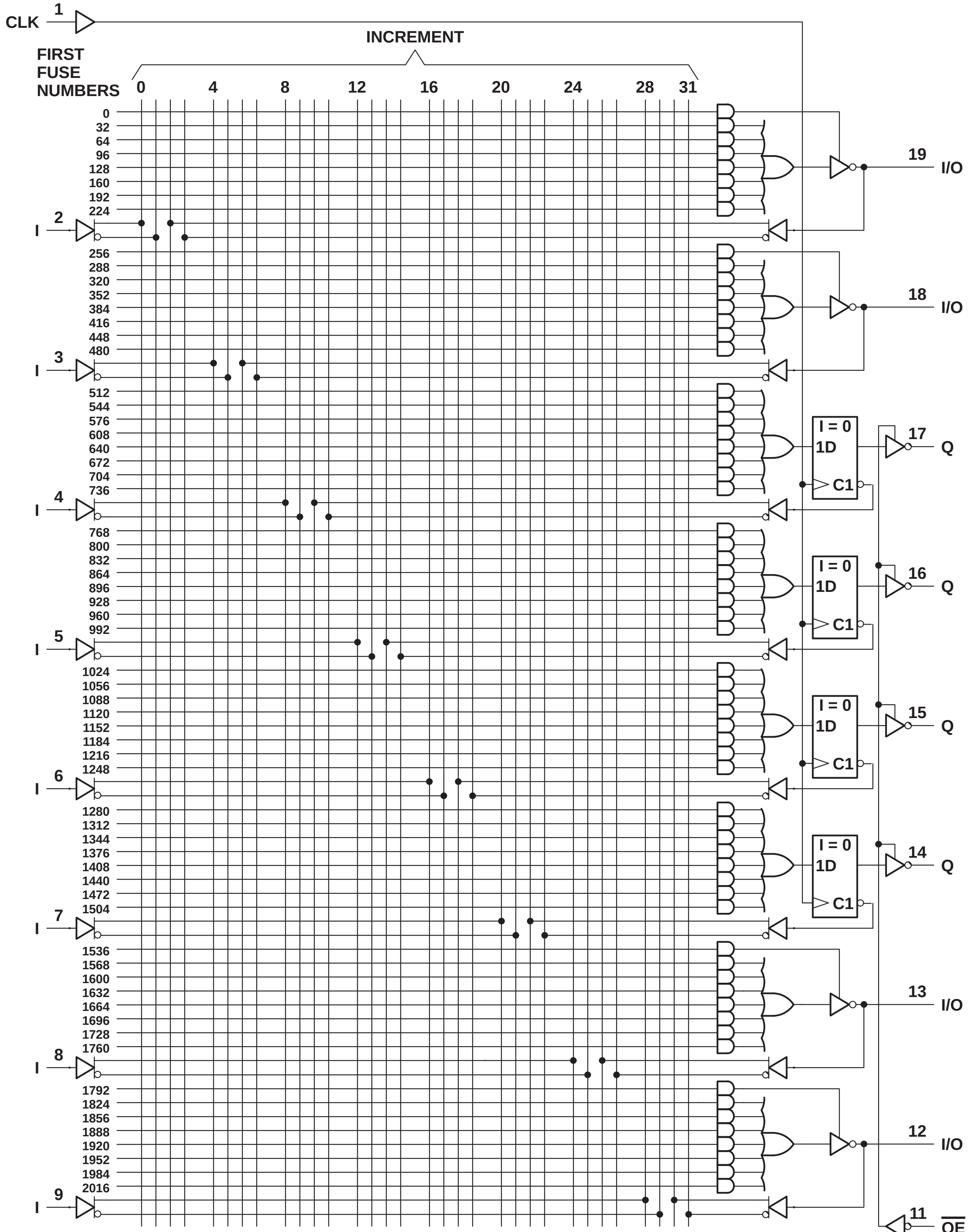
∿ denotes fused inputs

logic diagram (positive logic)



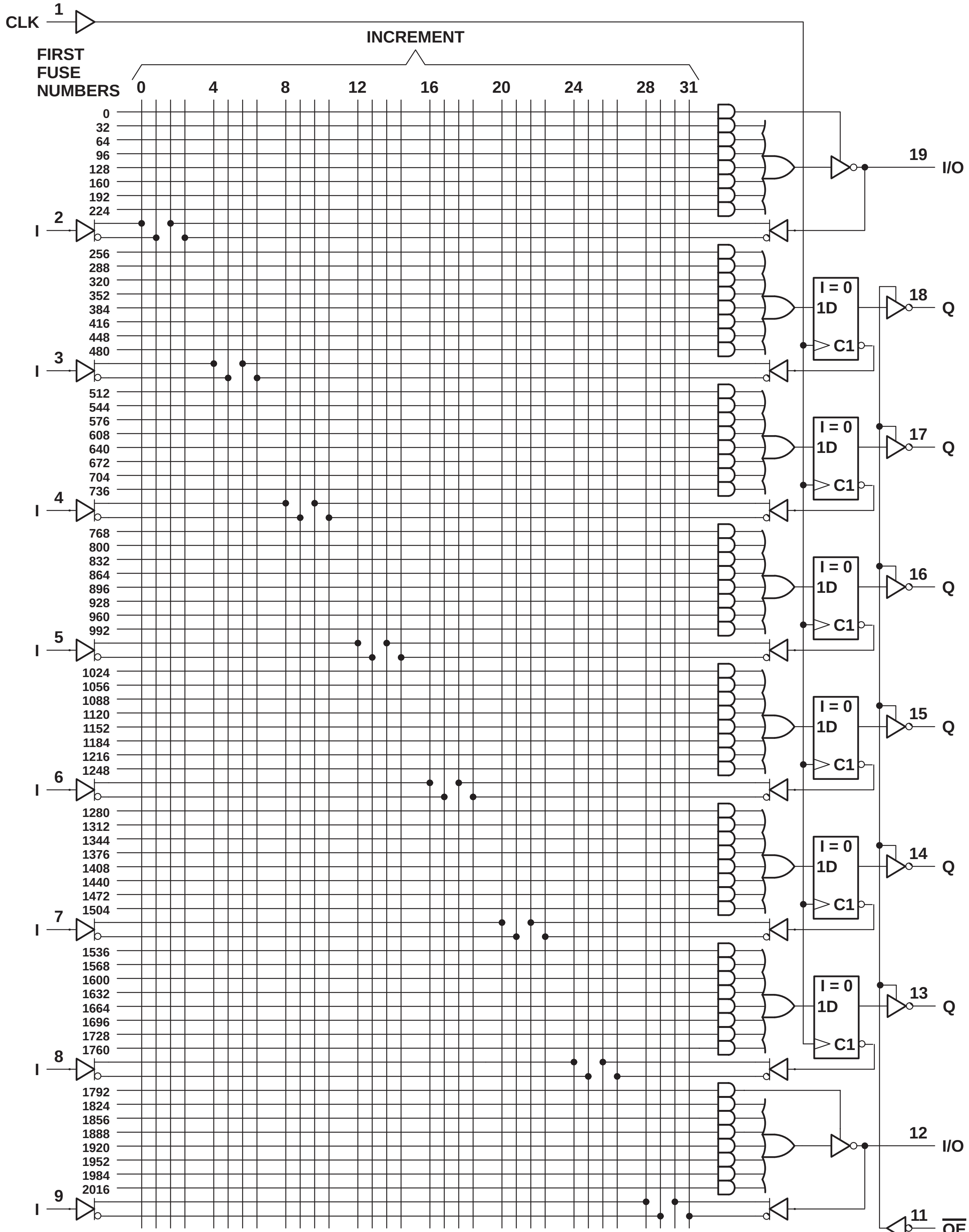
Fuse number = First fuse number + Increment

logic diagram (positive logic)



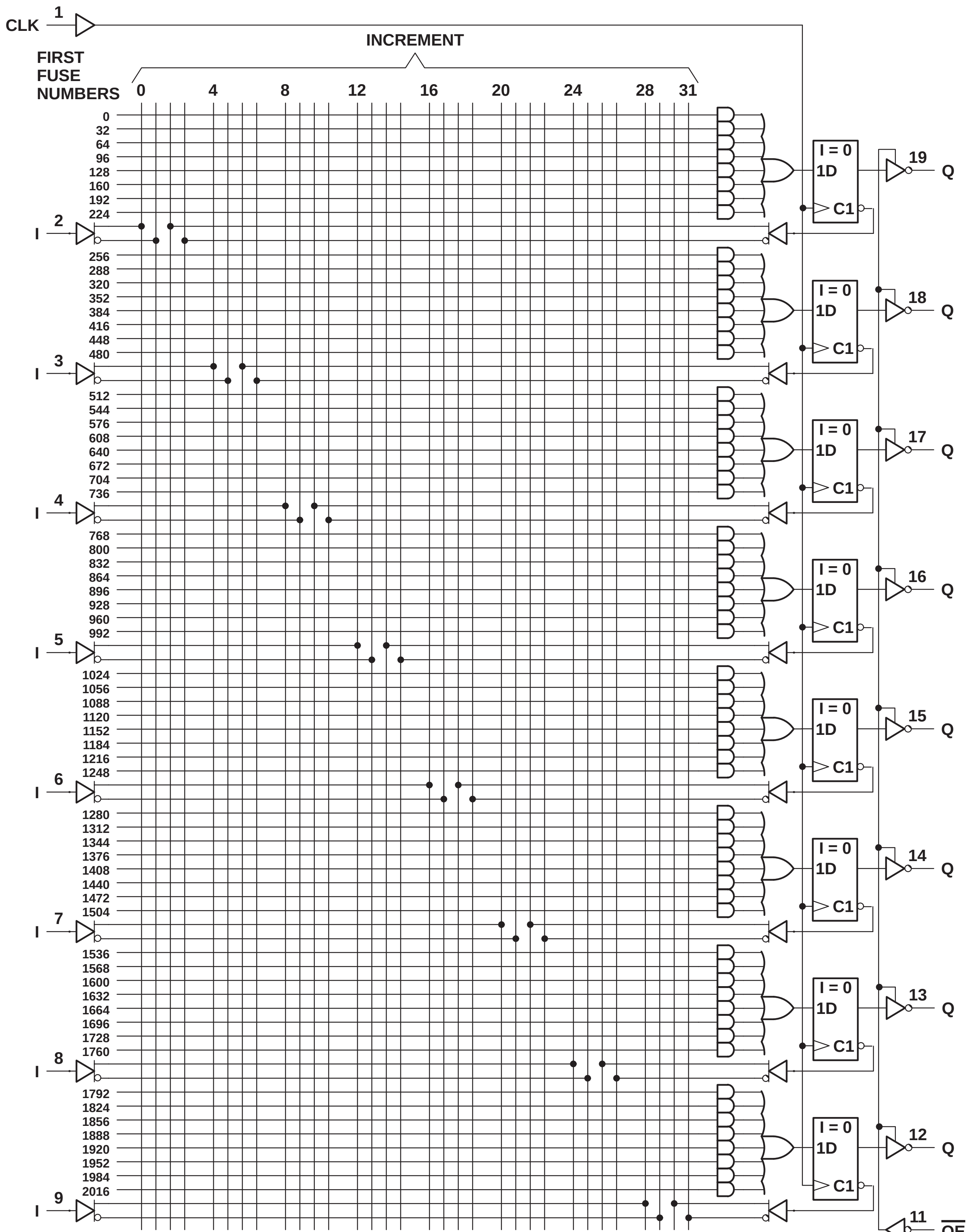
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V				–250	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open			180	mA
C_i	f = 1 MHz,	V_I = 2 V			8.5		pF
C_o	f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL16L8-5CFN		TIBPAL16L8-5CJ TIBPAL16L8-5CN		UNIT
					MIN	MAX	MIN	MAX	
t_{pd}	I, I/O	O, I/O	with up to 4 outputs switching	R1 = 200 Ω, R2 = 200 Ω, See Figure 8	1.5	5	1.5	5	ns
t_{pd}	I, I/O	O, I/O	with more than 4 outputs switching		1.5	5	1.5	5.5	ns
t_{en}	I, I/O	O, I/O			2	7	2	7	ns
t_{dis}	I, I/O	O, I/O			2	7	2	7	ns

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V				–250	µA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0,	Outputs open			200	mA
C_i	I	f = 1 MHz,	V_I = 2 V			7		pF
	CLK/$\overline{OE}$					5		
C_o	I/O	f = 1 MHz,	V_O = 2 V			10		pF
	Q					7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL16R4-5CFN TIBPAL16R6-5CFN			TIBPAL16R4-5CJ TIBPAL16R6-5CJ TIBPAL16R4-5CN TIBPAL16R6-5CN			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)			125			125			
	with external feedback			117			111			
t_{pd}	CLK↑	Q		1.5		4	1.5		4.5	ns
t_{pd}	CLK↑	Internal feedback				3.5			3.5	ns
t_{pd}	I, I/O	I/O		1.5		5	1.5		5	ns
t_{en}	$\overline{OE}$↓	Q		1.5		6	1.5		6	ns
t_{dis}	$\overline{OE}$↑	Q		1		6.5	1		7	ns
t_{en}	I, I/O	I/O		2		7	2		7	ns
t_{dis}	I, I/O	I/O		2		7	2		7	ns
t_r					1.5			1.5		ns
t_f					1.5			1.5		ns
$t_{sk(o)}$#	Skew between registered outputs				0.5			0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
¶ See 'f_{max} Specification' near the end of this data sheet.
# $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			TIBPAL16R8-5CFN			TIBPAL16R8-5CJ TIBPAL16R8-5CN			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5		0.3	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V				100			100	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.4 V				–100			–100	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				100			100	µA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				25			25	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V				–250			–250	µA
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0,	Outputs open			180			180	mA
C_i	I	f = 1 MHz,	V_I = 2 V			8.5			6.5		pF
	CLK/$\overline{OE}$					7.5			5.5		
C_o		f = 1 MHz,	V_O = 2 V			10			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL16R8-5CFN			TIBPAL16R8-5CJ TIBPAL16R8-5CN			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}§	without feedback			R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)				125			125			
	with external feedback				117			111			
t_{pd}	CLK↑	Q	with up to 4 outputs switching		1.5		4	1.5		4	ns
	CLK↑	Q	with more than 4 outputs switching		1.5		4	1.5		4.5	
t_{pd}¶	CLK↑	Internal feedback					3.5			3.5	ns
t_{en}	$\overline{OE}$↓	Q			1.5		6	1.5		6	ns
t_{dis}	$\overline{OE}$↑	Q			1		6.5	1		7	ns
t_r						1.5			1.5		ns
t_f						1.5			1.5		ns
$t_{sk(o)}$#	Skew between outputs					0.5			0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
§ See 'f_{max} Specification' near the end of this data sheet.
¶ This parameter is calculated from the measured f_{max} with internal feedback in a counter configuration (see Figure 2 for illustration).
# $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range . . . . –55°C to 125°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		100	MHz
t_w†	Pulse duration, clock	High	5			ns
		Low	5			
t_{su}†	Setup time, input or feedback before clock↑		7			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply to TIBPAL16L8'

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	2.7		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	μA
	I/O ports						–250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V				–250	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	$\overline{OE}$ = V_{IH}, Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V			8.5		pF
	CLK/$\overline{OE}$					7.5		
C_o		f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 8	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t_{pd}	I, I/O	O, I/O		1	7	ns
t_{pd}	CLK	Q		1	7	ns
t_{en}	OE↓	Q		1	8	ns
t_{dis}	OE↑	Q		1	10	ns
t_{en}	I, I/O	O, I/O		1	9	ns
t_{dis}	I, I/O	O, I/O		1	10	ns

§ See 'f_{max} Specification' near the end of this data sheet. f_{max} does not apply for TIBPAL16L8'. f_{max} with external feedback is not production tested and is calculated from the equation located in the f_{max} specifications section.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

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asynchronous preload procedure for registered outputs (see Figure 1 and Note 3)†

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Lower Pin 11 to 5 V.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

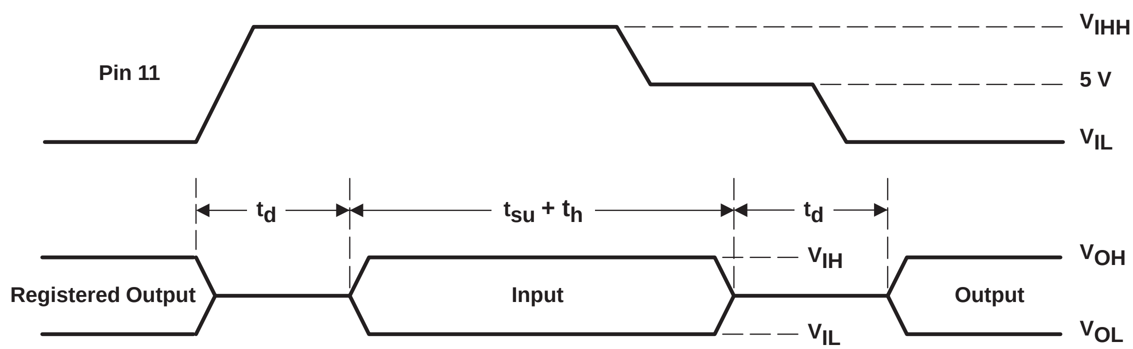
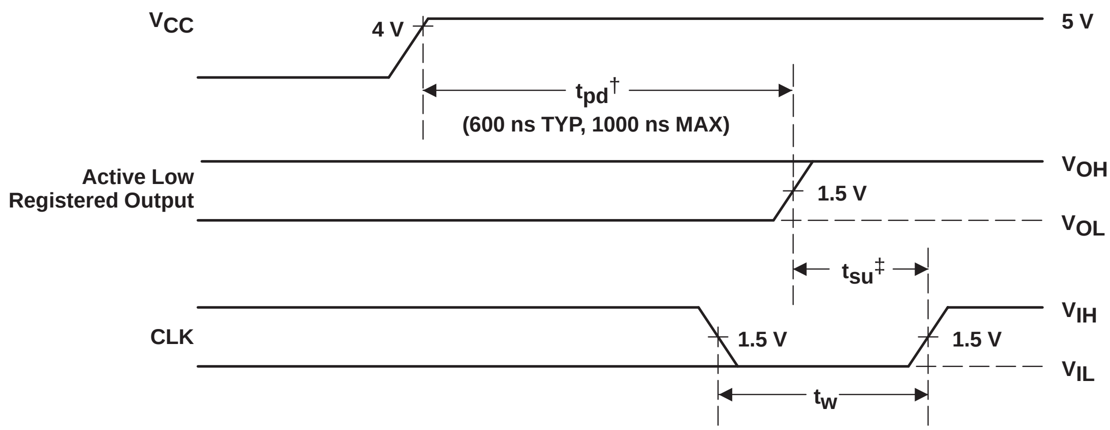


Figure 1. Asynchronous Preload Waveforms †

† Not applicable for TIBPAL16L8-5C and TIBPAL16L8-7M.
NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns
V_{IHH} = 10.25 V to 10.75 V

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback (see Figure 3)

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum fmax is determined by the minimum clock period (t_w high + t_w low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w\text{high} + t_w\text{low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

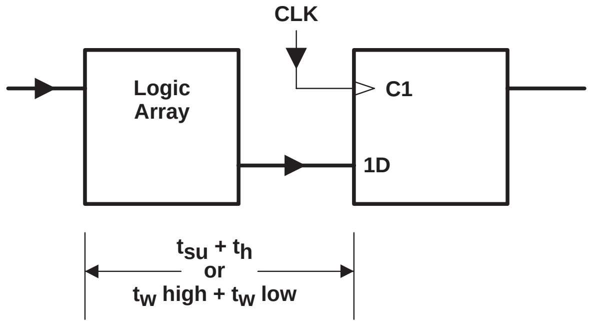


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback (see Figure 4)

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK} - \text{to} - \text{FB})}$.

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

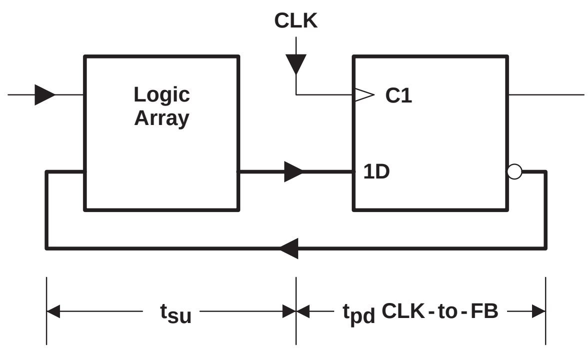


Figure 4. f_{max} With Internal Feedback

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f_{max} SPECIFICATIONS

f_{max} with external feedback (see Figure 5)

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK} - \text{to} - \text{Q})}$.

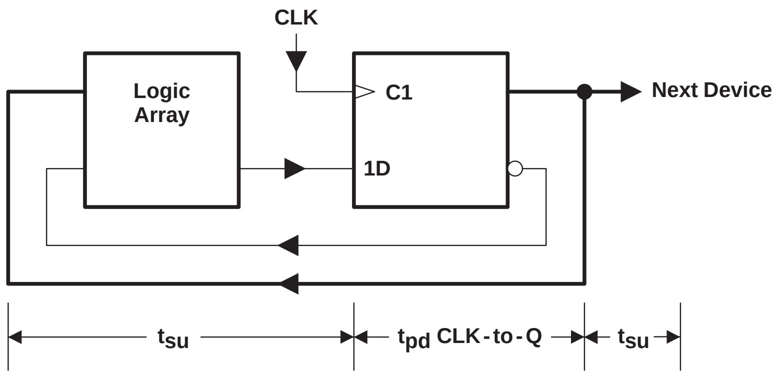


Figure 5. f_{max} With External Feedback

THERMAL INFORMATION

thermal management of the TIBPAL16R8-5C

Thermal management of the TIBPAL16R8-5CN and TIBPAL16R8-5CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 6 (a) and 6 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 7 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of eight fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.

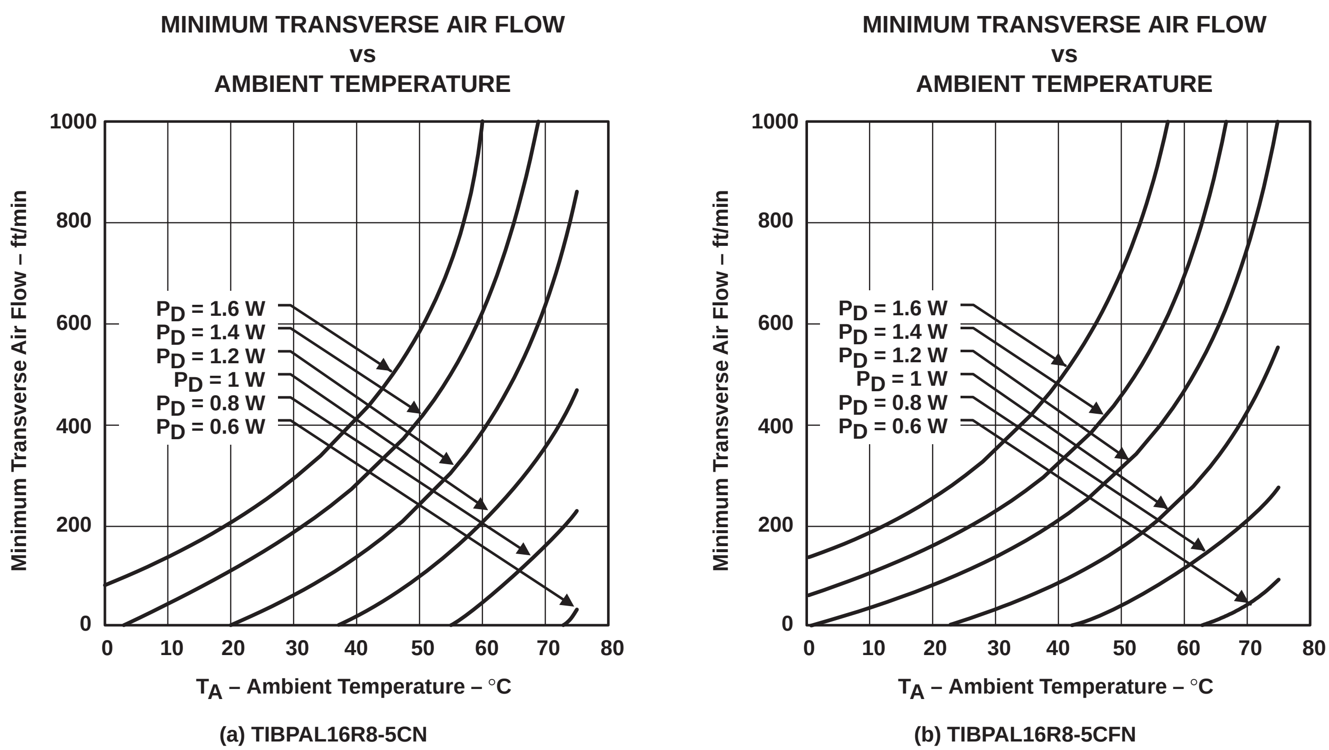


Figure 6

THERMAL INFORMATION

POWER DISSIPATION
vs
FREQUENCY

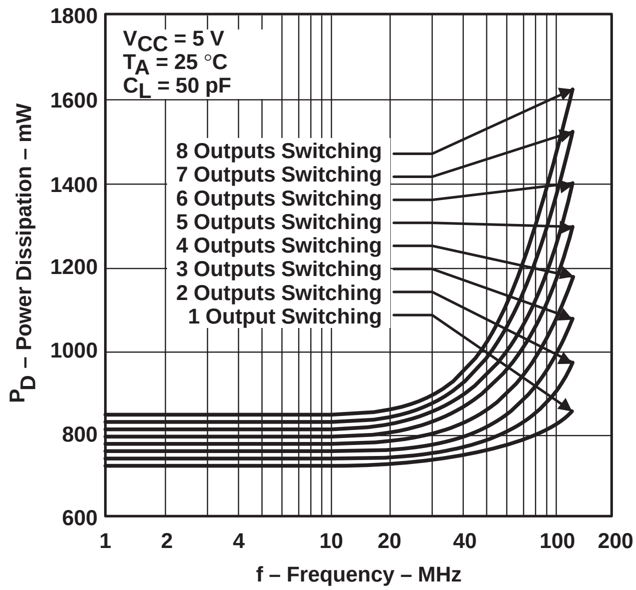
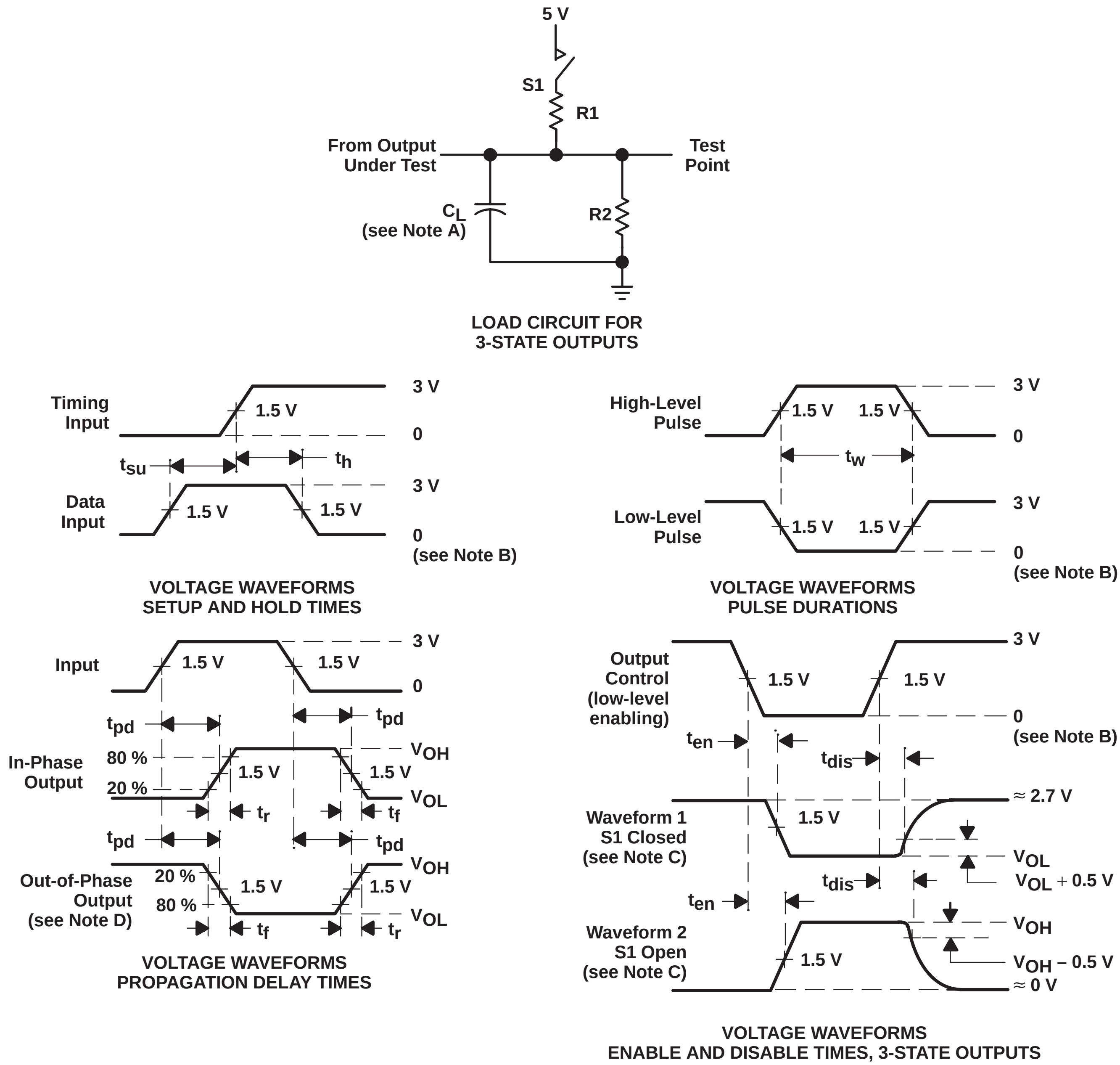


Figure 7

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: For C suffix, PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, PRR ≤ 10 MHz, $t_r = t_f \le 2$ ns, duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 8. Load Circuit and Voltage Waveforms

metastable characteristics of TIBPAL16R4-5C, TIBPAL16R6-5C, and TIBPAL16R8-5C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 9 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after system clock (SCLK). The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

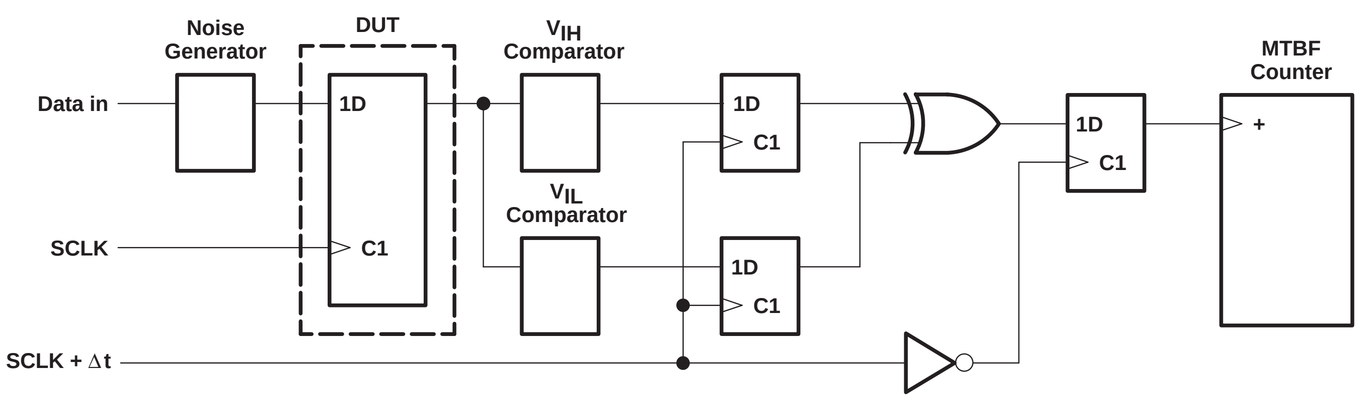
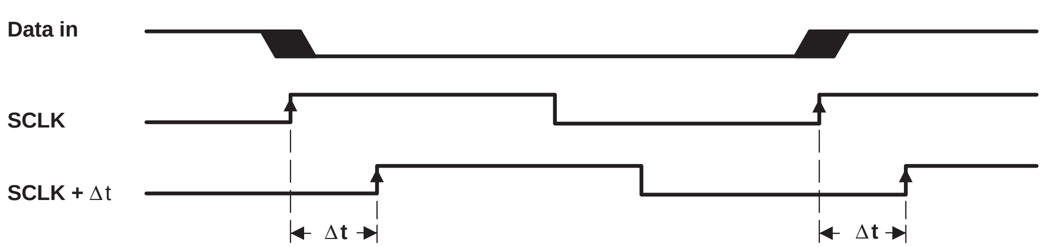


Figure 9. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 10. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$MTBF = \frac{Time\ (sec)}{\#\ Failures}$$

$$t_{rec} = \Delta t - CLK\ to\ Q\ (max)$$

Figure 10. Timing Diagram

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 9). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 11 shows the results for the TIBPAL16’-5C operating at 1 MHz.

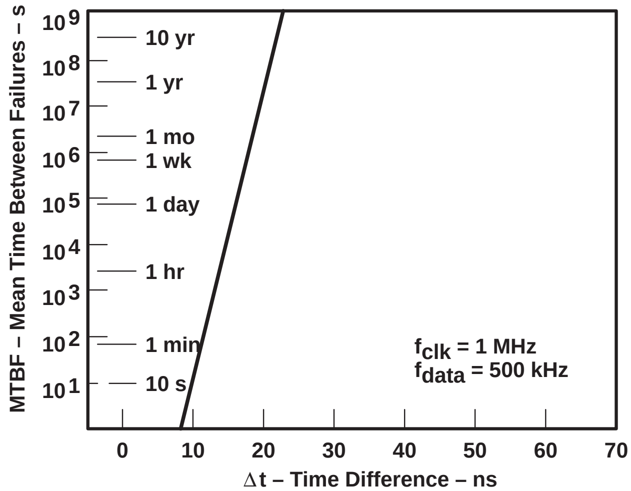


Figure 11. Metastable Characteristics

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times C1 \; e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: $C1 = 4.37 \times 10^{-3}$ and $C2 = 2.01$

Therefore

$$\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times 4.37 \times 10^{-3} \; e^{(-2.01 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 5-ns registered PLD programmed with the equation Q : = D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-5C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, ”Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits.’’

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

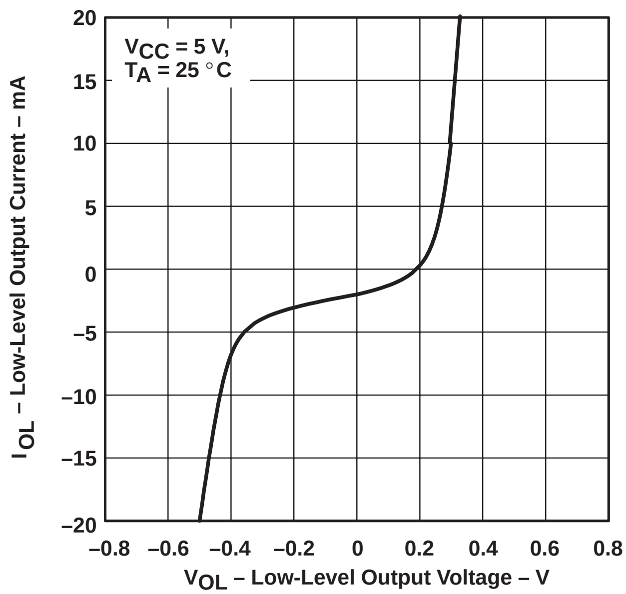


Figure 12

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

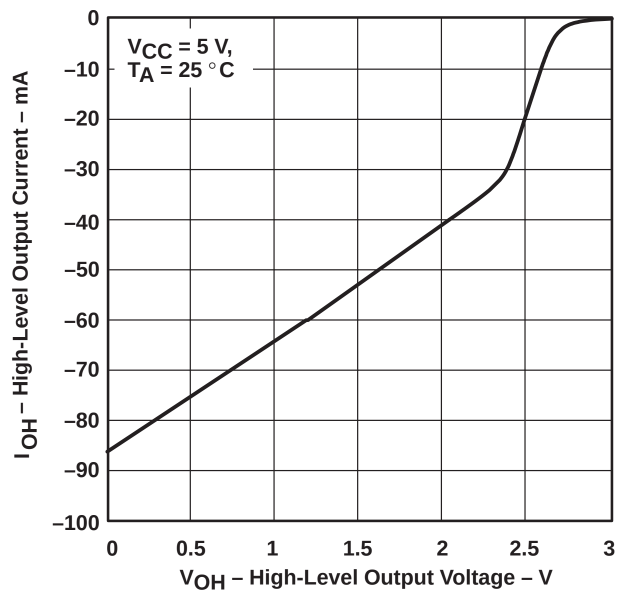


Figure 13

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

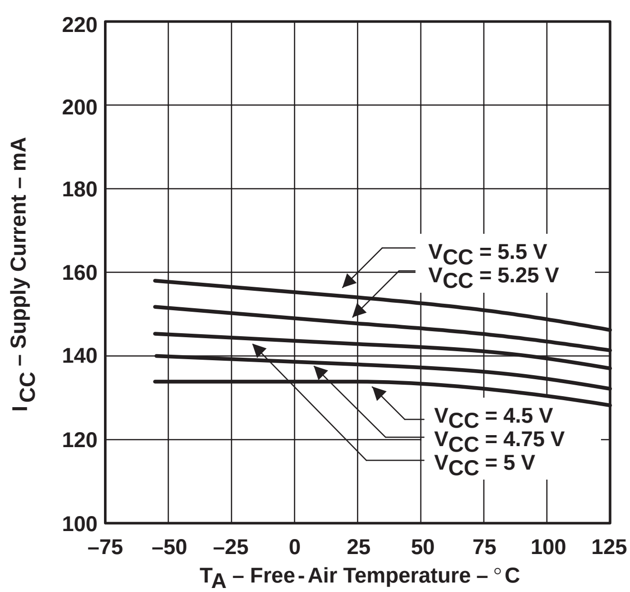


Figure 14

TYPICAL CHARACTERISTICS

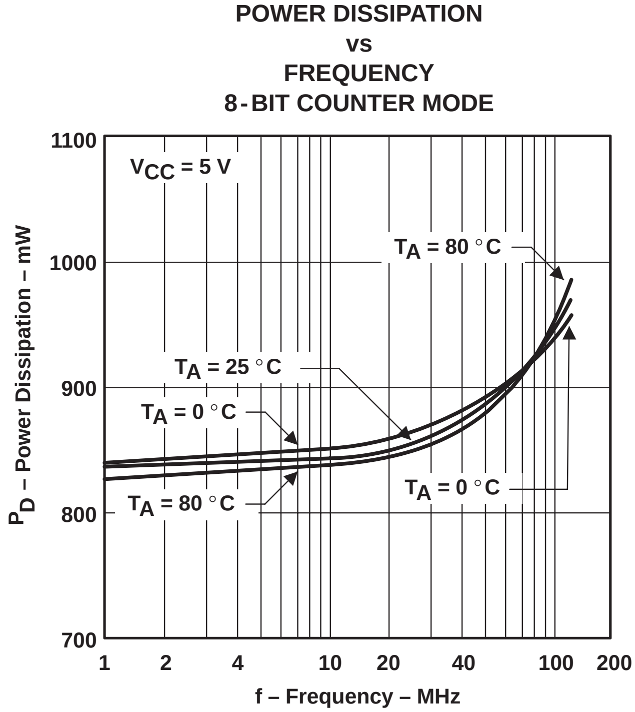


Figure 15

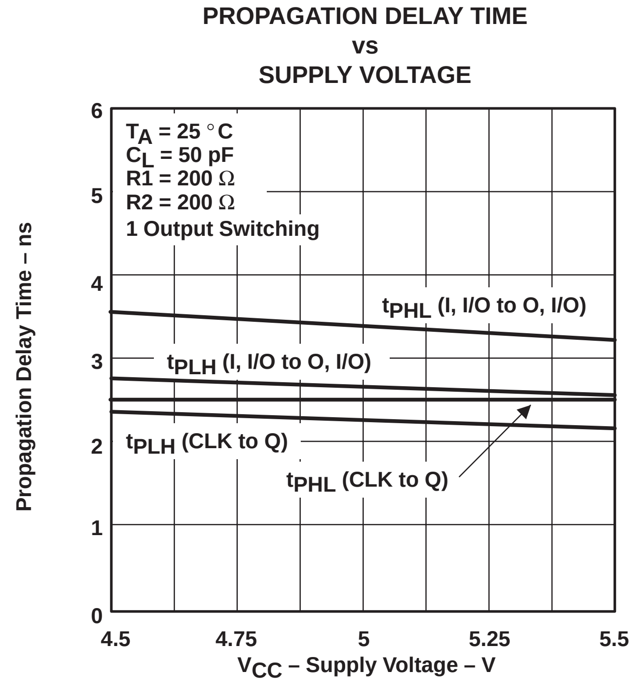


Figure 16

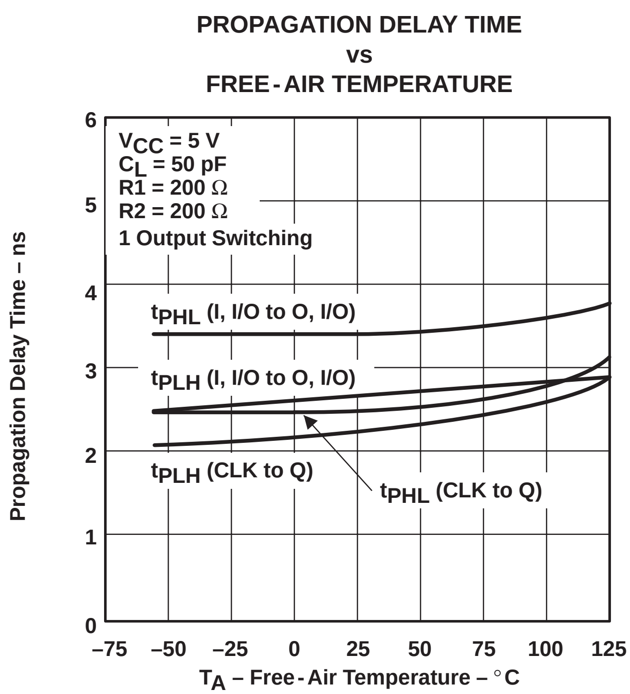


Figure 17

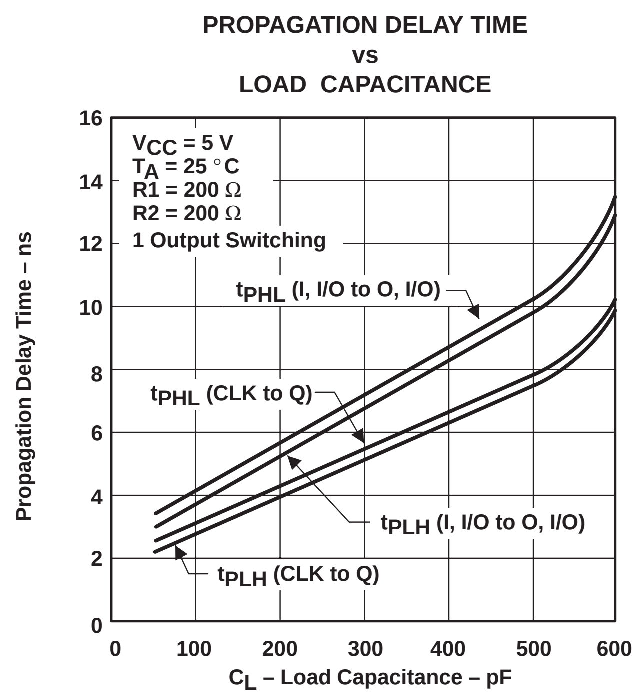


Figure 18

TYPICAL CHARACTERISTICS

SKEW BETWEEN OUTPUTS vs NUMBER OF OUTPUTS SWITCHING

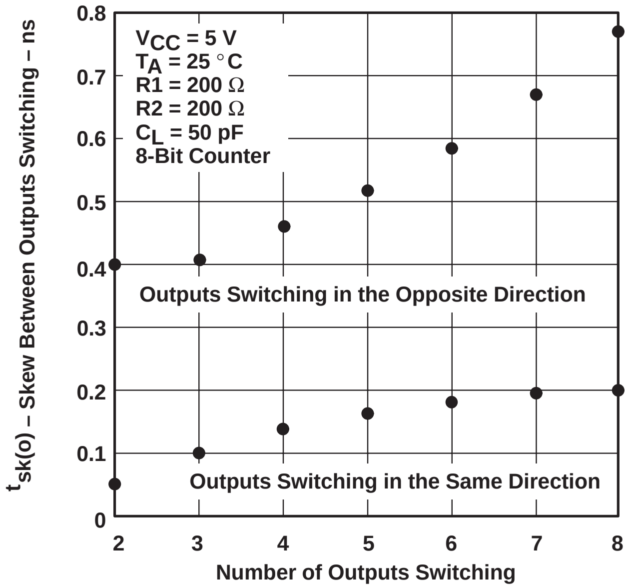


Figure 19

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

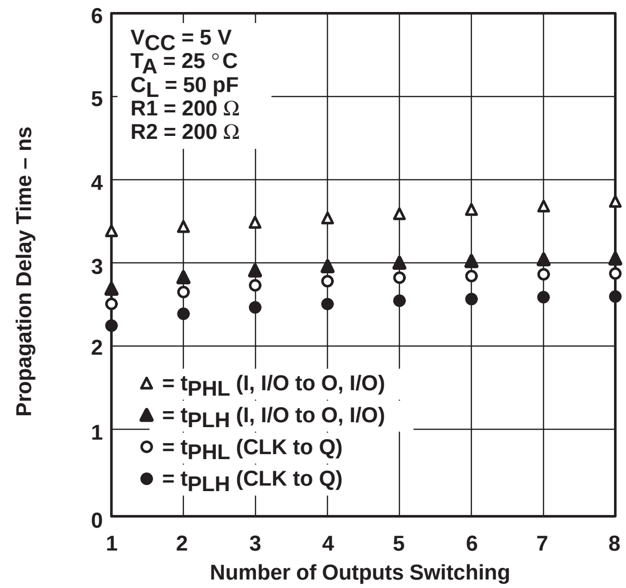


Figure 20

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