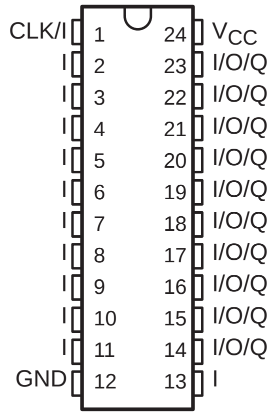
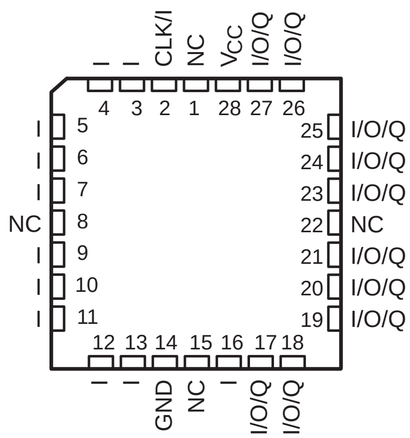
- **Functionally Equivalent to the TIBPAL22V10/10A, with Additional Feedback Paths in the Output Logic Macrocell**
- **Choice of Operating Speeds:**
  TIBPAL22VP10-20C . . . 20 ns Max
  TIBPAL22VP10-25M . . . 25 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic Dual-In-Line and Chip Carrier Packages**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22VP10’ is equivalent to the TIBPAL22V10A but offers additional flexibility in the output structure. The improved output macrocell uses the registered outputs as inputs when in a high-impedance condition. This provides two additional output configurations for a total of six possible macrocell configurations all of which are shown in Figure 1.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting. In addition, the data may be fed back into the array from either the register or the I/O port. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

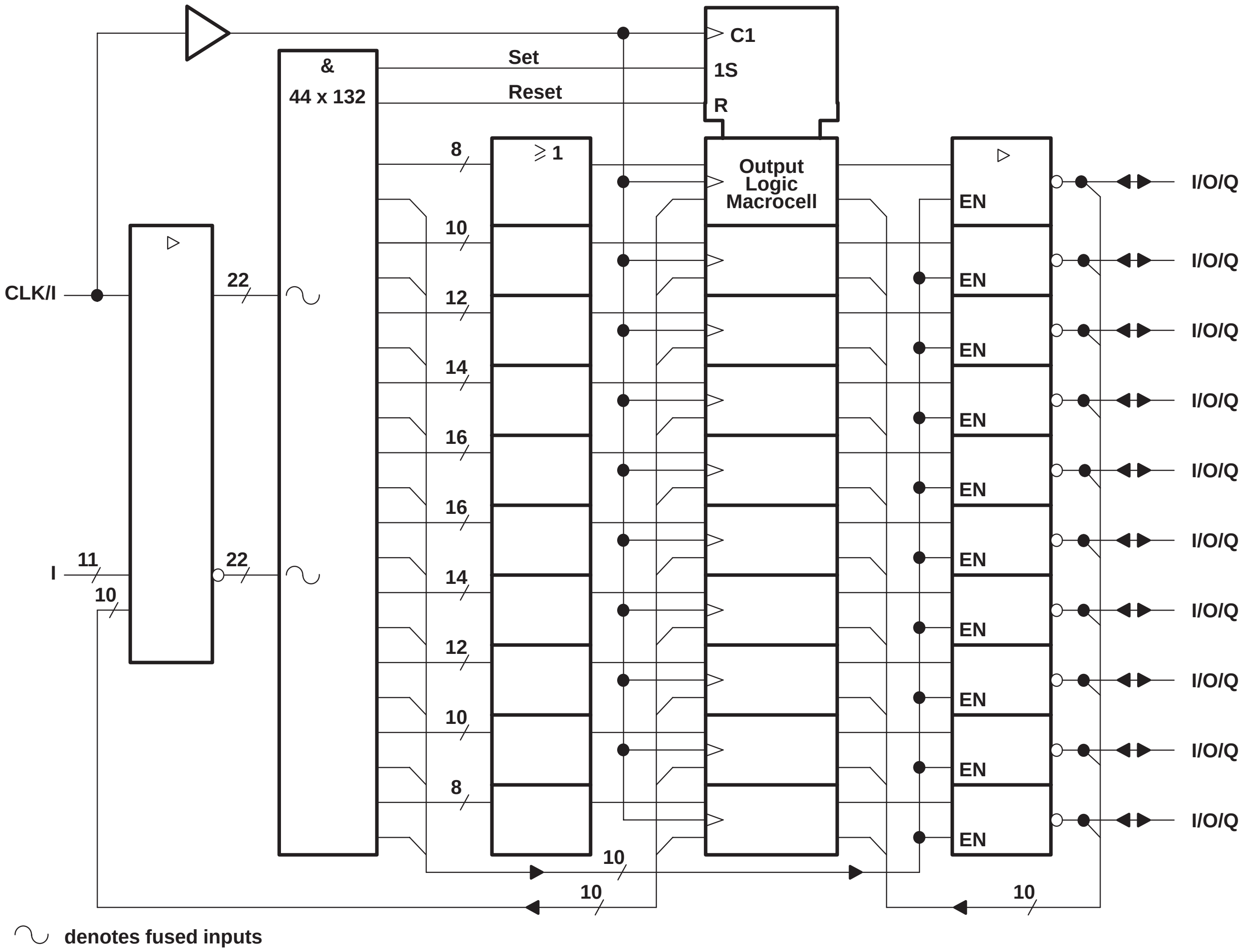
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22VP10' offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

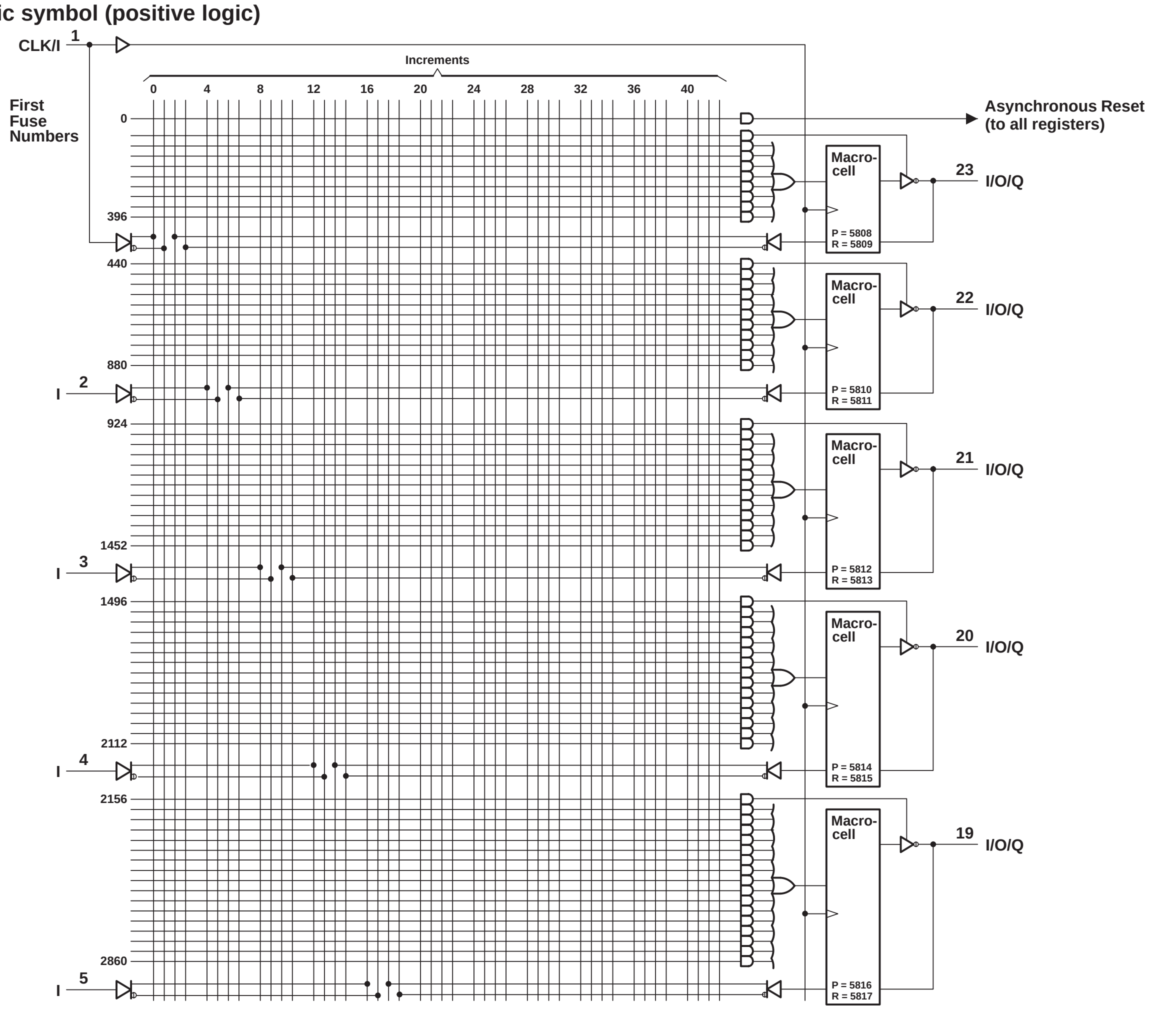
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

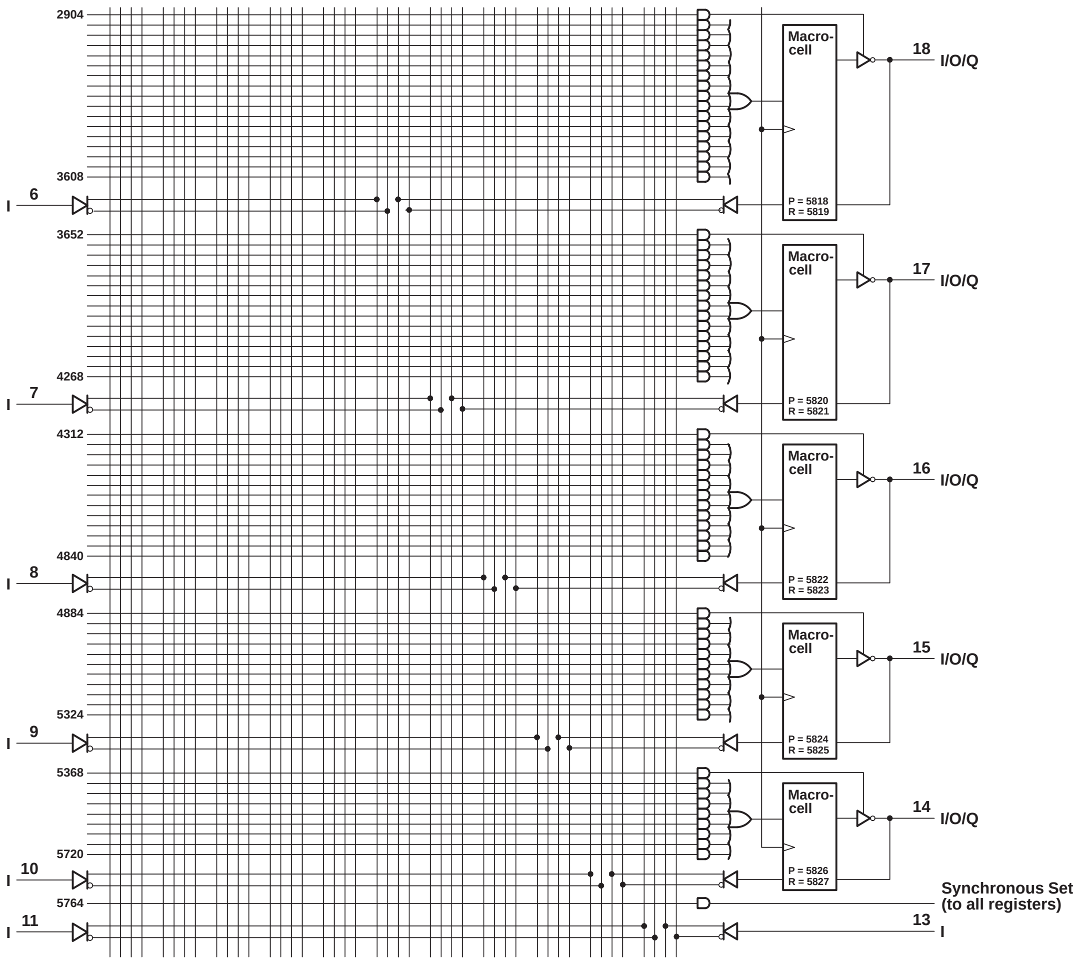
The TIBPAL22V10-20C is characterized for operation from 0°C to 75°C. The TIBPAL22V10-25M is characterized for operation over the full military temperature range of –55°C to 125°C.

functional block diagram (positive logic)



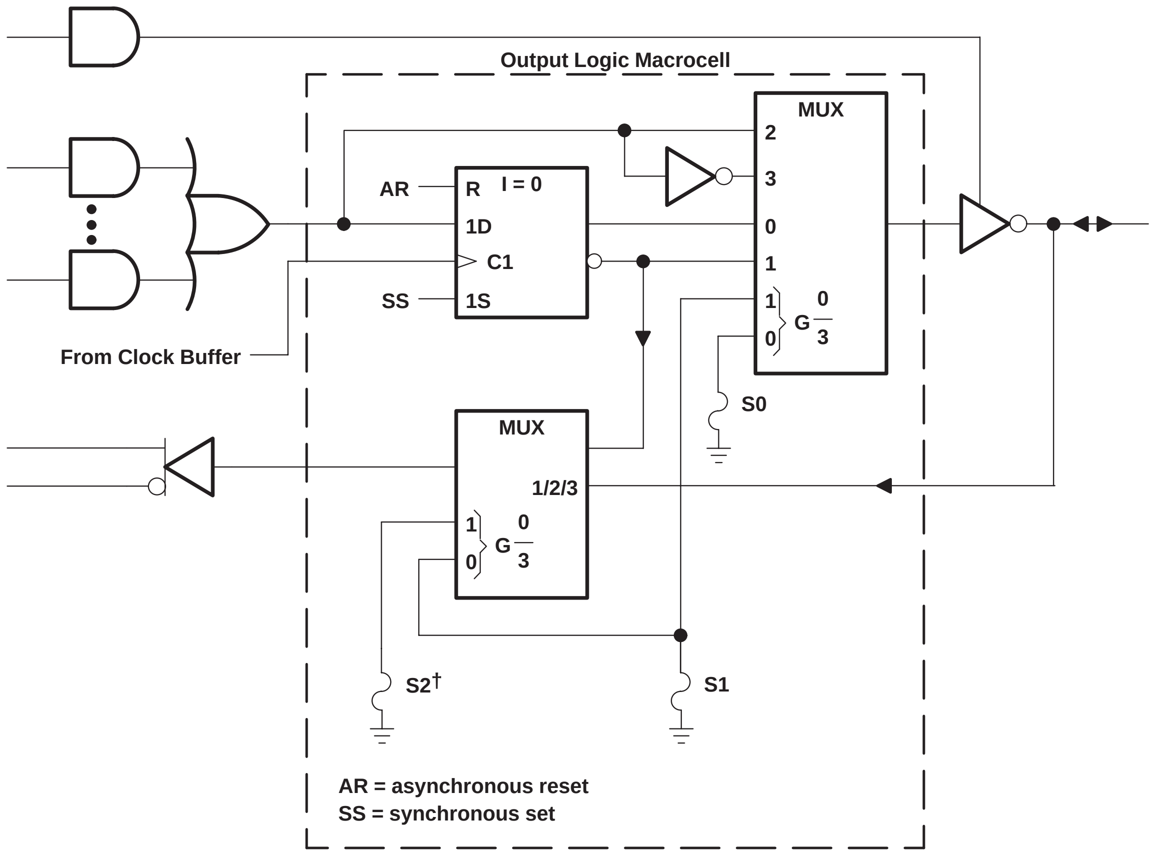
logic symbol (positive logic)



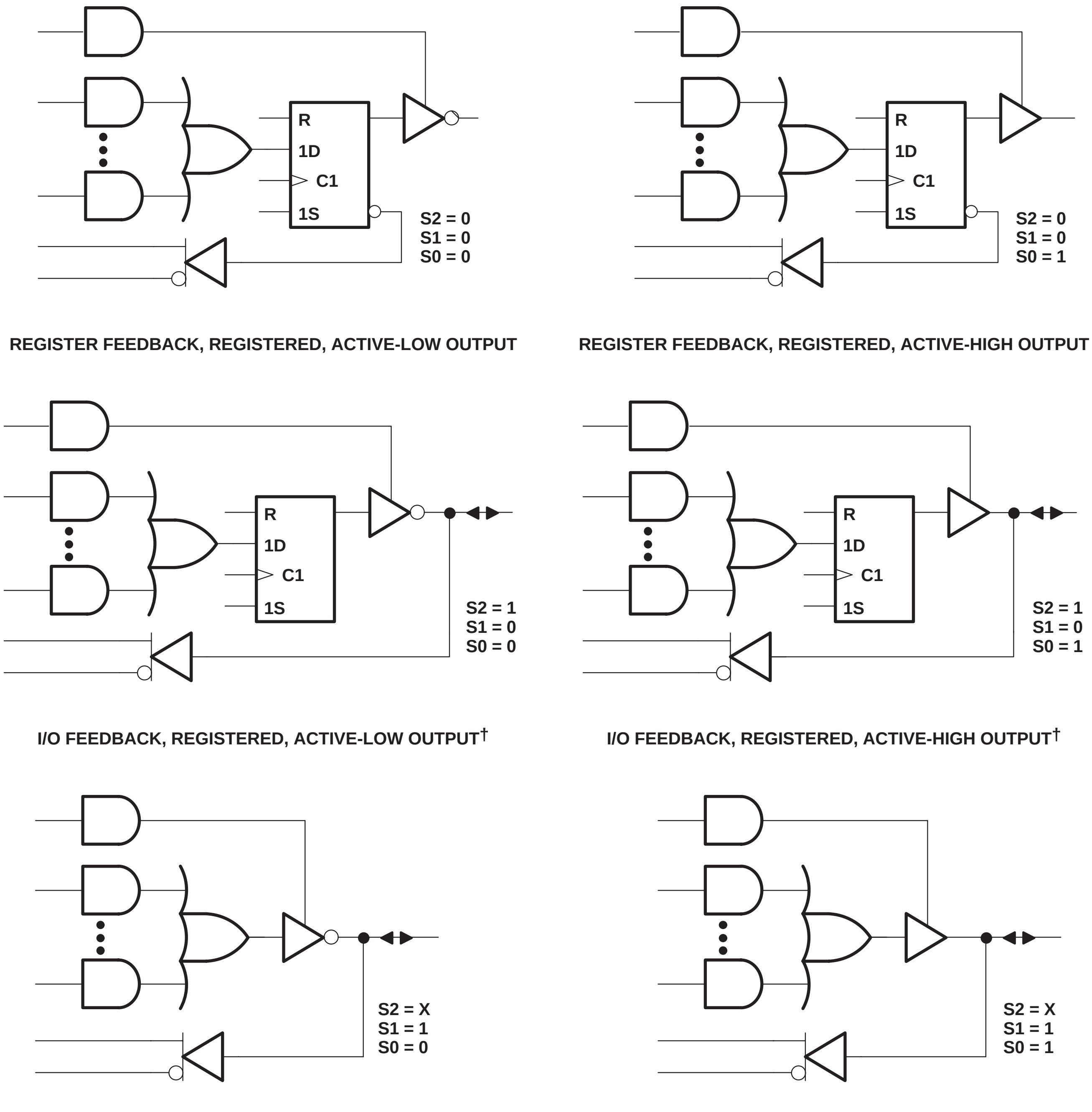


Fuse number = First fuse number + Increment
Inside each MACROCELL the ”P” fuse is the polarity fuse and the ”R” fuse is the register fuse.

output logic macrocell diagram



† This fuse is unique to the Texas Instruments TIBPAL22VP10'. It allows feedback from the I/O port using registered outputs as shown in the macrocell fusing logic function table.



REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT†

I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT†

I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT

I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

† These configurations are unique to the TIBPAL22VP10’ and provide added flexibility when comparing it to the TIBPAL22V10 or TIBPAL22V10A.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT			FEEDBACK AND OUTPUT CONFIGURATION		
S2	**S1**	**S0**			
0	0	0	Register feedback	Registered	Active low
0	0	1	Register feedback	Registered	Active high
1	0	0	I/O feedback	Registered	Active low
1	0	1	I/O feedback	Registered	Active high
X	1	0	I/O feedback	Combinational	Active low
X	1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse, X = unblown or blown fuse
S2, S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (see Note 1) . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . 5.5 V
Operating free-air temperature range: TIBPAL22VP10-20C . . . . 0°C to 75°C
TIBPAL22VP10-25M . . . . –55°C to 125°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			TIBPAL22VP10-20C			TIBPAL22VP10-25M			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–3.2			–2	mA
I_{OL}	Low-level output current				16			12	mA
f_{clock}	Clock frequency†				37			25	MHz
t_w	Pulse duration	Clock high or low	10			20			ns
		Asynchronous Reset high or low	20			30			
t_{su}	Setup time before clock↑	Input	15			20			ns
		Feedback	15			20			
		Synchronous Preset (active)	15			20			
		Asynchronous Reset (inactive)	20			25			
t_h	Hold time, input, preset, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0		75	–55		125	°C

† $f_{clock}\ (\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{clock} without feedback can be calculated as

$$f_{clock}\ (\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	Any output	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	μA
	Any I/O						–250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–90	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open		140	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§			C_L = 50 pF, R1 = 300 Ω, R2 = 390 Ω, See Figure 4	37	50		MHz
t_{pd}	I, I/O	I/O			12	20	ns
t_{pd}	I, I/O (reset)	Q			12	20	ns
t_{pd}	CLK	Q			8	12	ns
t_{en}	I, I/O	I/O, Q			12	20	ns
t_{dis}	I, I/O	I/O, Q			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
§ $f_{max}\ (\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} without feedback can be calculated as

$$f_{max}\ (\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.5		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V				–0.1	mA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				25	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–90	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	200	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§			C_L = 50 pF, R1 = 390 Ω, R2 = 750 Ω, See Figure 4	25	50		MHz
t_{pd}	I, I/O	I/O			12	25	ns
t_{pd}	I, I/O (reset)	Q			12	25	ns
t_{pd}	CLK	Q			8	15	ns
t_{en}	I, I/O	I/O, Q			12	25	ns
t_{dis}	I, I/O	I/O, Q			12	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
§ $f_{max}\ (\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} without feedback can be calculated as

$$f_{max}\ (\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

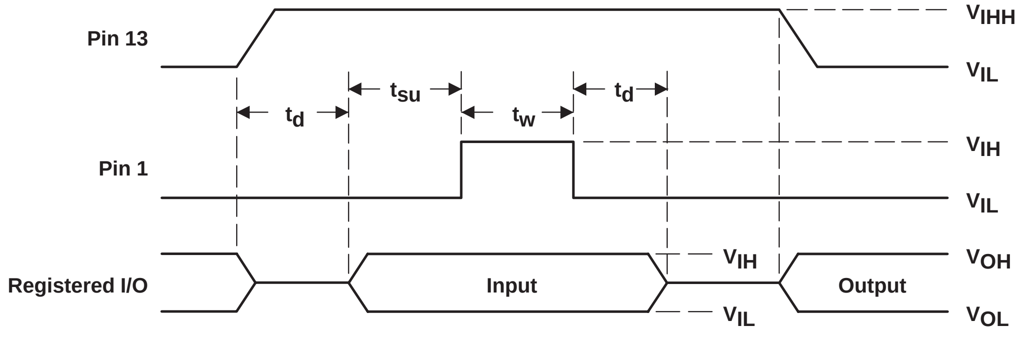
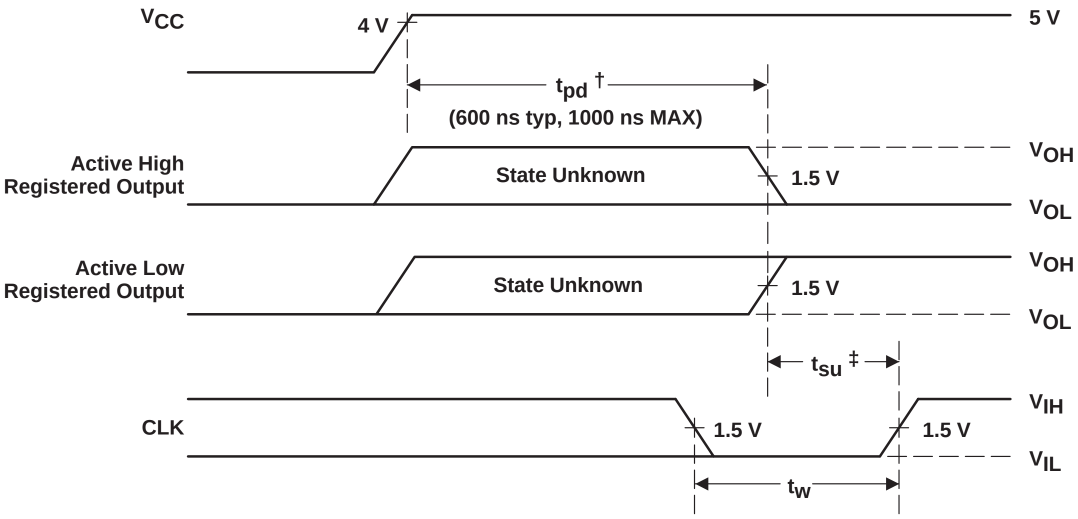


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

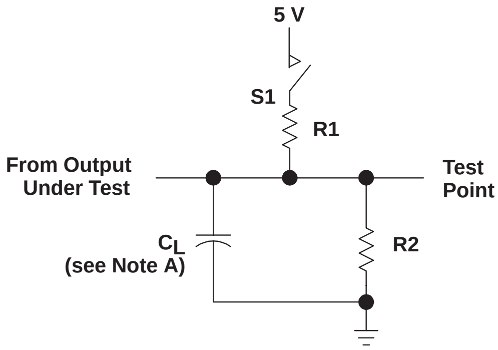
programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

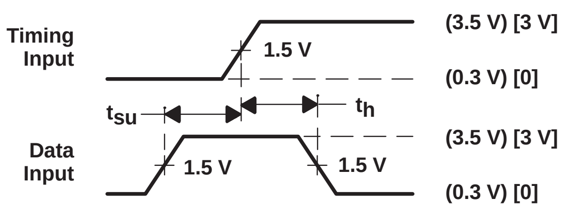
When the additional fuses are not being used, the TIBPAL22VP10 can be programmed using the TIBPAL22V10/10A programming algorithm. The fuse configuration data can either be from a JEDEC file (format per JEDEC Standard No. 3-A) or a TIBPAL22V10/10A master.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

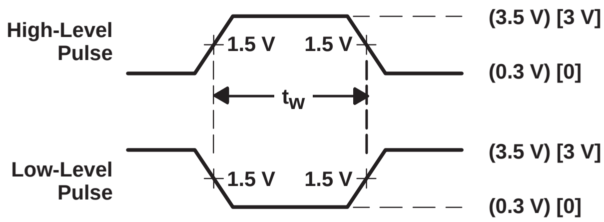
PARAMETER MEASUREMENT INFORMATION



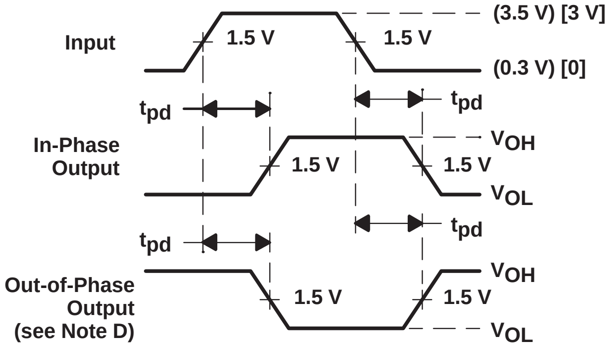
LOAD CIRCUIT FOR 3-STATE OUTPUTS



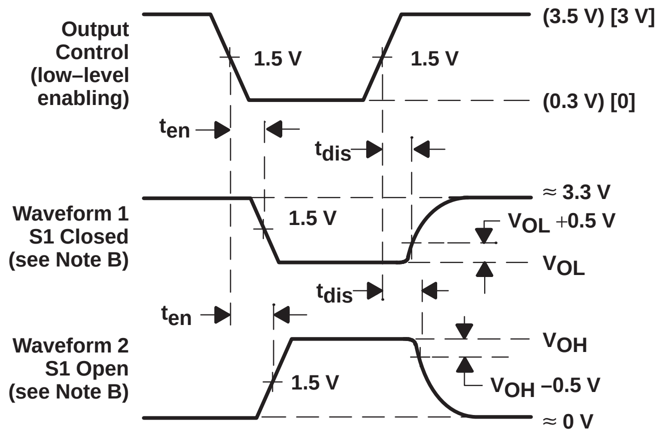
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

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AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd., 6-10 Talavera Road, North Ryde (Sydney), New South Wales, Australia 2113, 2-878-9000; 14th Floor, 380 Street, Kilda Road, Melbourne, Victoria, Australia 3004, 3-696-1211; 171 Philip Highway, Elizabeth, South Australia 5112, 8 255-2066.
BELGIUM: Texas Instruments Belgium S.A./N.V., Avenue Jules Bordetlaan 11, 1140 Brussels, Belgium, (02) 242 30 80.
BRAZIL: Texas Instruments Electronicos do Brasil Ltda., Av. Eng. Luiz Carlos Berrini 1461-11o andar, 04571, Sao Paulo, SP, Brazil, 11-535–5133.
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