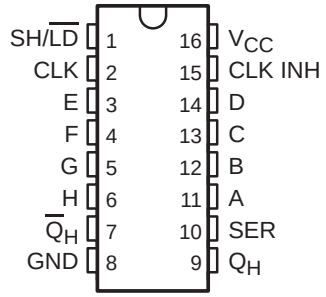
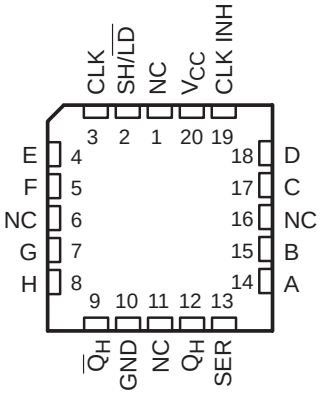
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS165 . . . J PACKAGE
SN74ALS165 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′ALS165 are parallel-load 8-bit serial shift registers that, when clocked, shift the data toward serial (Q_H and $\overline{Q}_H$) outputs. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ′ALS165 have a clock-inhibit function and complemented serial outputs.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and the clock inhibit (CLK INH) input is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

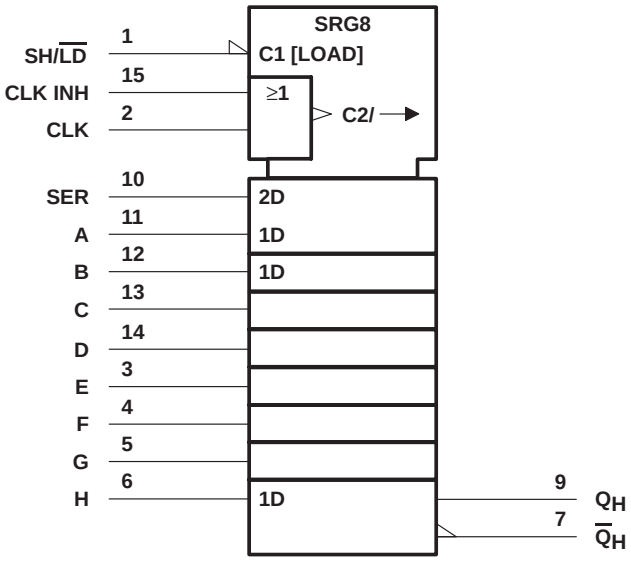
The SN54ALS165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS165 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

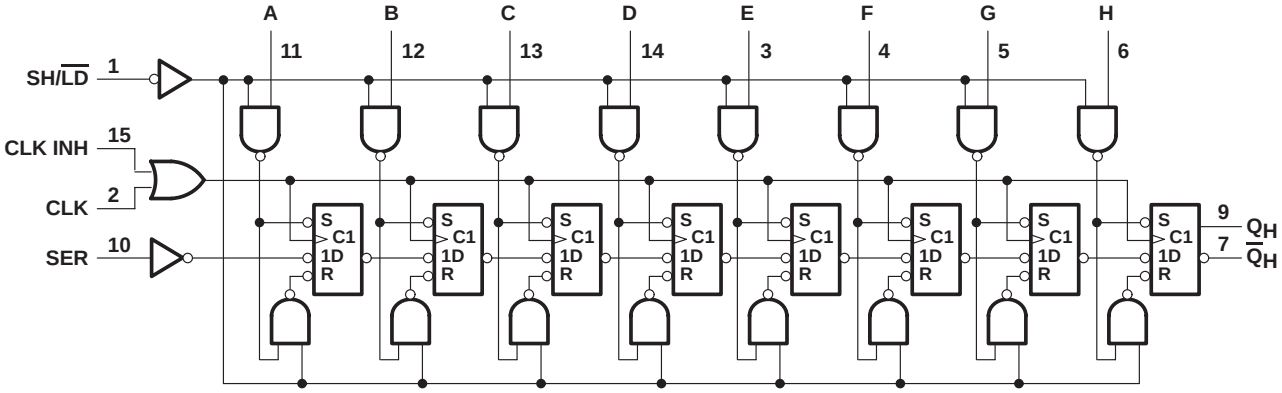
† Shift = content of each internal register shifts toward serial outputs. Data at SER is shifted into first register.

logic symbol†



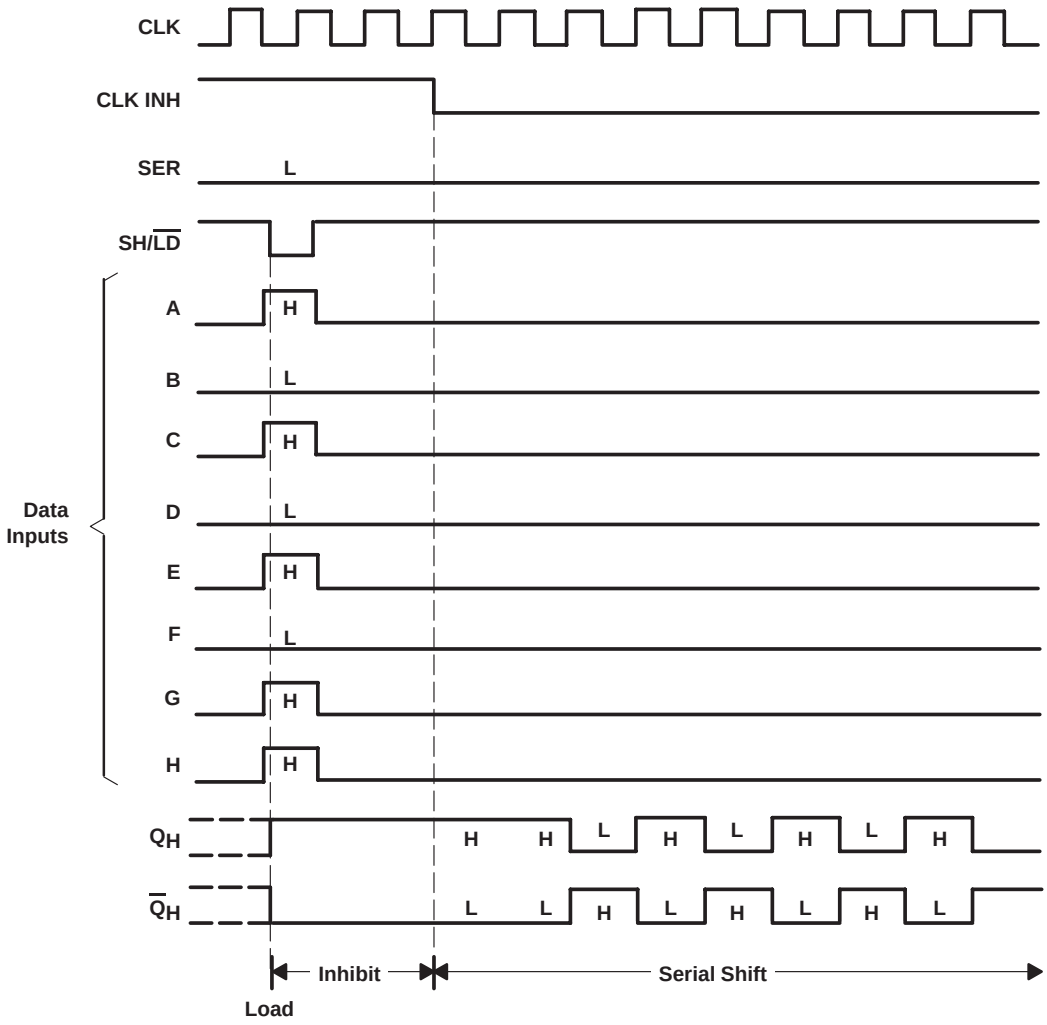
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS165 . . . . . –55°C to 125°C
SN74ALS165 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS165			SN74ALS165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		35	0		45	MHz
$t_{w(CLK)}$	Pulse duration, CLK (see Figure 1)	CLK high	14			11			ns
		CLK low	14			11			
$t_{w(load)}$	Pulse duration, SH/$\overline{LD}$ low	CLK low	15			12			ns
t_{su1}	Setup time, clock enable (see Figure 1)		15			11			ns
t_{su2}	Setup time, parallel input (see Figure 1)		11			10			ns
t_{su3}	Setup time, serial input (see Figure 2)		11			10			ns
t_{su4}	Setup time, shift (see Figure 2)		15			10			ns
t_h	Hold time at any input		4			4			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS165			SN74ALS165			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		12	24		12	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

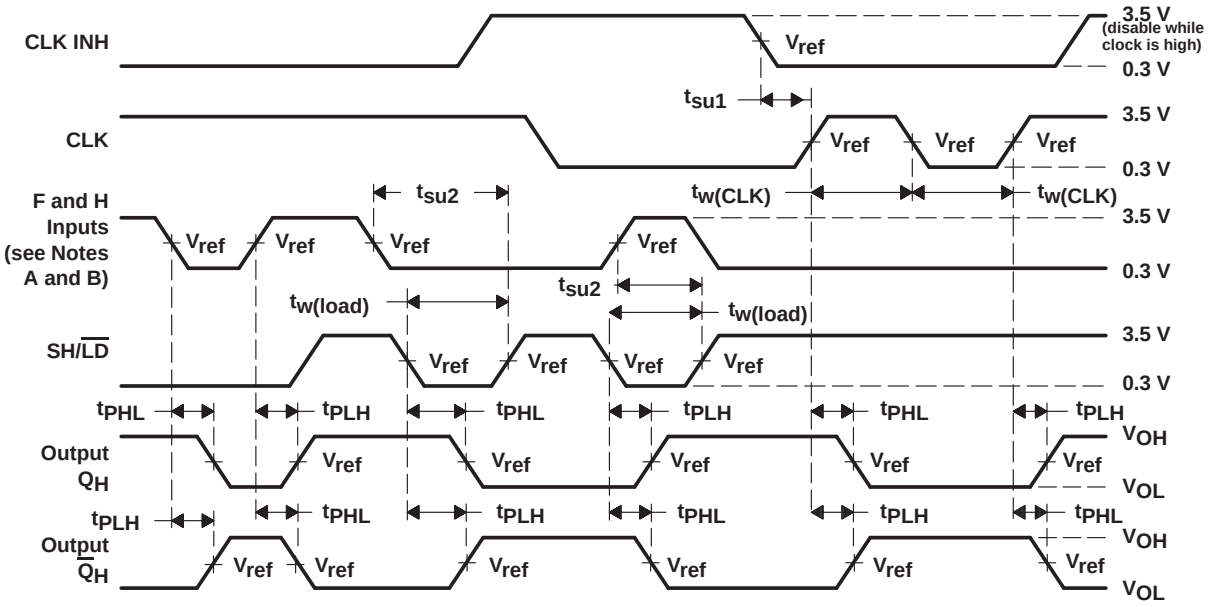
NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/$\overline{LD}$, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

switching characteristics (see Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS165		SN74ALS165		
			MIN	MAX	MIN	MAX	
f_{max}			35		45		MHz
t_{PLH}	SH/$\overline{LD}$	Any	4	23	4	20	ns
t_{PHL}			4	23	4	22	
t_{PLH}	CLK	Any	3	14	3	13	ns
t_{PHL}			3	15	3	14	
t_{PLH}	H	Q_H	3	14	3	13	ns
t_{PHL}			3	18	3	16	
t_{PLH}	H	Q_H	2	17	2	15	ns
t_{PHL}			3	17	3	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

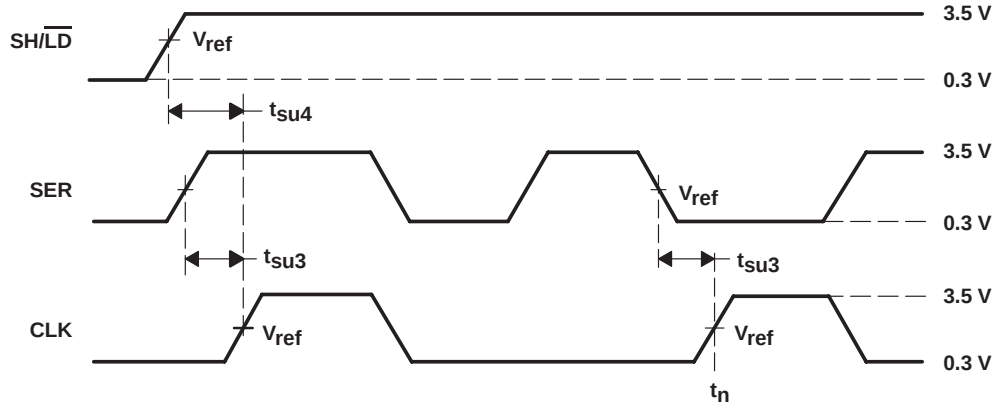
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The remaining six data inputs and SER are low.
B. Prior to test, high-level data is loaded into the H input.
C. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $t_r = t_f$ = 2 ns.
D. V_{ref} = 1.3 V

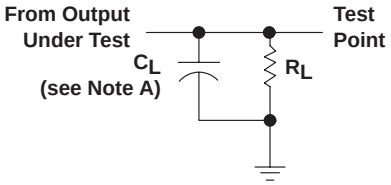
Figure 1. Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The eight data inputs and CLK INH are low. Results are monitored at Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f = 2$ ns.
C. $V_{ref} = 1.3$ V

Figure 2. Voltage Waveforms



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit for Switching Tests

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