

SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

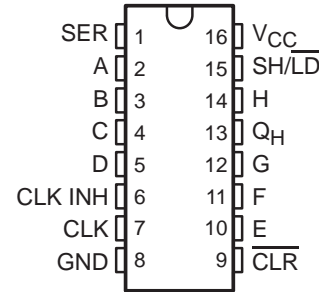
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

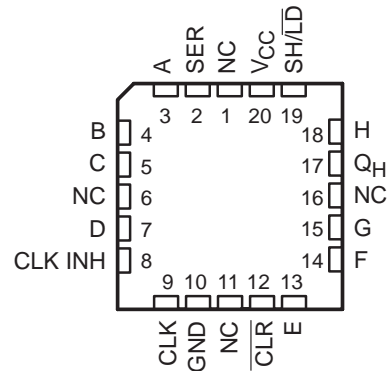
The 'HC166 parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear (CLR) input. The parallel-in or serial-in modes are established by the shift/load (SH/LD) input. When high, SH/LD enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. CLR overrides all other inputs, including CLK, and resets all flip-flops to zero.

The SN54HC166 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC166 is characterized for operation from -40°C to 85°C .

SN54HC166 . . . J OR W PACKAGE
SN74HC166 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC166 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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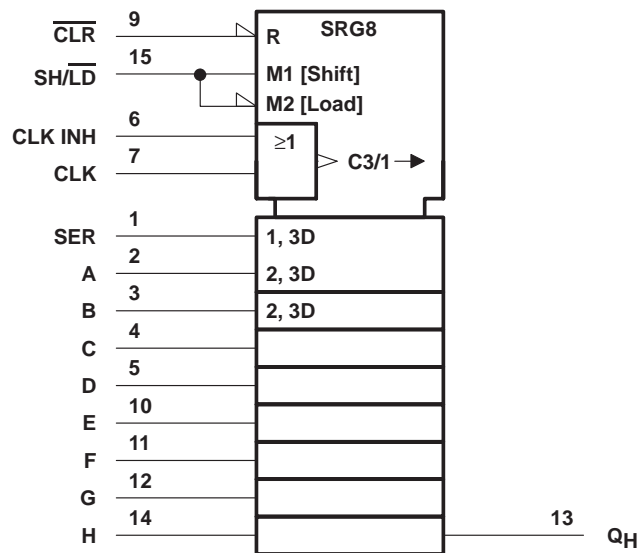
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SCLS117B – DECEMBER 1982 – REVISED MAY 1997

FUNCTION TABLE

INPUTS						OUTPUTS		
						INTERNAL		QH
CLR	SH/LD	CLK INH	CLK	SER	PARALLEL A...H	QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

logic symbol†

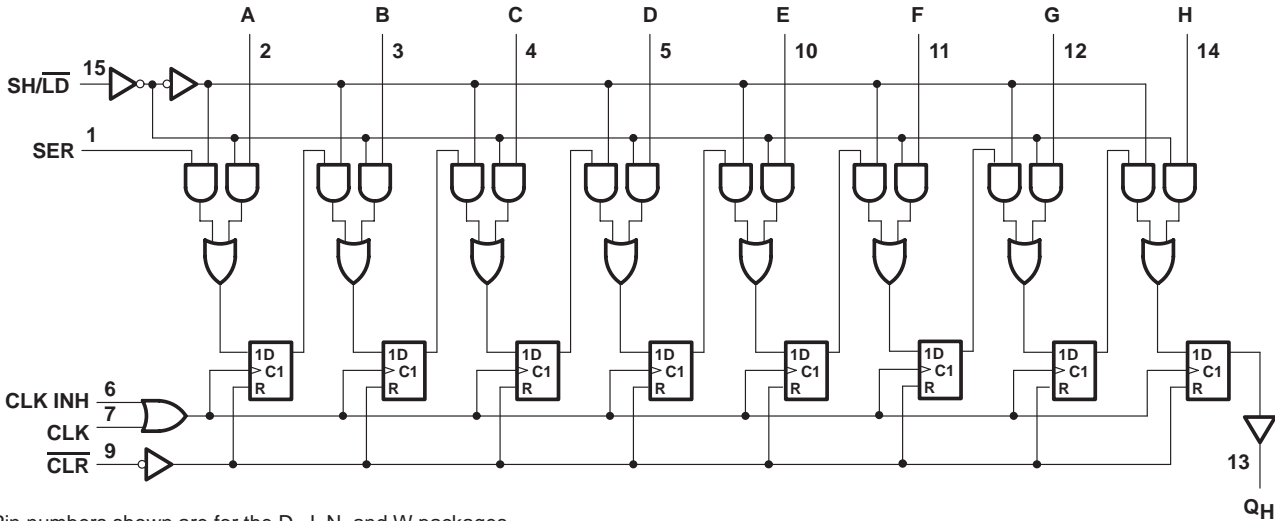


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

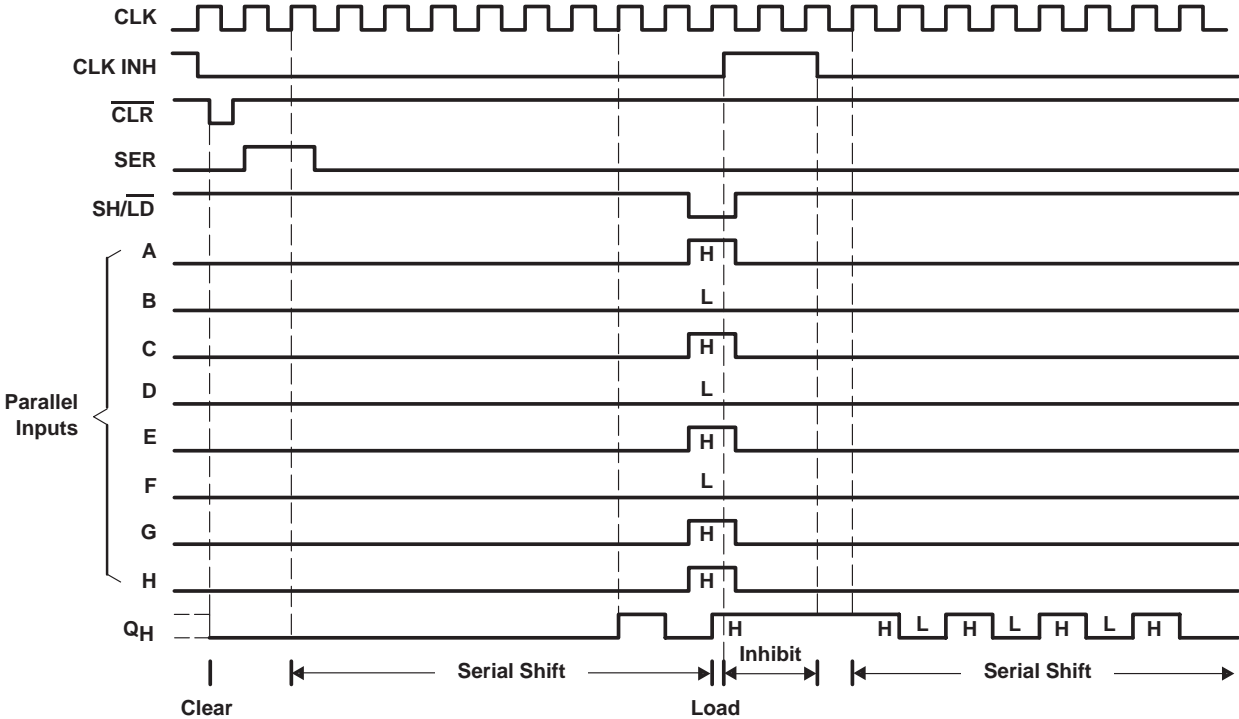
SCLS117B – DECEMBER 1982 – REVISED MAY 1997

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

typical clear, shift, load, inhibit, and shift sequence



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8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HC166			SN74HC166			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0	0.5	0	0.5		V
		$V_{CC} = 4.5$ V	0	1.35	0	1.35		
		$V_{CC} = 6$ V	0	1.8	0	1.8		
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t^\ddagger	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	0	1000		ns
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
T_A	Operating free-air temperature	–55		125	–40		85	°C

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC166		SN74HC166		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t _w	CLR low	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t _{su}	SH/LD high before CLK↑	2 V	145		220		180		ns
		4.5 V	29		44		36		
		6 V	25		38		31		
	SER before CLK↑	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
	CLK INH low before CLK↑	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
	Data before CLK↑	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
	CLR inactive before CLK↑	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
t _h	SH/LD high after CLK↑	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		
	SER after CLK↑	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		
	CLK INH high after CLK↑	2 V	0		0		0		
		4.5 V	0		0		0		
		6 V	0		0		0		
	Data after CLK↑	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		



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SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	11		4.2		5	MHz	
			4.5 V	31	36		21		25		
			6 V	36	45		25		29		
t _{PHL}	$\overline{\text{CLR}}$	Q _H	2 V		62	120		180		150	ns
			4.5 V		18	24		36		30	
			6 V		13	20		31		26	
t _{pd}	CLK	Q _H	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t _t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

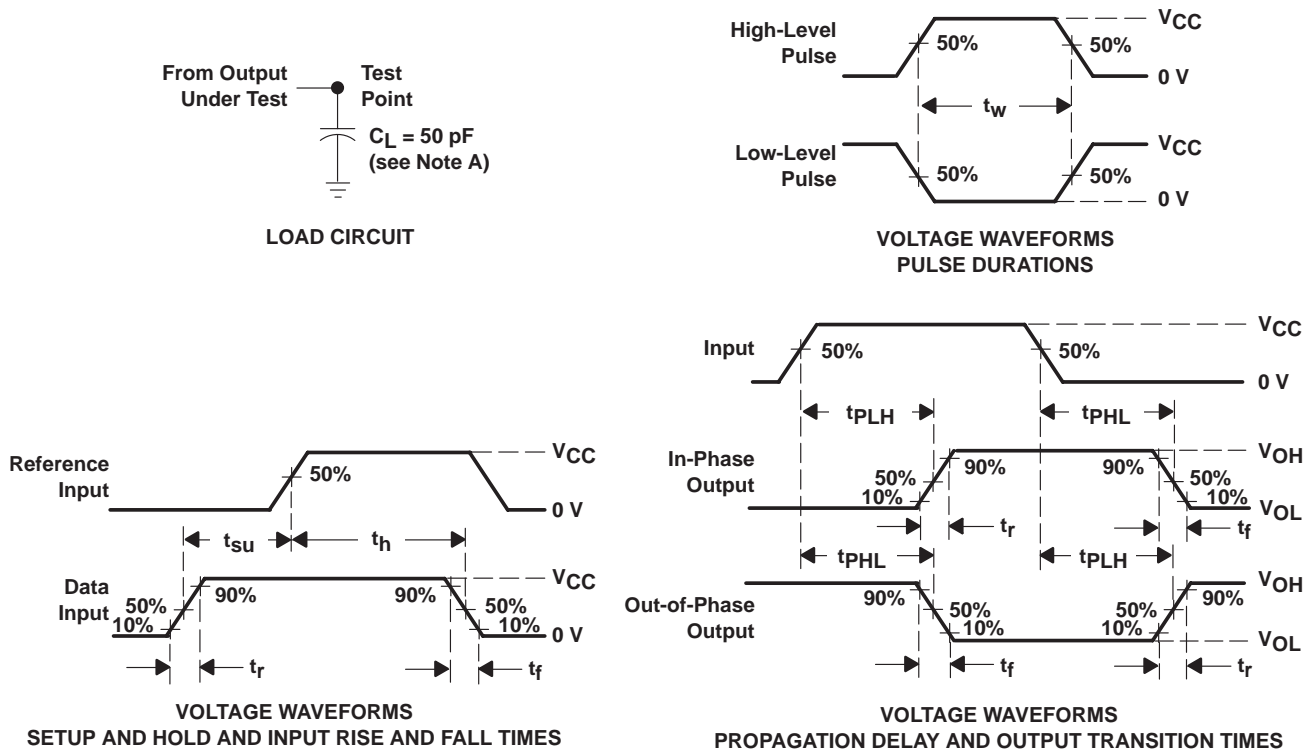
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	50	pF



SN54HC166, SN74HC166 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS117B – DECEMBER 1982 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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