

SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

SDLS007

D2635, JANUARY 1981 - REVISED MARCH 1988

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Accurate Shift-Frequency . . . DC to 20 MHz

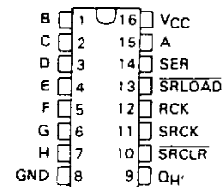
description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

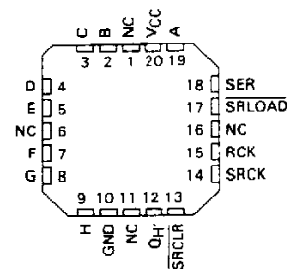
SN54LS597 . . . J OR W PACKAGE
SN74LS597 . . . N PACKAGE

(TOP VIEW)



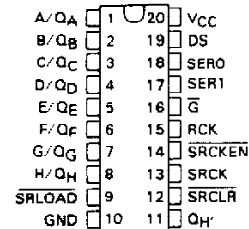
SN54LS597 . . . FK PACKAGE

(TOP VIEW)



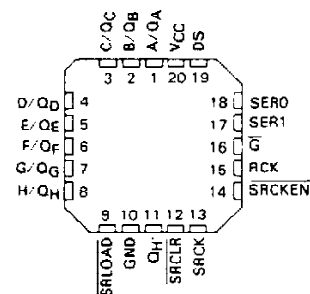
SN54LS598 . . . J OR W PACKAGE
LS598 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS598 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

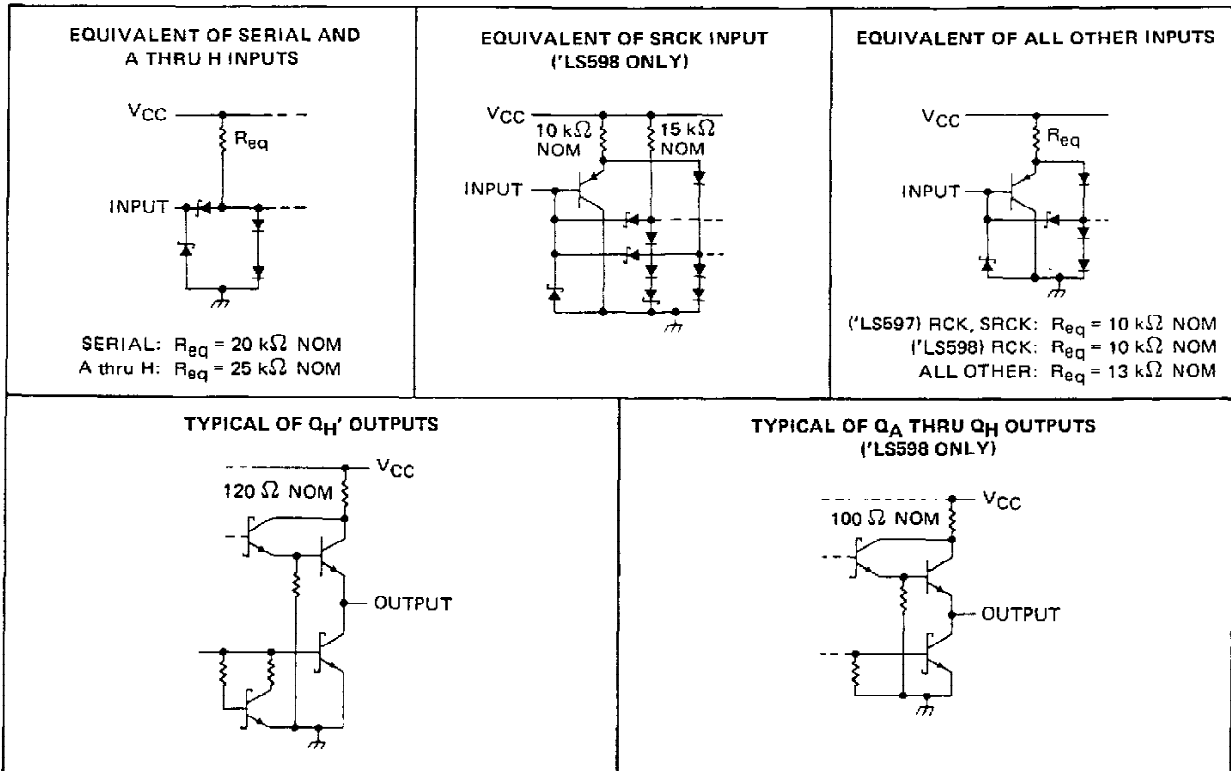
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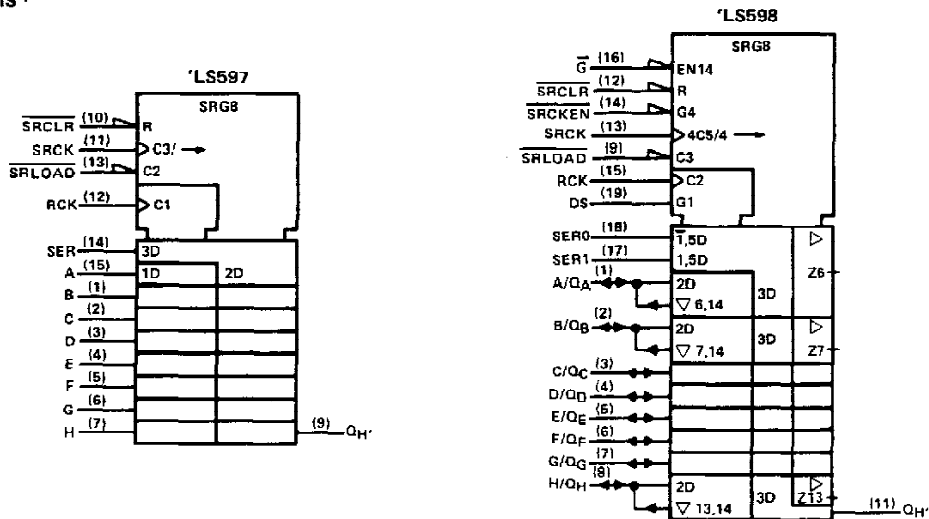
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schematics of inputs and outputs



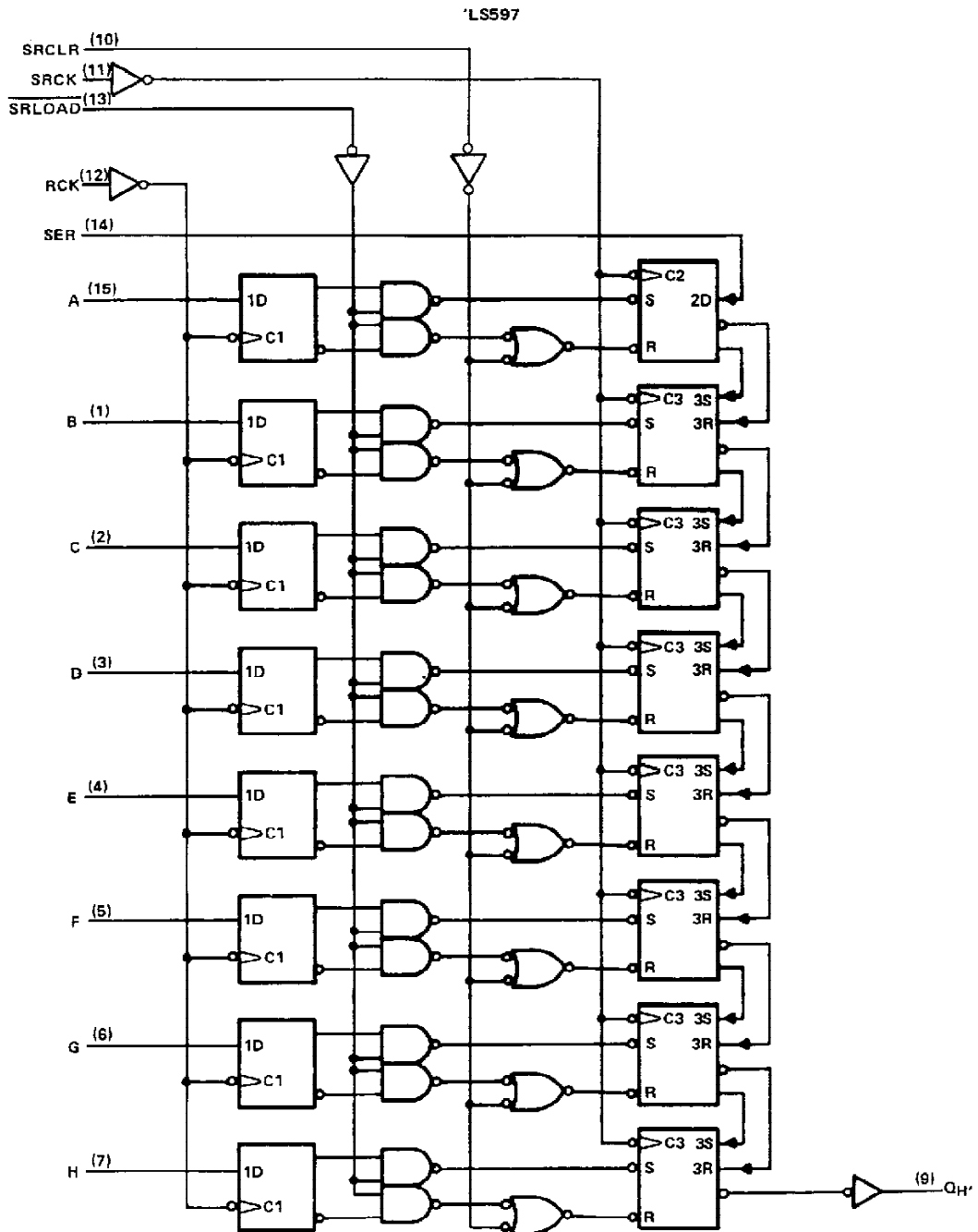
logic symbols †



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

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logic diagram (positive logic)



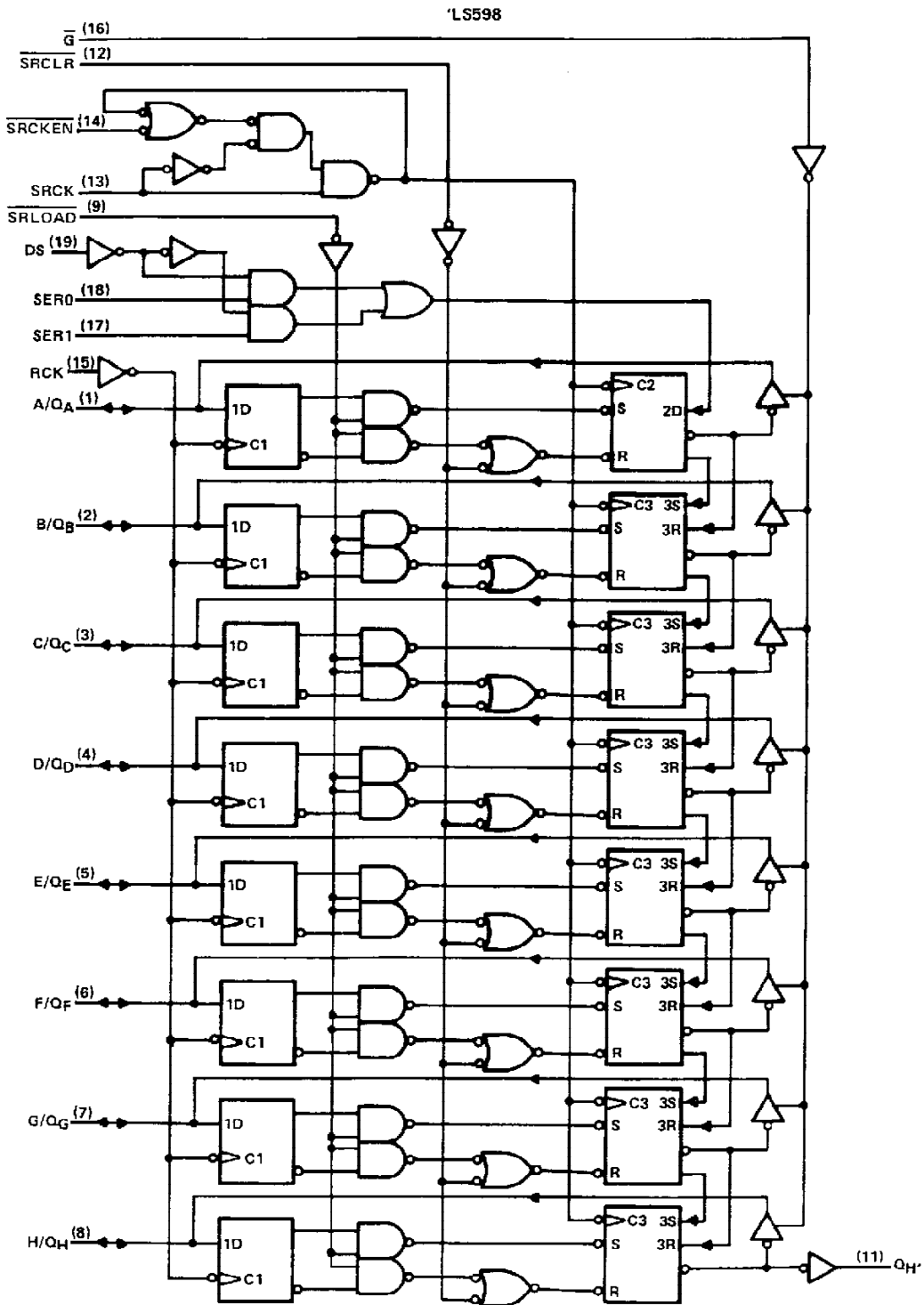
Pin numbers shown are for DW, J, N, and W packages.



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SN54LS598, SN74LS598
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logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598	- 55°C to 125°C
SN74LS597, SN74LS598	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
I_{OH}	High-level output current	Q_H'		- 1	Q_H'		- 1	mA
		Q_A thru Q_H , 'LS598 only		- 1	Q_A thru Q_H , 'LS598 only		- 2.6	
I_{OL}	Low-level output current	Q_H'		8	Q_H'		16	mA
		Q_A thru Q_H , 'LS598 only		12	Q_A thru Q_H , 'LS598 only		24	
f_{SCK}	Shift clock frequency	0		20	0		20	MHz
t_w	Pulse duration	SRCK	high	15	15		ns	
			low	35	35			
		RCK		20	20			
		SRCLR		20	20			
t_{su}	Setup time	Data before RCK ↑		20	20		ns	
		DS before SRCK ↑ ('LS598 only)		30	30			
		SRCKEN low before SRCK ↑ ('LS598 only)		20	20			
		SRCLR inactive before SRCK ↑		25	25			
		SRLOAD inactive before SRCK ↑		30	30			
		RCK ↑ before SRLOAD ↑ (see Note 2)		40	40			
SER before SRCK ↑		20	20					
t_h	Hold time	0			0			ns
T_A	Operating free-air temperature	- 55		125	0		70	°C

NOTE 2: The RCK ↑ before SRLOAD ↑ setup time ensures the data saved by RCK ↑ will also be loaded into the shift register.


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8-BIT SHIFT REGISTERS WITH INPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V		
V _{OH}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA	2.4	3.2			V		
	Q _H '		I _{OH} = -2.6 mA			2.4	3.1			
V _{OL}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V	
	Q _H '		I _{OL} = 24 mA				0.35	0.5		
			I _{OL} = 8 mA		0.25	0.4		0.25		0.4
			I _{OL} = 16 mA					0.35		0.5
I _{OZH}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V, V _{IL} = MAX					20	μA		
I _{OZL}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V, V _{IL} = MAX					-0.4	mA		
I _I	'LS598 Q	V _{CC} = MAX	V _I = 5.5 V					0.1	mA	
	Others		V _I = 7 V					0.1		
I _{IH}		V _{CC} = MAX, V _I = 2.7 V						20	μA	
I _{IL}	'LS598 SRCK	V _{CC} = MAX, V _I = 0.4 V						-0.8	mA	
	SER, A Thru H							-0.4		
	Others							-0.2		
I _{OS} §	'LS598 Q	V _{CC} = MAX, V _O = 0 V		-30	-130		-30	-130	mA	
	Q _H '			-20	-100		-20	-100		
I _{CC}	'LS597	V _{CC} = MAX, All possible inputs grounded, All outputs open	I _{CC} H	35	53		35	53	mA	
			I _{CC} L	35	53		35	53		
	'LS598		I _{CC} H	45	68		45	68		
			I _{CC} L	54	80		54	80		
			I _{CC} Z	56	85		56	85		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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8-BIT SHIFT REGISTERS WITH INPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LS597			LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	SRCK	Q	$R_L = 667\ \Omega$, $C_L = 45\ \mu\text{F}$	20	35		20	35		MHz
f_{max}	SRCK	Q_H'	$R_L = 1\ \text{k}\Omega$, $C_L = 30\ \text{pF}$	20	35					MHz
t_{PLH}	SRCK \uparrow	Q_H'	$R_L = 1\ \text{k}\Omega$, $C_L = 30\ \text{pF}$		15	23		11	17	ns
t_{PHL}	SPCK \uparrow	Q_H'			20	30		15	23	ns
t_{PLH}	SRLOAD \downarrow	Q_H'			38	57		28	42	ns
t_{PHL}	SRLOAD \downarrow	Q_H'			29	44		20	30	ns
t_{PHL}	SRCLR \downarrow	Q_H'			24	36		18	27	ns
t_{PLH}	RCK \uparrow	Q_H'	$R_L = 1\ \text{k}\Omega$, $C_L = 30\ \text{pF}$	41	60		32	48		ns
t_{PHL}	RCK \uparrow	Q_H'	SRLOAD = L	32	48		24	36		ns
t_{PLH}	SRCK \uparrow	Q	$R_L = 667\ \Omega$, $C_L = 45\ \mu\text{F}$					12	18	ns
t_{PHL}	SRCK \uparrow	Q						19	28	ns
t_{PLH}	SRLOAD \downarrow	Q						32	48	ns
t_{PHL}	SRLOAD \downarrow	Q						27	40	ns
t_{PHL}	SRCLR \downarrow	Q						25	38	ns
t_{PZH}	G \downarrow	Q						26	31	ns
t_{PZL}	G \downarrow	Q						29	43	ns
t_{PHZ}	G \uparrow	Q	$R_L = 667\ \Omega$, $C_L = 5\ \text{pF}$					25	38	ns
t_{PLZ}	G \uparrow	Q						20	30	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

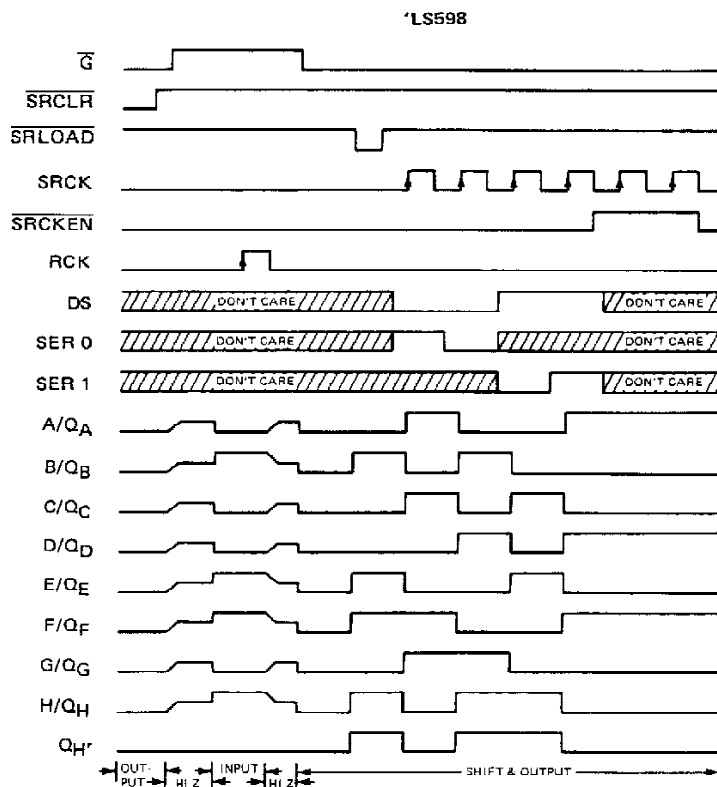
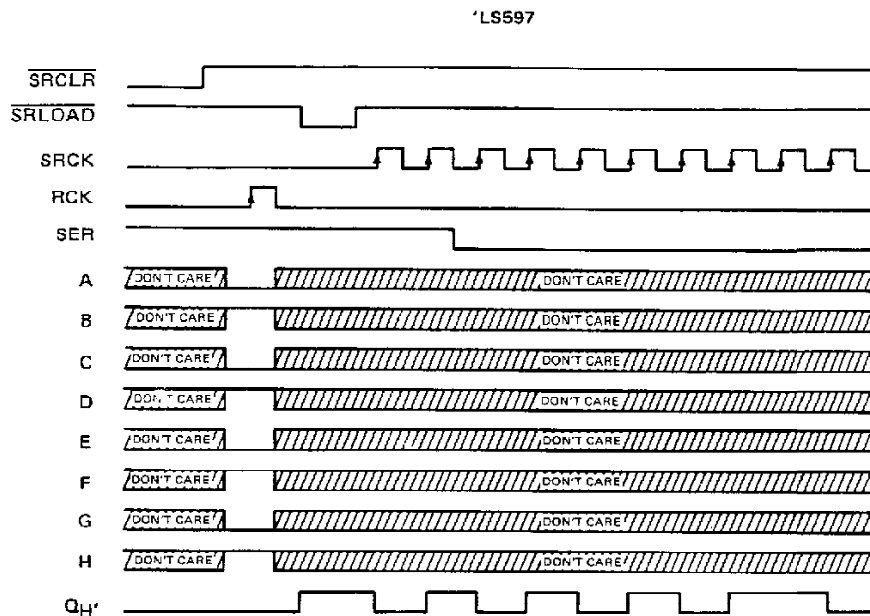


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8-BIT SHIFT REGISTERS WITH INPUT LATCHES

typical operating sequences




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