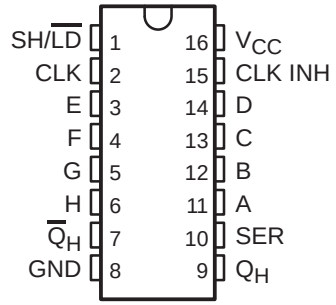
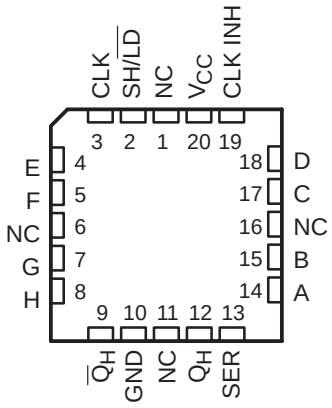
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) < 2 V at V_{CC}, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV165A . . . J OR W PACKAGE
SN74LV165A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV165A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ’LV165A devices feature a clock inhibit function and a complemented serial output $\overline{Q}_H$.

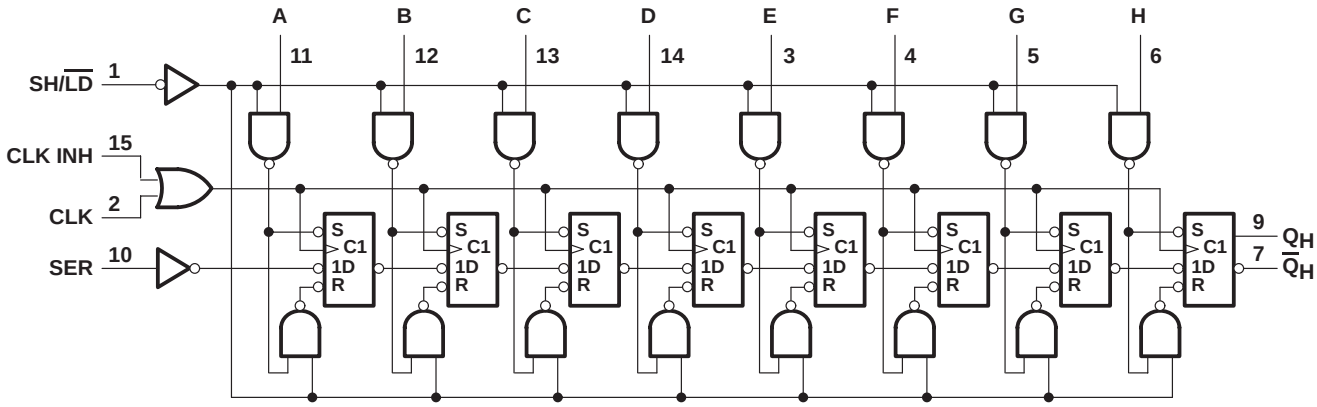
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of the CLK and CLK INH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is held low, independently of the levels of CLK, CLK INH, or SER.

The SN54LV165A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV165A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

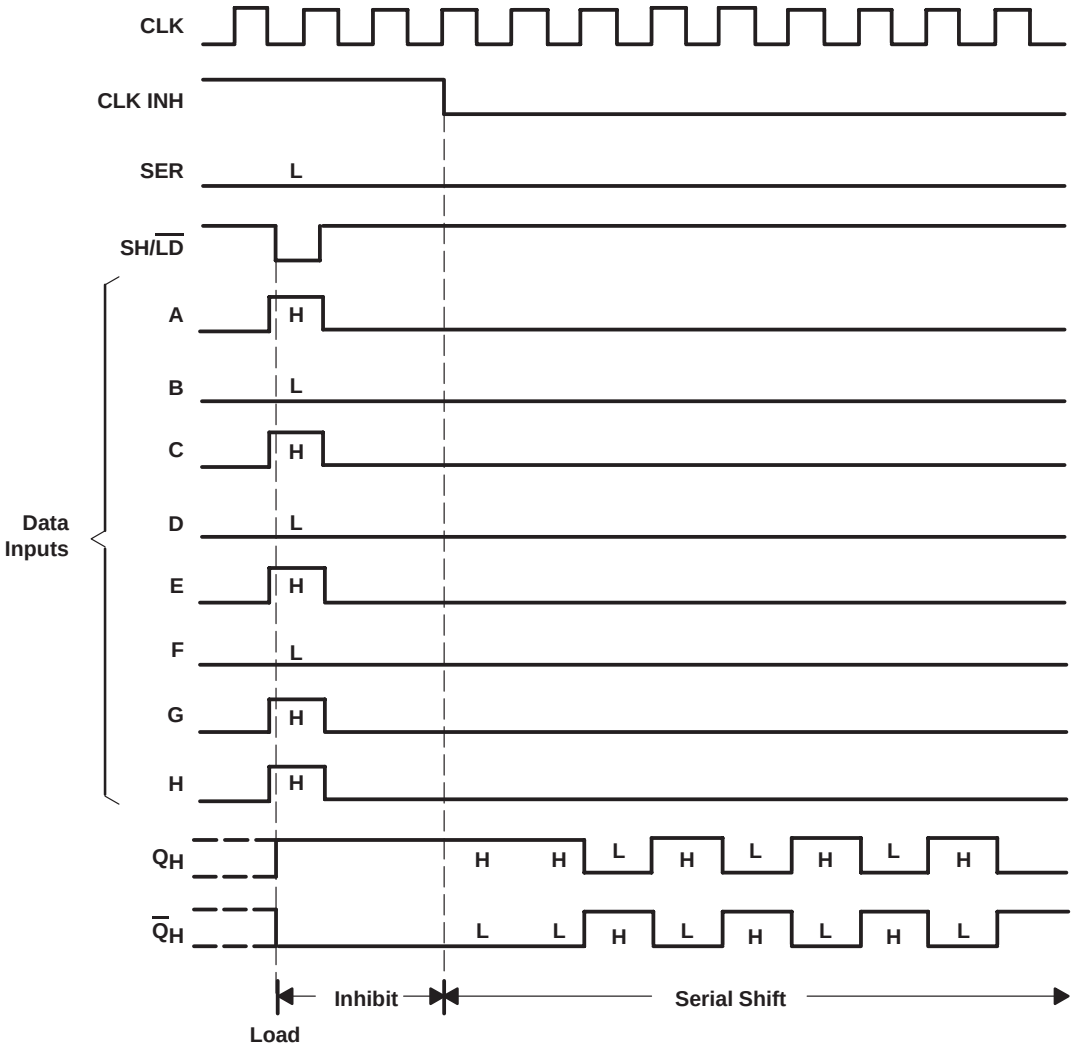
INPUTS			OPERATION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
DGV package . . . . . 180°C/W
NS package . . . . . 111°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–6		–6	
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV165A			SN74LV165A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –6 mA	3 V	2.48			2.48			
	I_{OH} = –12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	5.5 V			±1			±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		1.7			1.7		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	8.5		9		9		ns
		SH/$\overline{LD}$ low	11		13		13		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	7		8.5		8.5		ns
		SER before CLK↑	8.5		9.5		9.5		
		CLK INH before CLK↑	7		7		7		
		Data before SH/$\overline{LD}$↑	11.5		12		12		
t_h	Hold time	SER data after CLK↑	–1		0		0		ns
		Parallel data after SH/$\overline{LD}$↑	0		0.5		0.5		
		SH/$\overline{LD}$ high after CLK↑	0		0		0		

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	6		7		7		ns
		SH/$\overline{LD}$ low	7.5		9		9		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	5		6		6		ns
		SER before CLK↑	5		6		6		
		CLK INH before CLK↑	5		5		5		
		Data before SH/$\overline{LD}$↑	7.5		8.5		8.5		
t_h	Hold time	SER data after CLK↑	0		0		0		ns
		Parallel data after SH/$\overline{LD}$↑	0.5		0.5		0.5		
		SH/$\overline{LD}$ high after CLK↑	0		0		0		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV165A		SN74LV165A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	4		4		4		ns
		SH/$\overline{LD}$ low	5		6		6		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	4		4		4		ns
		SER before CLK↑	4		4		4		
		CLK INH before CLK↑	3.5		3.5		3.5		
		Data before SH/$\overline{LD}$↑	5		5		5		
t_h	Hold time	SER data after CLK↑	0.5		0.5		0.5		ns
		Parallel data after SH/$\overline{LD}$↑	1		1		1		
		SH/$\overline{LD}$ high after CLK↑	0.5		0.5		0.5		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	50	80		45		45		MHz
			C_L = 50 pF	40	65		35		35		
t_{pd}*	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		12.2	19.8	1	22	1	22	ns
	SH/$\overline{LD}$				13.1	21.5	1	23.5	1	23.5	
	H				12.9	21.7	1	24	1	24	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		15.3	23.3	1	26	1	26	ns
	SH/$\overline{LD}$				16.1	25.1	1	28	1	28	
	H				15.9	25.3	1	28	1	28	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	65	115		55		55		MHz
			C_L = 50 pF	60	90		50		50		
t_{pd}*	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		8.6	15.4	1	18	1	18	ns
	SH/$\overline{LD}$				9.1	15.8	1	18.5	1	18.5	
	H				8.9	14.1	1	16.5	1	16.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		10.9	18.9	1	21.5	1	21.5	ns
	SH/$\overline{LD}$				11.3	19.3	1	22	1	22	
	H				11.1	17.6	1	20	1	20	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

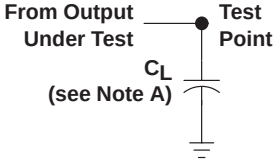
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF*	110	165		90		90		MHz
			C_L = 50 pF	95	125		85		85		
t_{pd}*	CLK	Q_H or $\overline{Q}_H$	C_L = 15 pF		6	9.9	1	11.5	1	11.5	ns
	SH/$\overline{LD}$				6	9.9	1	11.5	1	11.5	
	H				6	9	1	10.5	1	10.5	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	C_L = 50 pF		7.7	11.9	1	13.5	1	13.5	ns
	SH/$\overline{LD}$				7.7	11.9	1	13.5	1	13.5	
	H				7.6	11	1	12.5	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

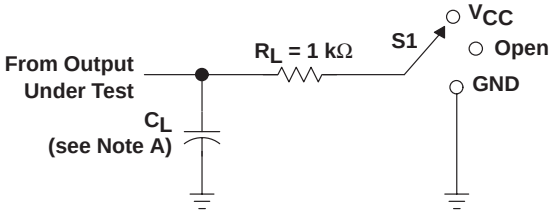
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	36.1	pF
				5 V	37.5	

PARAMETER MEASUREMENT INFORMATION

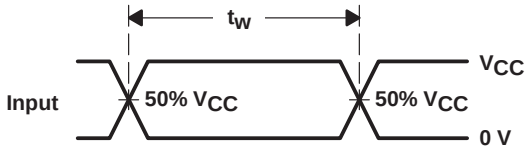


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

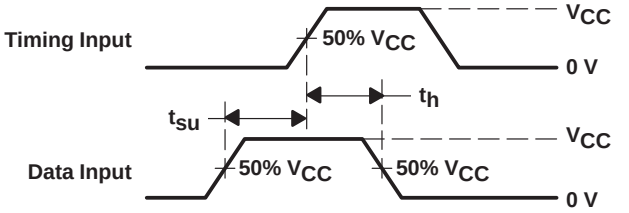


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

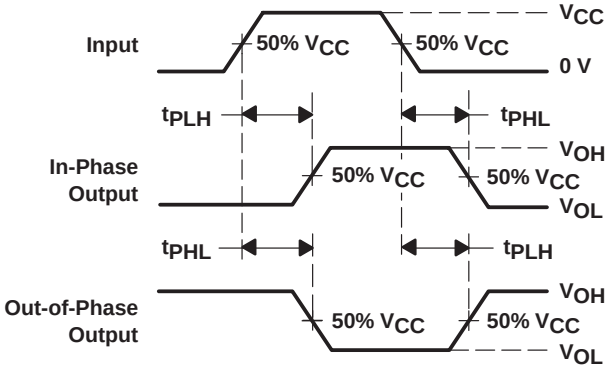
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



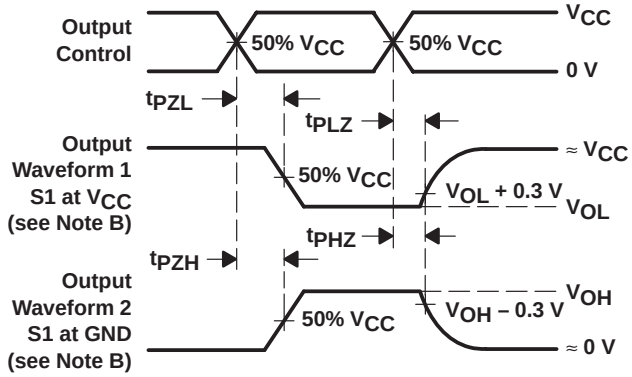
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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