TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS101

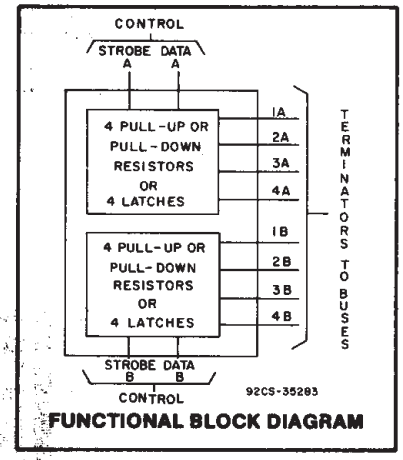
NOT RECOMMENDED FOR NEW DESIGNS

CD40117B Types

Programmable Dual 4-Bit Terminator

High-Voltage Types (20-Volt Rating)

Features:
- *One standard "B" output will drive eight terminator circuits.*
- *Will terminate a CMOS data bus with up to 40 B-series inputs inputs or 3-state outputs connected at VDD of 5 V.*
- *Input terminals protected by standard "B" series ESD protection network.*
- *Preserves final logic state.*
- *Output after switching is closer to VDD or VSS rail than with a resistor.*
- *Requires only one solder connection.*
- *Open circuited terminator not used will not affect performance.*
- *Can be connected to any CMOS I/O line.*
- *Draws current only when logic state is changing.*
- *Can be preset.*



FUNCTIONAL BLOCK DIAGRAM

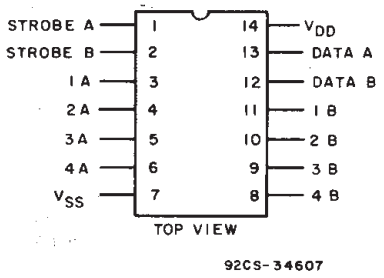
■ CD40117B is a dual 4-bit terminator that can be programmed by means of STROBE and DATA control bits to function as pull-up or pull-down resistors. The CD40117B can also be programmed to function as latches to terminate any open or unused CMOS logic when used with 3-state logic or during a power-down condition. Considerable savings in power and board space can be realized when this device is used to replace pull-up or pull-down resistors. When the STROBE is in the logic "1" state, the terminator functions as a pull-up resistor if the DATA input is a logic "1" or as a pull-down resistor if the DATA input is a logic "0".

When the STROBE is in the logic "0" state, the terminator performs the latch function, i.e., it follows the changing states of the bus. If the bus goes into the high-Z state or into a power-down condition, the latched terminator retains the data ("1" or "0") that the bus carried before it switched to the high-Z or power-down state. If and when the bus changes from the high-Z state to the state opposite to that which the latch is storing, the bus will override the latch and the terminator will reflect the state on the bus. The small geometries chosen for the inverters in the latch allow this override mode. When checking the data bus whose last state is being preserved by the terminator, a resistor should be used in series with the probe whose input capacitance could trip the small latches. The resistance should be in excess of the output impedance of the latch, i.e., R should be > 30 KΩ at V_{DD} = 10 V.

The STROBE and DATA inputs in each section can be paralleled allowing this device to be used as an 8-bit bus terminator.

The CD40117B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Applications:
- *Error state identification.*
- *Replaces pull-up or pull-down resistors*
- *Avoids floating inputs in modular systems*
- *Sharpens transistors (hysteresis)*
- *Anti-bounce circuit*



TERMINAL DIAGRAM

TRUTH TABLE

STROBE	DATA	1A(B)	2A(B)	3A(B)	4A(B)
1	0	0Δ	0Δ	0Δ	0Δ
1	1	1+	1+	1+	1+
0	X	*	*	*	*

1 = High, 0 = Low, X = Don't Care

Δ Equivalent to pull-down resistor.
+ Equivalent to pull-up resistor.
*Equivalent to a latch.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	—	3	18	V

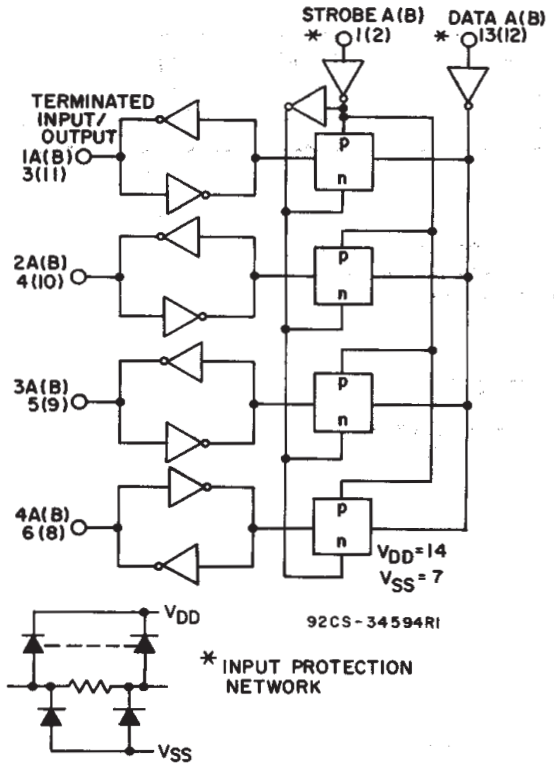
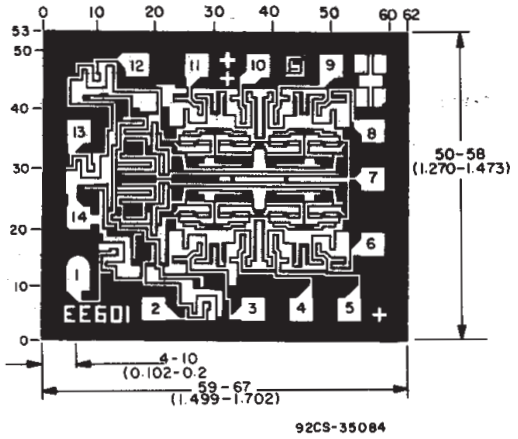


Fig. 1 - Logic diagram (¼ of CD40117B)



Dimensions and pad layout for CD40117B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TYPICAL APPLICATIONS

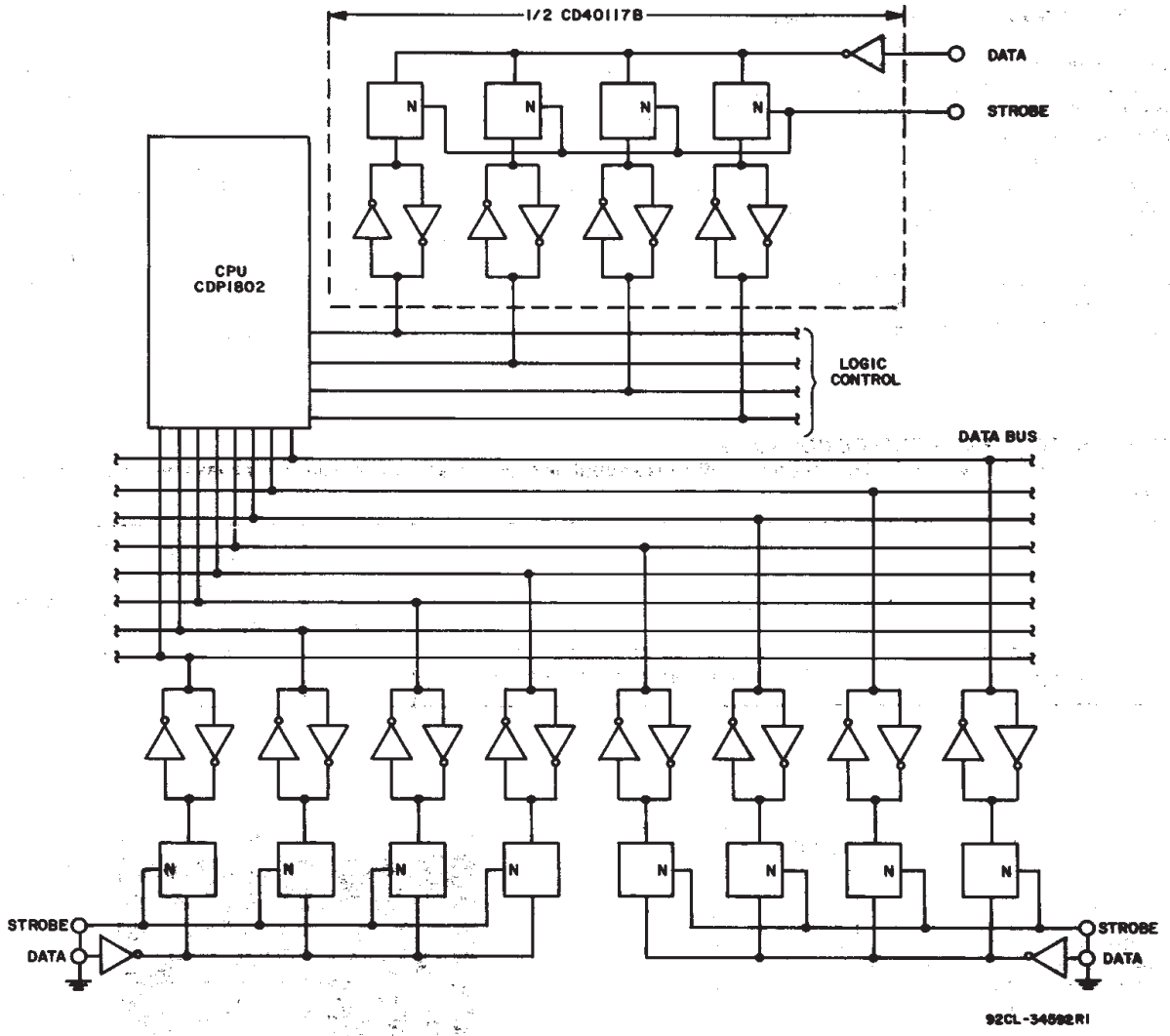


Fig. 2 - Schematic of CD40117B interfacing with microprocessor terminating an 8-bit bus line and 1/2 of CD40117B as a programmable pull-up/pull down logic controller.

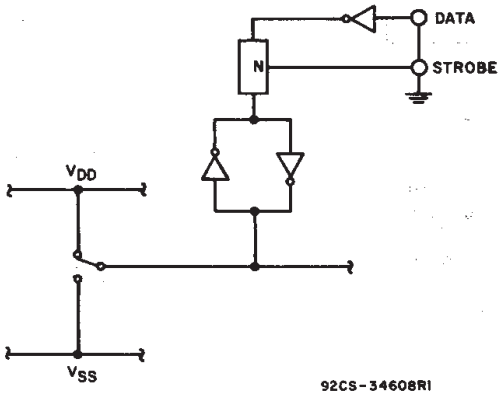


Fig. 3 - Schematic of CD40117B in anti-bounce circuit application.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current Max.	I_{DD}	—	0, 5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
		—	0, 10	10	0.5	0.5	15	15	—	0.01	0.5	
		—	0, 15	15	1	1	30	30	—	0.01	1	
		—	0, 20	20	5	5	150	150	—	0.02	5	
Output Low Sink Current Min.	I_{OL}	0.4	0, 5	5	—	—	—	—	—	25	—	μA
		0.5	0, 10	10	—	—	—	—	—	60	—	
		1.5	0, 15	15	—	—	—	—	—	250	—	
Output High (Source) Current Min.	I_{OH}	4.6	0, 5	5	—	—	—	—	—	-25	—	
		2.5	0, 5	5	—	—	—	—	—	—	—	
		9.5	0, 10	10	—	—	—	—	—	-60	—	
		13.5	0, 15	15	—	—	—	—	—	-250	—	
Output Voltage: Low-Level Max.	V_{OL}	—	0, 5	5	0.05				—	0	0.05	V
		—	0, 10	10	0.05				—	0	0.05	
		—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	V_{OH}	—	0, 5	5	4.95				4.95	5	—	
		—	0, 10	10	9.95				9.95	10	—	
		—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max.	V_{IL}	0.5, 4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5, 13.5	—	15	4				—	—	4	
Input High Voltage Min.	V_{IH}	0.5, 4.5	—	5	3.5				3.5	—	—	
		1, 9	—	10	7				7	—	—	
		1.5, 13.5	—	15	11				11	—	—	
Input Current Max.	I_{IN}	—	0, 18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS All Packages MIN.	TYP.	MAX.	UNITS
Propagation Delay Time Strobe, Data to Outputs	t_{PHL}	5	—	1.7	—	μs
		10	—	850	—	ns
		15	—	575	—	ns
	t_{PLH}	5	—	1.5	—	μs
		10	—	625	—	ns
		15	—	500	—	ns
Transition Time	t_{THL}, t_{TLH}	5	—	3.3	—	μs
		10	—	1.6	—	
		15	—	1.1	—	
Minimum Strobe Pulse Width	t_W	5	—	1.5	—	μs
		10	—	600	—	ns
		15	—	475	—	ns
Minimum Data Pulse Width	t_{WH}, t_{WL}	5	—	1.6	—	μs
		10	—	700	—	ns
		15	—	500	—	ns
Minimum Terminator Input/Output Pulse Width	t_W	5	—	10	—	ns
Minimum Data Setup Time Data to Strobe	t_{SU}	5	—	0	—	ns
		10	—	0	—	
		15	—	0	—	
Input Capacitance	C_{IN}	Any Input	—	5	—	pF

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