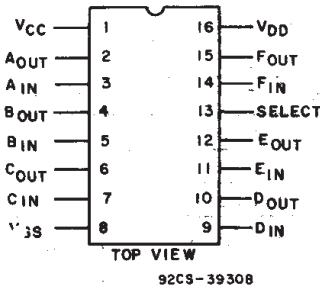


# CD4504B Types



**TERMINAL ASSIGNMENT**

## CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)

**Features:**

- Independence of power-supply sequence considerations— $V_{CC}$  can exceed  $V_{DD}$ ; input signals can exceed both  $V_{CC}$  and  $V_{DD}$
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the  $V_{CC}$  logic level to the  $V_{DD}$  logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the  $V_{CC}$  HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B device is supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead dual-in-line surface-mount plastic packages (M suffix), and in chip form (H suffix).

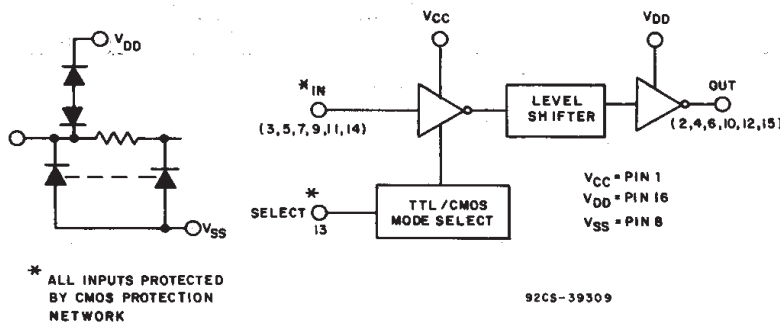


Fig. 1 - Functional diagram for CD4504B.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

|  |  |
|--|--|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )  | -0.5V to +20V                                      |
| Voltages referenced to $V_{SS}$ Terminal)                                    |  |
| INPUT VOLTAGE RANGE, ALL INPUTS  | -0.5V to $V_{DD} + 0.5V$                           |
| DC INPUT CURRENT, ANY ONE INPUT  | $\pm 10$ mA  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                     |  |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                        | 500mW  |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                       | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR:                                    |  |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$        | 100mW  |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )  | $-55^\circ\text{C}$ to $+125^\circ\text{C}$        |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                                      | $-65^\circ\text{C}$ to $+150^\circ\text{C}$        |
| LEAD TEMPERATURE (DURING SOLDERING):   |  |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max | $+265^\circ\text{C}$                               |

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## CD4504B Types

### STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC  | CONDITIONS            |                        |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |   |
|---|-----------------------|------------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|---|
|   | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>CC</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |   |
|   |                       |                        |                        |                        |                                       |       |       |       | MIN   | TYP               | MAX  |       |   |
| Quiescent Device Current, I <sub>DD</sub> Max and I <sub>CC</sub> in CMOS-CMOS Mode | —                     | 0,5                    | 5                      | 5                      | 1                                     | 1     | 30    | 30    | —     | 0.02              | 1    | μA    |   |
|   | —                     | 0,10                   | 5                      | 10                     | 2                                     | 2     | 60    | 60    | —     | 0.02              | 2    |       |   |
|   | —                     | 0,15                   | 5                      | 15                     | 4                                     | 4     | 120   | 120   | —     | 0.02              | 4    |       |   |
|   | —                     | 0,20                   | 5                      | 20                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |   |
| Quiescent Device Current, I <sub>CC</sub> Max TTL-CMOS Mode                         | —                     | 0,5                    | 5                      | 5                      | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    | mA    |   |
|   | —                     | 0,10                   | 5                      | 10                     | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    |       |   |
|   | —                     | 0,15                   | 5                      | 15                     | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    |       |   |
| Output Low (Sink) Current, I <sub>OL</sub> Min                                      | 0.4                   | 0,5                    | —                      | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |   |
|   | 0.5                   | 0,10                   | —                      | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |   |
|   | 1.5                   | 0,15                   | —                      | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |   |
| Output High (Source) Current, I <sub>OH</sub> Min                                   | 4.8                   | 0,5                    | —                      | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |   |
|   | 2.5                   | 0,5                    | —                      | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |   |
|   | 9.5                   | 0,10                   | —                      | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |   |
|   | 13.5                  | 0,15                   | —                      | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |   |
| Output Voltage: Low-Level, V <sub>OL</sub> Max                                      | —                     | 0,5                    | —                      | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |   |
|   | —                     | 0,10                   | —                      | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |   |
|   | —                     | 0,15                   | —                      | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |   |
| Output Voltage: High-Level, V <sub>OH</sub> Min                                     | —                     | 0,5                    | —                      | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |   |
|   | —                     | 0,10                   | —                      | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |   |
|   | —                     | 0,15                   | —                      | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |   |
| Input Low Voltage, V <sub>IL</sub> Max Note 1                                       | TTL-CMOS              | 1                      | —                      | 5                      | 10                                    | 0.8   |       |       |       | —                 | —    | 0.8   | V |
|   | TTL-CMOS              | 1                      | —                      | 5                      | 15                                    | 0.8   |       |       |       | —                 | —    | 0.8   |   |
|   | CMOS-CMOS             | 1                      | —                      | 5                      | 10                                    | 1.5   |       |       |       | —                 | —    | 1.5   |   |
|   | CMOS-CMOS             | 1.5                    | —                      | 5                      | 15                                    | 1.5   |       |       |       | —                 | —    | 1.5   |   |
|   | CMOS-CMOS             | 1.5                    | —                      | 10                     | 15                                    | 3     |       |       |       | —                 | —    | 3     |   |
| Input High Voltage, V <sub>IH</sub> Min Note 1                                      | TTL-CMOS              | 9                      | —                      | 5                      | 10                                    | 2     |       |       |       | 2                 | —    | —     | V |
|   | TTL-CMOS              | 13.5                   | —                      | 5                      | 15                                    | 2     |       |       |       | 2                 | —    | —     |   |
|   | CMOS-CMOS             | 9                      | —                      | 5                      | 10                                    | 3.5   |       |       |       | 3.5               | —    | —     |   |
|   | CMOS-CMOS             | 13.5                   | —                      | 5                      | 15                                    | 3.5   |       |       |       | 3.5               | —    | —     |   |
|   | CMOS-CMOS             | 13.5                   | —                      | 10                     | 15                                    | 7     |       |       |       | 7                 | —    | —     |   |
| Input Current, I <sub>IN</sub> Max  | —                     | 0,18                   | —                      | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |   |

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

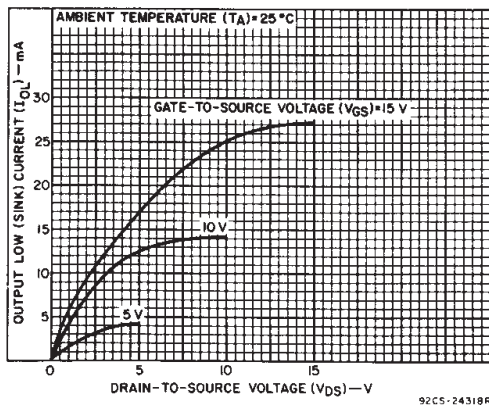


Fig. 2 - Typical output low (sink) current characteristics.

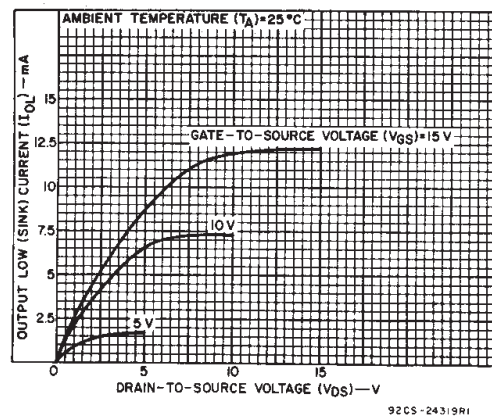


Fig. 3 - Minimum output low (sink) current characteristics.

# CD4504B Types

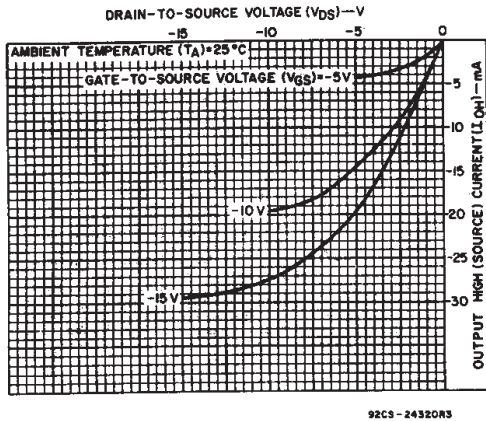


Fig. 4 - Typical output high (source) current characteristics.

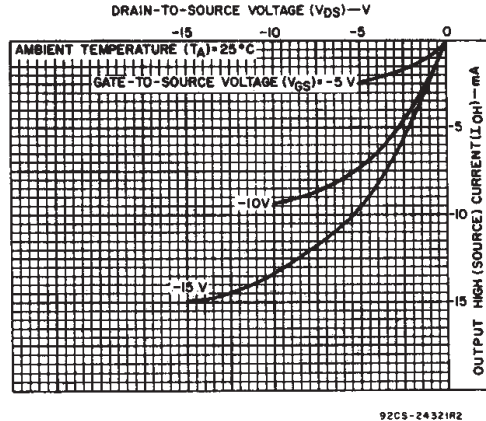


Fig. 5 - Minimum output high (source) current characteristics.

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | V <sub>DD</sub> (V) | LIMITS |      | UNITS |
|--|---------------------|--------|------|-------|
|  |                     | Min.   | Max. |       |
| Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range) | —                   | 3      | 18   | V     |

## DYNAMIC ELECTRICAL CHARACTERISTICS, At T<sub>A</sub> = 25°C; Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 Ω

| CHARACTERISTIC                                       | SHIFTING MODE                                     | V <sub>CC</sub> (V) | V <sub>DD</sub> (V) | LIMITS |      | UNITS |
|--|---|---------------------|---------------------|--------|------|-------|
|  |   |                     |                     | TYP.   | MAX. |       |
| Propagation Delay:<br>High-to-Low, t <sub>PHL</sub>  | TTL to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub>  | 5                   | 10                  | 140    | 280  | ns    |
|  | CMOS to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub> | 5                   | 10                  | 120    | 240  |       |
|  |   | 5                   | 15                  | 120    | 240  |       |
|  |   | 10                  | 15                  | 70     | 140  |       |
|  | CMOS to CMOS<br>V <sub>CC</sub> > V <sub>DD</sub> | 10                  | 5                   | 275    | 550  |       |
|  |   | 15                  | 5                   | 275    | 550  |       |
|  |   | 15                  | 10                  | 70     | 140  |       |
|  |   |                     |                     |        |      |       |
| Low-to-High, t <sub>PLH</sub>                        | TTL to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub>  | 5                   | 10                  | 140    | 280  | ns    |
|  | CMOS to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub> | 5                   | 10                  | 120    | 240  |       |
|  |   | 5                   | 15                  | 120    | 240  |       |
|  |   | 10                  | 15                  | 70     | 140  |       |
|  | CMOS to CMOS<br>V <sub>CC</sub> > V <sub>DD</sub> | 10                  | 5                   | 200    | 400  |       |
|  |   | 15                  | 5                   | 200    | 400  |       |
|  | 15  | 10                  | 60                  | 120    |      |       |
| Transition Time, t <sub>THL</sub> , t <sub>TLH</sub> | All Modes   |                     | 5                   | 100    | 200  |       |
|  |   |                     | 10                  | 50     | 100  |       |
|  |   |                     | 15                  | 40     | 80   |       |
| Input Capacitance, C <sub>IN</sub>                   | Any Input   |                     |                     | 5      | 7.5  | pF    |

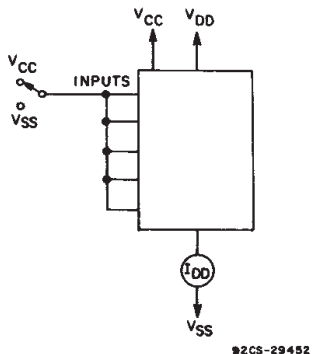


Fig. 6 - Quiescent device current.

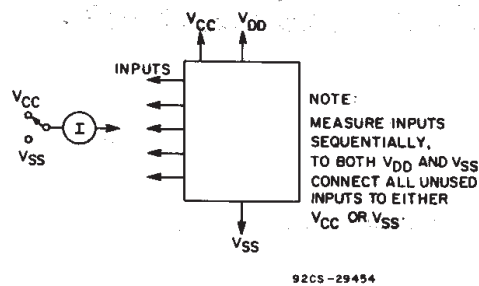


Fig. 7 - Input current.

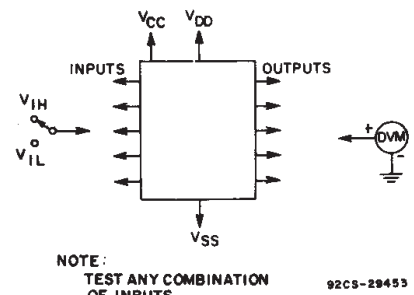


Fig. 8 - Input voltage.

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## CD4504B Types

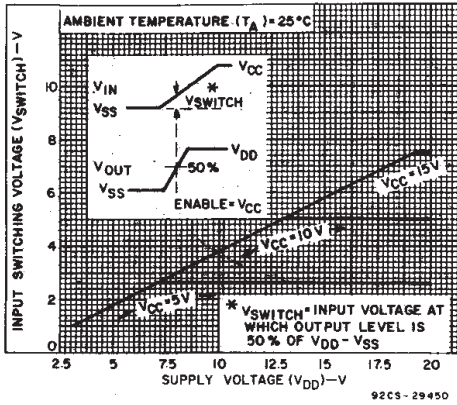


Fig. 9 - Typical input switching as a function of high-level supply voltage. (SELECT at  $V_{CC}$ -CMOS mode).

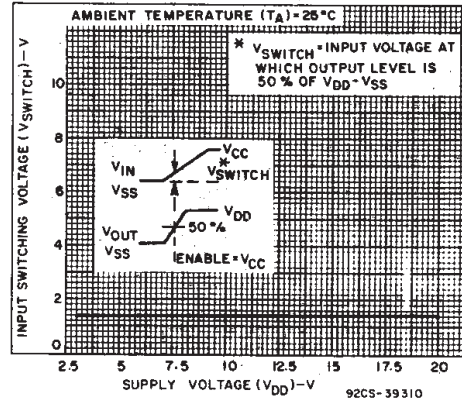


Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at  $V_{SS}$ -TTL mode).

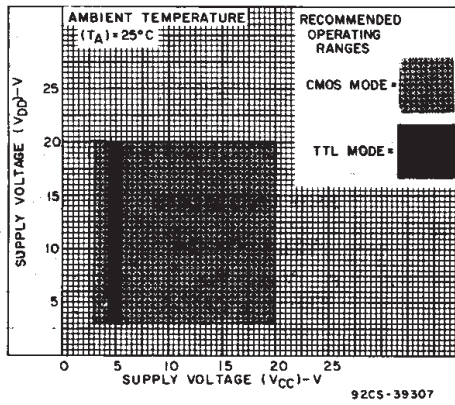
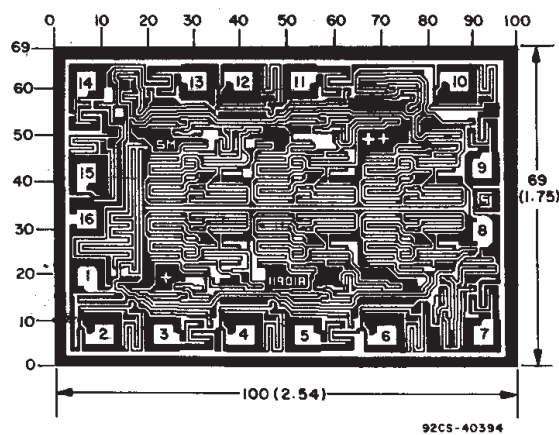


Fig. 11 - High-level supply voltage vs. low-level supply voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4504BH.

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