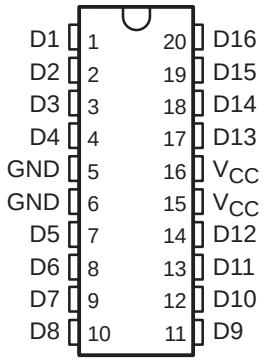
- **Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems**
- **Reduces Undershoot and Overshoot Caused By Line Reflections**
- **Repetitive Peak Forward Current . . . I_{FRM} = 100 mA**
- **Inputs Are TTL-Voltage Compatible**
- **Low Power Consumption (Like CMOS)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**

DW PACKAGE
(TOP VIEW)



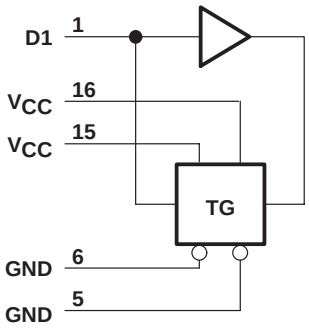
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1073 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1073 is characterized for operation from –40°C to 85°C.

logic diagram, one of sixteen channels (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Continuous input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Positive-peak input clamp current, I_{IK} (V_I > V_{CC}) (t_w < 1 µs, duty cycle < 20%) . . . . . 100 mA
Negative-peak input clamp current, I_{IK} (V_I < 0) (t_w < 1 µs, duty cycle < 20%) . . . . . –100 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TA = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
I_{IL}	V_{CC} = 4.5 to 5.5 V,	V_I = 0.8 V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	V_{CC} = 4.5 to 5.5 V,	V_I = 2.5 V	–0.2	–0.5	–1.4	–0.15	–1.5	mA
V_{IKL}	I_{IN} = –18 mA				–1.5		–1.5	V
V_{IKH}	I_{IN} = 18 mA				V_{CC}+2		V_{CC}+2	V
I_{CC}‡	V_{CC} = 5.5 V,	Inputs open			4		40	µA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at V_{CC} or GND			0.9		1	mA
C_i	V_I = V_{CC} or GND			3				pF

† All typical values are at V_{CC} = 5 V.
‡ Inputs may be set high or low prior to the I_{CC} measurement.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

TYPICAL CHARACTERISTICS

FORWARD CURRENT vs INPUT VOLTAGE (UPPER CLAMPING DIODE)

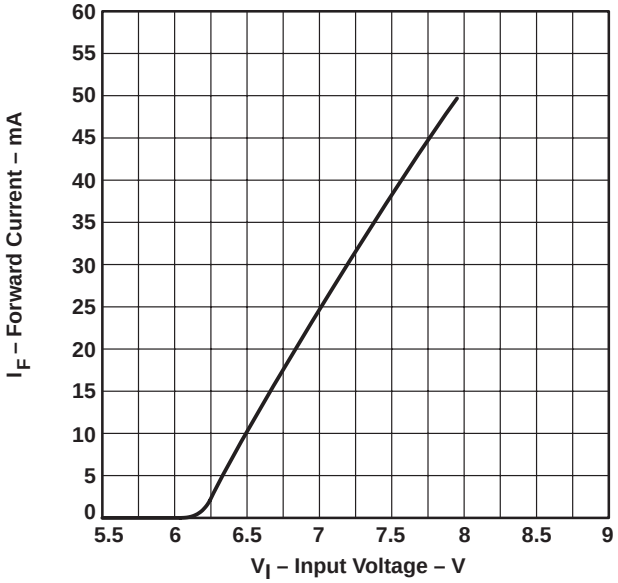


Figure 1

FORWARD CURRENT vs INPUT VOLTAGE (LOWER CLAMPING DIODE)

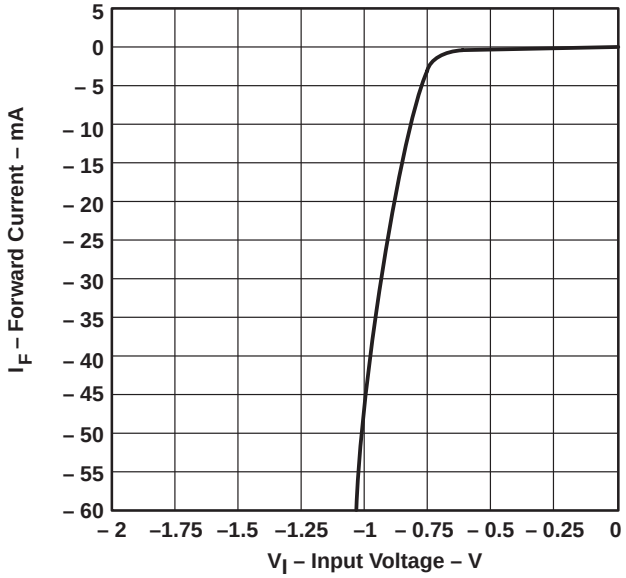


Figure 2

INPUT CURRENT vs INPUT VOLTAGE

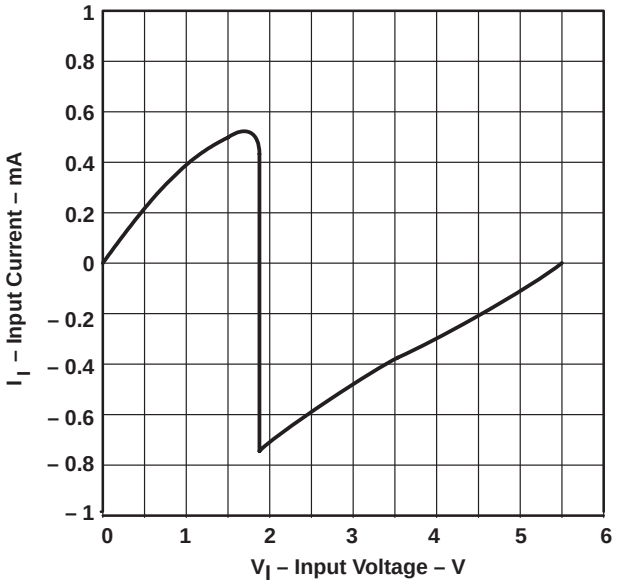


Figure 3

SUPPLY CURRENT vs INPUT VOLTAGE

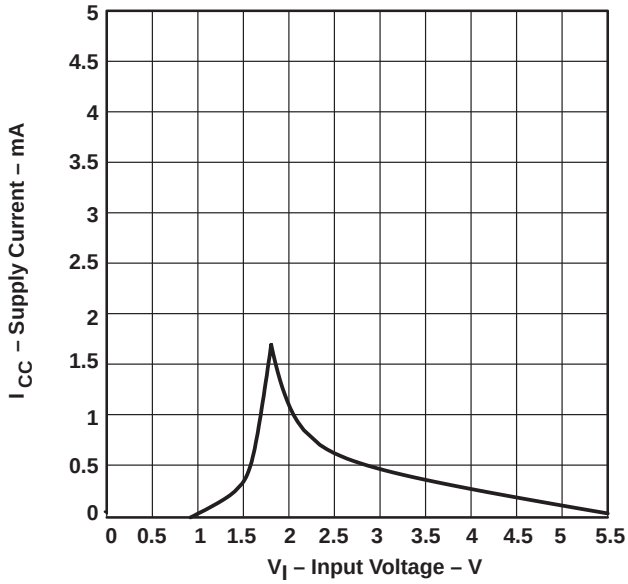


Figure 4

APPLICATION INFORMATION

The SN74ACT1073 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

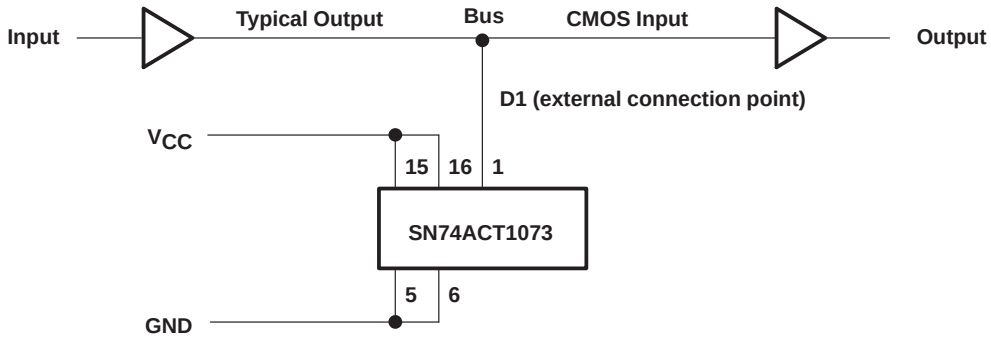


Figure 5. Bus-Hold Application

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