TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS205A

CD74HC4049, CD74HC4050

High-Speed CMOS Logic
Hex Buffers, Inverting and Non-Inverting

February 1998 - Revised June 1999

Features

- **Typical Propagation Delay: 6ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **High-to-Low Voltage Level Converter for up to V_I = 16V**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . –55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**

Description

The CD74HC4049 and CD74HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15-V input pulse levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. These parts also can be used as simple buffers or inverters without level translation. The CD74HC4049 and CD74HC4050 are enhanced versions of equivalent CMOS types.

Ordering Information

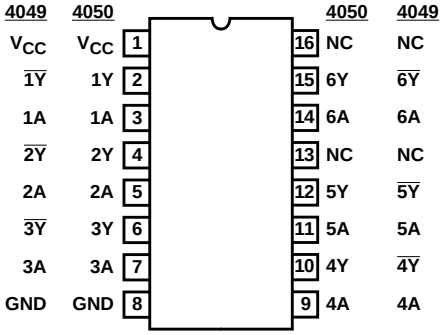
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4049E	–55 to 125	16 Ld PDIP	E16.3
CD74HC4050E	–55 to 125	16 Ld PDIP	E16.3
CD74HC4049M	–55 to 125	16 Ld SOIC	M16.15
CD74HC4050M	–55 to 125	16 Ld SOIC	M16.15
CD74HC4050PW	–55 to 125	16 Ld TSSOP	

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to the M suffix or the R suffix to the PW package to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or customer service for ordering information.

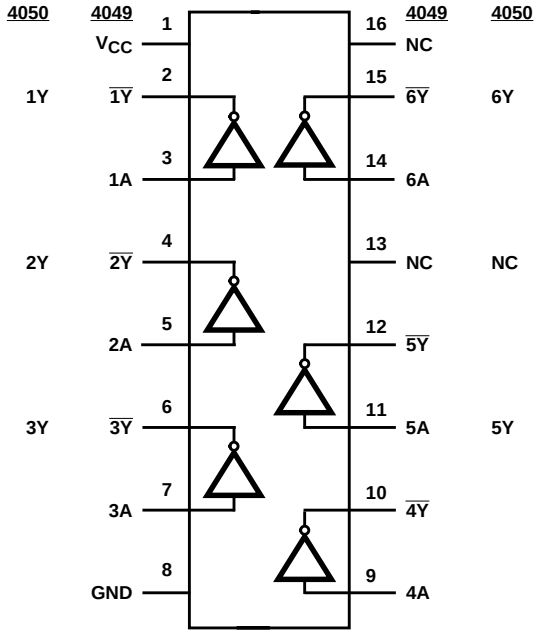
Pinout

CD74HC4049, CD74HC4050
(PDIP, SOIC, TSSOP)
TOP VIEW



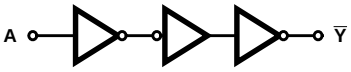
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

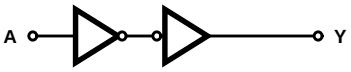


Logic Diagrams

HC4049



HC4050



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . –0.5V to 7V
DC Input Diode Current, I_{IK}
For $V_I < –0.5V$ or $V_I > V_{CC} + 0.5V$ . . . . . ±20mA
DC Output Diode Current, I_{OK}
For $V_O < –0.5V$ or $V_O > V_{CC} + 0.5V$ . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For $V_O > –0.5V$ or $V_O < V_{CC} + 0.5V$ . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

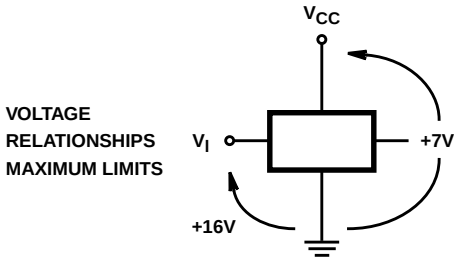
Operating Conditions

Temperature Range (T_A) . . . . . –55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	78
SOIC Package	113
TSSOP Package	149

Maximum Junction Temperature (Hermetic Package or Die) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . –65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)



CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	–40°C TO 85°C MIN	–40°C TO 85°C MAX	–55°C TO 125°C MIN	–55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	–0.02	2	1.9	-	-	1.9	-	1.9	-	V
			–0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			–0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			–4	4.5	3.98	-	-	3.84	-	3.7	-	V
			–5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
		15	-	6	-	-	±0.5	-	±5	-	±5	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	2	-	20	-	40	µA

NOTE: For dual-supply systems theorectical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			−40°C TO 85°C		−55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, nA to n$\overline{Y}$ HC4049 nA to nY HC4050	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	85	-	105	-	130	ns
			4.5	-	-	17	-	21	-	26	ns
			6	-	-	14	-	18	-	22	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	35	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per gate.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

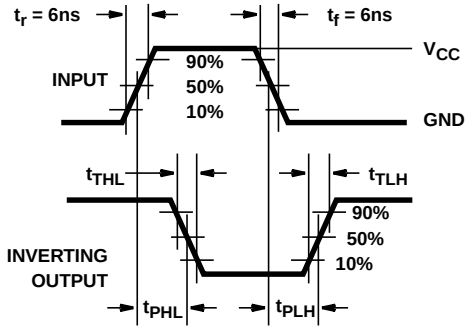


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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