

# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS182E – FEBRUARY 1997 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs

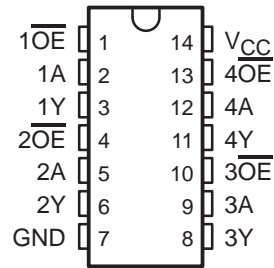
## description

The 'ABT125 quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

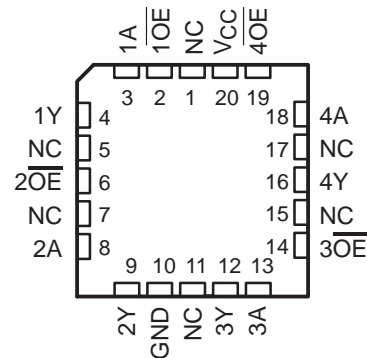
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT125 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT125 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT125 . . . J OR W PACKAGE  
SN74ABT125 . . . D, DB, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each buffer)

| INPUTS          |   | OUTPUT |
|-----------------|---|--------|
| $\overline{OE}$ | A | Y      |
| L               | H | H      |
| L               | L | L      |
| H               | X | Z      |



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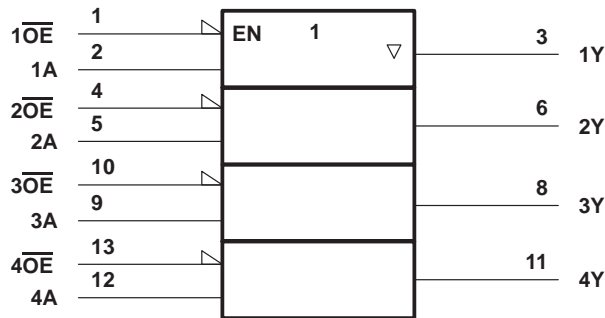
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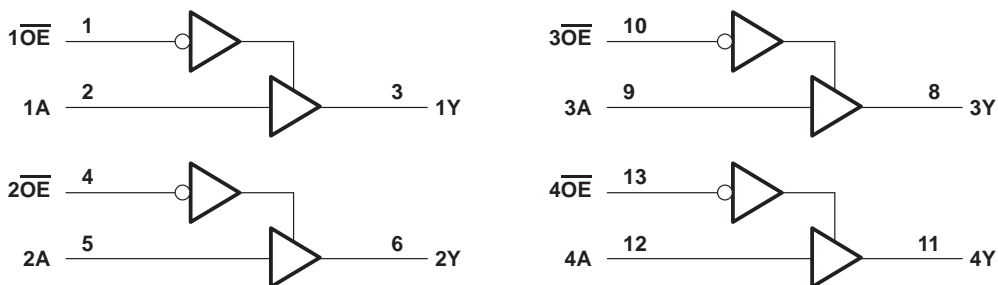
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT125              | 96 mA           |
| SN74ABT125  | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package          | 127°C/W         |
| DB package  | 158°C/W         |
| N package   | 78°C/W          |
| PW package  | 170°C/W         |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

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**recommended operating conditions (see Note 3)**

|                     |                                    | SN54ABT125 |                 | SN74ABT125 |                 | UNIT |
|---------------------|------------------------------------|------------|-----------------|------------|-----------------|------|
|                     |                                    | MIN        | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     | 4.5        | 5.5             | 4.5        | 5.5             | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2          |                 | 2          |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            |            | 0.8             |            | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      | 0          | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | High-level output current          |            | -24             |            | -32             | mA   |
| I <sub>OL</sub>     | Low-level output current           |            | 48              |            | 64              | mA   |
| Δt/Δv               | Input transition rise or fall rate |            | 10              |            | 10              | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 | 200        |                 | 200        |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | -55        | 125             | -40        | 85              | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS   | T <sub>A</sub> = 25°C |      |       | SN54ABT125 |       | SN74ABT125 |       | UNIT |
|---------------------|---|-----------------------|------|-------|------------|-------|------------|-------|------|
|                     |   | MIN                   | TYP† | MAX   | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>IK</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA  |                       |      | -1.2  |            | -1.2  |            | -1.2  | V    |
| V <sub>OH</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA  |                       |      | 2.5   |            | 2.5   |            | 2.5   | V    |
|                     | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA  |                       |      | 3     |            | 3     |            | 3     |      |
|                     | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA   |                       |      | 2     |            | 2     |            |       |      |
| V <sub>OL</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA  |                       |      |       |            | 0.55  |            |       | V    |
|                     |   |                       |      |       |            | 0.55* |            | 0.55  |      |
| V <sub>hys</sub>    |   |                       |      | 100   |            |       |            |       | mV   |
| I <sub>I</sub>      | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                                 |                       |      | ±1    |            | ±1    |            | ±1    | µA   |
| I <sub>OZPU</sub> ‡ | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$                    |                       |      | ±50   |            | ±50   |            | ±50   | µA   |
| I <sub>OZPD</sub> ‡ | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$                    |                       |      | ±50   |            | ±50   |            | ±50   | µA   |
| I <sub>OZH</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2 V$                    |                       |      | 10    |            | 10    |            | 10    | µA   |
| I <sub>OZL</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2 V$                    |                       |      | -10   |            | -10   |            | -10   | µA   |
| I <sub>off</sub>    | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V   |                       |      | ±100  |            |       |            | ±100  | µA   |
| I <sub>CEX</sub>    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high   |                       |      | 50    |            | 50    |            | 50    | µA   |
| I <sub>O</sub> §    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V   | -50                   | -100 | -200¶ | -50        | -200¶ | -50        | -200¶ | mA   |
| I <sub>CC</sub>     | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                  | Outputs high          |      | 1     | 250        | 250   |            | 250   | µA   |
|                     |   | Outputs low           |      | 24    | 30         | 30    |            | 30    | mA   |
|                     |   | Outputs disabled      |      | 0.5   | 250        | 250   |            | 250   | µA   |
| ΔI <sub>CC</sub> #  | Data inputs<br>V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND    | Outputs enabled       |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
|                     |   | Outputs disabled      |      | 0.05  |            | 0.05  |            | 0.05  |      |
|                     | Control inputs<br>V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND |                       |      | 1.5   |            | 1.5   |            | 1.5   |      |
| C <sub>i</sub>      | V <sub>I</sub> = 2.5 V or 0.5 V   |                       |      | 3     |            |       |            |       | pF   |
| C <sub>o</sub>      | V <sub>O</sub> = 2.5 V or 0.5 V   |                       |      | 7     |            |       |            |       | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This limit may vary among suppliers.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER                     | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | SN54ABT125 |     | SN74ABT125 |     | UNIT |
|-------------------------------|-----------------|----------------|---|-----|-----|------------|-----|------------|-----|------|
|                               |                 |                | MIN   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>PLH</sub> <sup>†</sup> | A               | Y              | 1   | 3.2 | 4.6 | 1          | 6   | 1          | 4.9 | ns   |
| t <sub>PHL</sub> <sup>†</sup> |                 |                | 1   | 2.5 | 4.6 | 1          | 6.2 | 1          | 4.9 |      |
| t <sub>PZH</sub> <sup>†</sup> | $\overline{OE}$ | Y              | 1   | 3.6 | 5   | 1          | 6   | 1          | 5.9 | ns   |
| t <sub>PZL</sub> <sup>†</sup> |                 |                | 1   | 2.5 | 6.2 | 1          | 7.5 | 1          | 6.8 |      |
| t <sub>PHZ</sub>              | $\overline{OE}$ | Y              | 1   | 3.8 | 5.4 | 1          | 6.3 | 1          | 6.2 | ns   |
| t <sub>PLZ</sub> <sup>†</sup> |                 |                | 1   | 3.3 | 5.3 | 1          | 6.5 | 1          | 6.2 |      |

<sup>†</sup> This limit may vary among suppliers.

# SN54ABT125, SN74ABT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

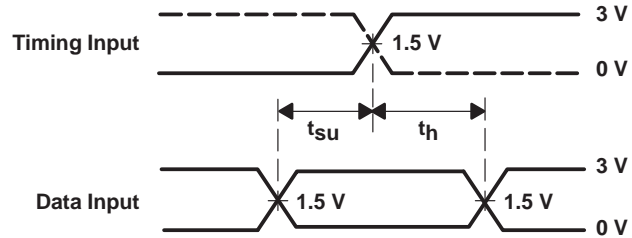


LOAD CIRCUIT

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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