- **Members of the Texas Instruments *Widebus*™ Family**

- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**

- **State-of-the-Art *EPIC-*II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**

- **High-Impedance State During Power Up and Power Down**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162244 . . . WD PACKAGE
SN74ABT162244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		48	2$\overline{OE}$
1Y1	2		47	1A1
1Y2	3		46	1A2
GND	4		45	GND
1Y3	5		44	1A3
1Y4	6		43	1A4
V_{CC}	7		42	V_{CC}
2Y1	8		41	2A1
2Y2	9		40	2A2
GND	10		39	GND
2Y3	11		38	2A3
2Y4	12		37	2A4
3Y1	13		36	3A1
3Y2	14		35	3A2
GND	15		34	GND
3Y3	16		33	3A3
3Y4	17		32	3A4
V_{CC}	18		31	V_{CC}
4Y1	19		30	4A1
4Y2	20		29	4A2
GND	21		28	GND
4Y3	22		27	4A3
4Y4	23		26	4A4
4$\overline{OE}$	24		25	3$\overline{OE}$
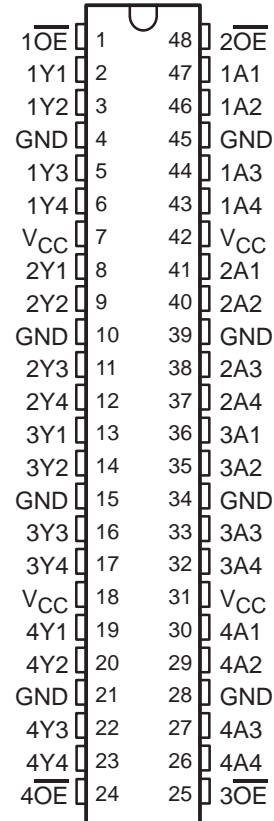
description

The 'ABT162244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162244 is characterized for operation from –40°C to 85°C.

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FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†
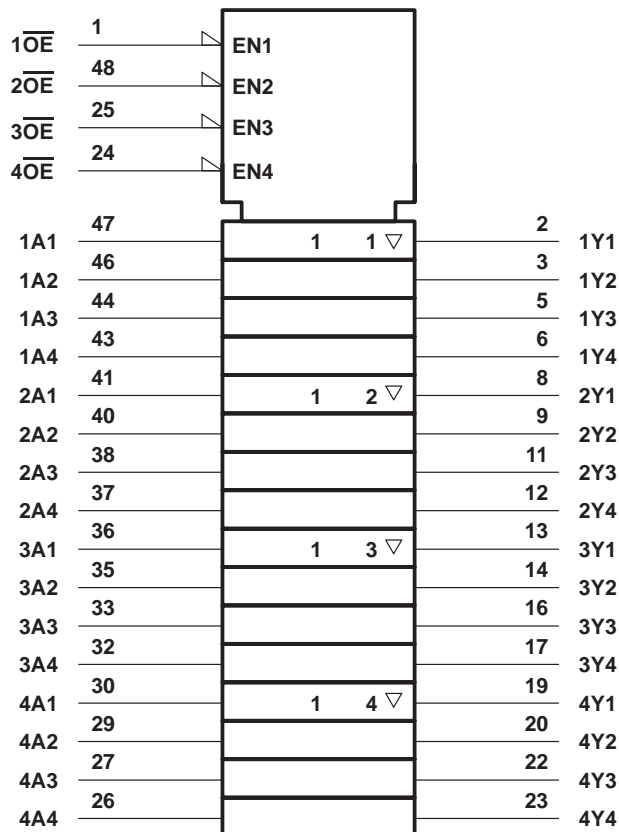
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O .... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) .... –18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 89°C/W
                                                   DGV package .... 93°C/W
                                                   DL package .... 94°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
      2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT162244		SN74ABT162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   Unused inputs must be held high or low to prevent them from floating.

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INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT162244 MIN	MAX	SN74ABT162244 MIN	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA	3.35			3.35		3.35		V
	$V_{CC} = 5$ V,	$I_{OH} = -1$ mA	3.85			3.85		3.85		
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	3.1			3.1		3.1		
		$I_{OH} = -12$ mA	2.6*						2.6	
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA		0.4	0.8		0.8		0.65	V
		$I_{OL} = 12$ mA							0.8	
V_{hys}				100						mV
I_I	$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZPU}‡	$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZPD}‡	$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZH}	$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10		10		10	µA
I_{OZL}	$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				−10		−10		−10	µA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Ouptuts high			50		50		50	µA
I_O§	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−25	−55	−100	−25	−100	−25	−100	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			2		2		2	mA
		Outputs low			30		30		30	
		Outputs disabled			2		2		2	
ΔI_{CC}¶ Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			50		50		50	µA
		Outputs disabled			50		50		50	
Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	
C_i	$V_I = 2.5$ V or 0.5 V			3						pF
C_o	$V_O = 2.5$ V or 0.5 V			8						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ This parameter is characterized, but not production tested.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)
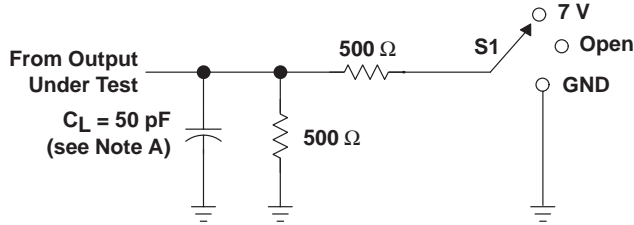
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT162244					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.5	3.6	1	4.1	ns
t_{PHL}			1	3.1	4.7	1	5.3	
t_{PZH}	$\overline{OE}$	Y	1	3.2	4.8	1	5.6	ns
t_{PZL}			1	3.2	4.7	1	5.5	
t_{PHZ}	$\overline{OE}$	Y	1	3.2	5.3	1	6.3	ns
t_{PLZ}			1	3.1	4.6	1	4.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT162244					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.5	3.2	1	3.9	ns
t_{PHL}			1	3.1	4	1	4.8	
t_{PZH}	$\overline{OE}$	Y	1	3.2	4.2	1	5.4	ns
t_{PZL}			1	3.2	4.1	1	5.1	
t_{PHZ}	$\overline{OE}$	Y	1	3.2	4	1	4.6	ns
t_{PLZ}			1	3.1	3.9	1	4.5	

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PARAMETER MEASUREMENT INFORMATION

From Output Under Test

$C_L = 50$ pF (see Note A)

500 Ω

S1

7 V
Open
GND

500 Ω

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

Timing Input — 3 V, 1.5 V, 0 V

t_{su} t_h

Data Input — 3 V, 1.5 V, 1.5 V, 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input — t_W — 3 V, 1.5 V, 1.5 V, 0 V
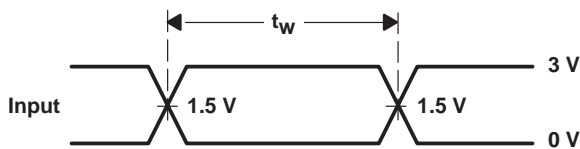
VOLTAGE WAVEFORMS
PULSE DURATION

Input — 3 V, 1.5 V, 1.5 V, 0 V

t_{PLH} t_{PHL}

Output — V_{OH}, 1.5 V, 1.5 V, V_{OL}

t_{PHL} t_{PLH}

Output — V_{OH}, 1.5 V, 1.5 V, V_{OL}
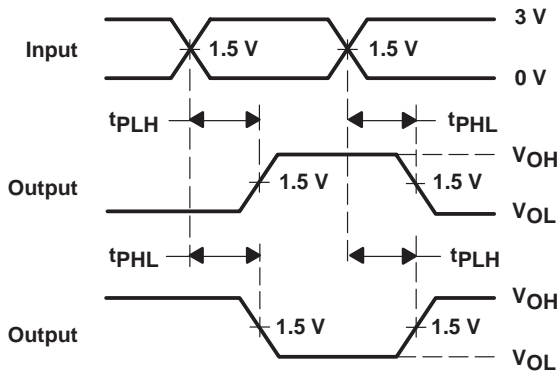
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Output Control — 3 V, 1.5 V, 1.5 V, 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at 7 V (see Note B) — 3.5 V, 1.5 V, V_{OL} + 0.3 V, V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at Open (see Note B) — V_{OH}, 1.5 V, V_{OH} − 0.3 V, ≈ 0 V
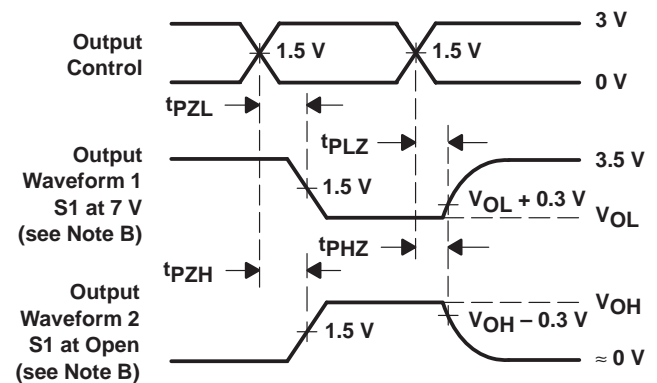
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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