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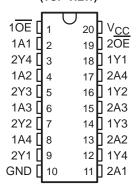
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Current Outputs Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

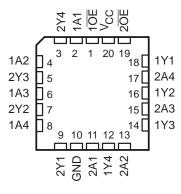
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 devices are organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN54HCT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT240 is characterized for operation from –40°C to 85°C.

SN54HCT240 . . . J OR W PACKAGE SN74HCT240 . . . DW, N, OR PW PACKAGE (TOP VIEW)



SN54HCT240 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE (each buffer/driver)

INP	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	н
Н	Χ	Z

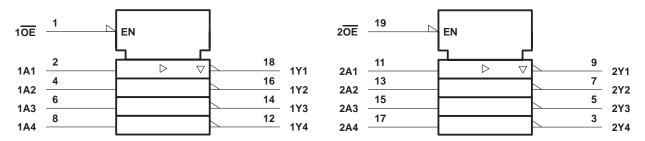


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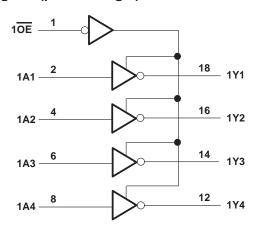
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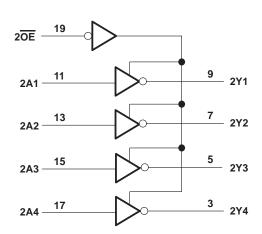
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V _{CC}		0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see	ee Note 1)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	c) (see Note 1)	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		±35 mA
Continuous current through V _{CC} or GND		±70 mA
Package thermal impedance, θ _{JA} (see Note 2)	: DW package	58°C/W
-	N package	69°C/W
	PW package	83°C/W
Storage temperature range, T _{stg}		

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

			SN54HCT240			SN74HCT240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
t _t	Input transition (rise and fall) time		0		500	0		500	ns
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VCC	T _A = 25°C			SN54HCT240		SN74HCT240		UNIT
PARAMETER	TEST CO	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
VOH	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V
VOH	VI = VIH OI VIL	$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		V
Voi	VI = VIH or VIL	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
VOL	AI = AIH OL AIL	I _{OL} = 6 mA			0.17	0.26		0.4		0.33	
lį	VI = VCC or 0		5.5 V		±0.1	±100		±1000		±1000	nA
loz	$V_O = V_{CC}$ or 0,	VI = VIH or VIL	5.5 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0,	I _O = 0	5.5 V			8		160		80	μΑ
ΔI _{CC} †	One input at 0.5 V one of the of the order o	*	5.5 V		1.4	2.4		3		2.9	mA
Ci			4.5 V to 5.5 V		3	10		10		10	pF

This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то		м то		T,	Վ = 25° C	;	SN54H	CT240	SN74H	CT240	UNIT
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN TYP	TYP	MAX	MIN	MAX	MIN	MAX	ONII		
	۸	Y	4.5 V		13	25		37		32	nc		
ъра	^t pd A	Y	T I	T T	5.5 V		12	23		33		29	ns
	OE Y	4.5 V		21	35		53		44	20			
^t en		ľ	5.5 V		19	32		48		40	ns		
+			Y	4.5 V		19	35		53		44	ns	
^t dis	OE	1	ı	5.5 V		18	32		48		40	110	
4.		V	4.5 V		8	12		18		15	ns		
t _t		1	5.5 V		7	11		16		14	110		



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switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

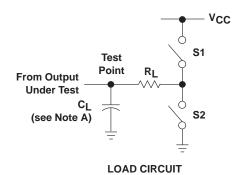
PARAMETER	FROM	то	Vaa	T,	ղ = 25°C	;	SN54H	CT240	SN74H	CT240	UNIT												
PARAMETER	(INPUT)	(OUTPUT)	VCC	VCC MIN TY	TYP	MAX	MIN	MAX	MIN	MAX	UNIT												
+ .	Δ.	V	4.5 V		20	42		63		53	no												
^t pd	A	T I	' ['	'	'	'	ı	'	'	'	'	ı	ľ	5.5 V		19	38		56		48	ns
		Υ	4.5 V		25	52		79		65													
t _{en}	OE		ı	5.5 V		22	47		71		59	ns											
t _t			V	4.5 V		17	42		63		53	no											
		T T	5.5 V		14	38		57		48	ns												

operating characteristics, $T_A = 25^{\circ}C$

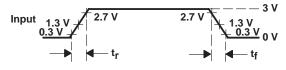
	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	40	pF

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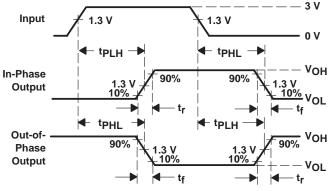
PARAMETER MEASUREMENT INFORMATION

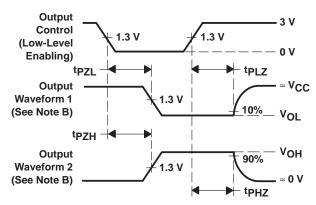


PARAMETER		RL	CL	S 1	S2	
	^t PZH	1 kΩ	50 pF		Closed	
^t en	tPZL	1 K22	150 pF	Closed	Open	
.	teles the telescope teles		50 pF	Open	Closed	
^t dis	tPLZ	1 K22	30 pr	Closed	Open	
t _{pd} or t _t		ı	50 pF or 150 pF	Open	Open	



VOLTAGE WAVEFORM INPUT RISE AND FALL TIMES





VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z $_{O}$ = 50 $\Omega,$ t_{f} = 6 ns, t_{f} = 6 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tp7I and tp7H are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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