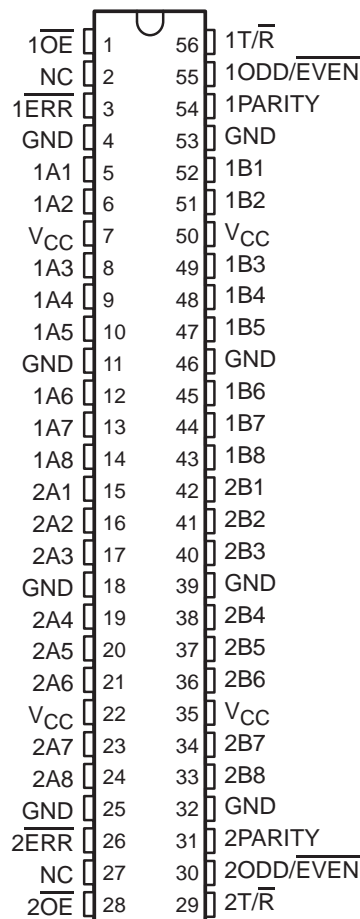


# 54ACT16657, 74ACT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16657 . . . WD PACKAGE  
74ACT16657 . . . DL PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'ACT16657 contain two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive (1T/R or 2T/R) input determines the direction of data flow. When 1T/R (or 2T/R) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/R (or 2T/R) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable (1OE or 2OE) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/EVEN (or 2ODD/EVEN) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/EVEN (or 2ODD/EVEN) input. For example, if 1ODD/EVEN is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.



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**16-BIT TRANSCEIVERS**  
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**description (continued)**

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the  $1\overline{\text{ERR}}$  (or  $2\overline{\text{ERR}}$ ) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if  $1\text{ODD}/\overline{\text{EVEN}}$  is high (odd parity selected),  $1\text{PARITY}$  is high, and there are three high bits on the 1B bus, then  $1\overline{\text{ERR}}$  is low, indicating a parity error.

The 74ACT16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16657 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT16657 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

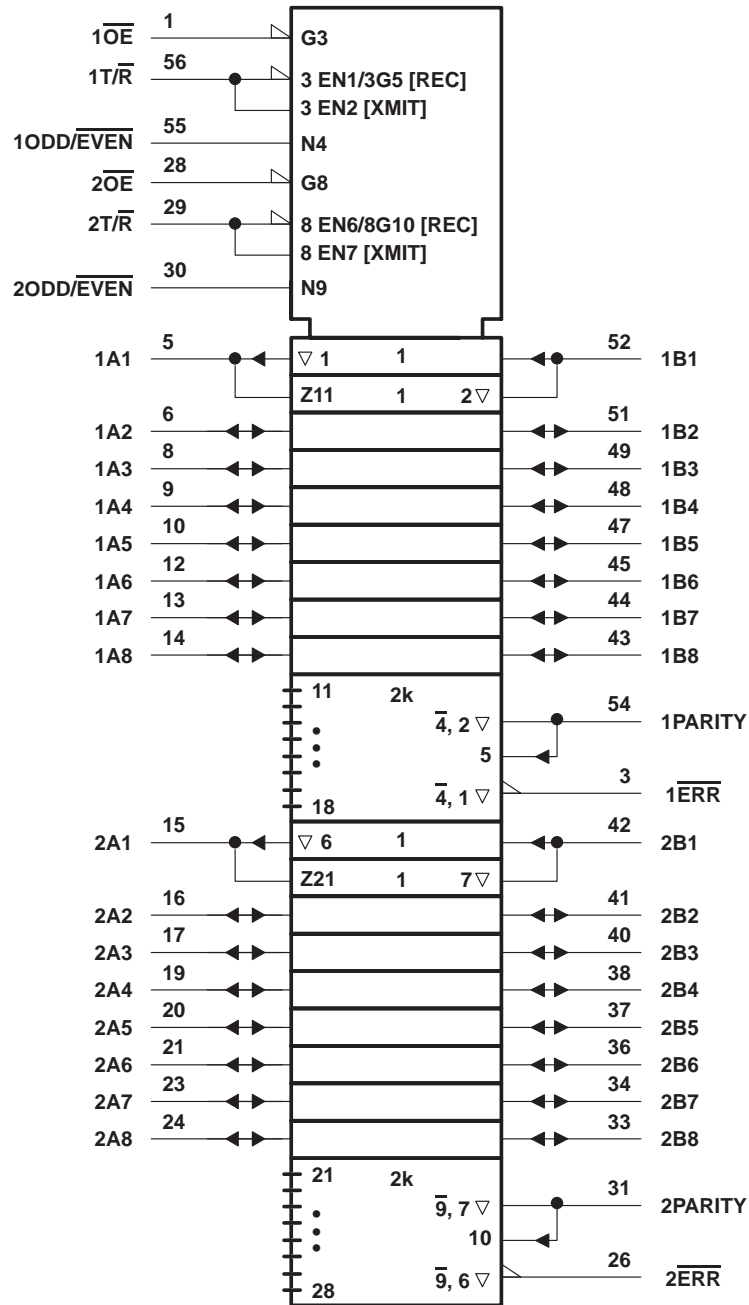
**FUNCTION TABLE**

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{\text{OE}}$	$\text{T}/\overline{\text{R}}$	$\text{ODD}/\overline{\text{EVEN}}$		$\overline{\text{ERR}}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z



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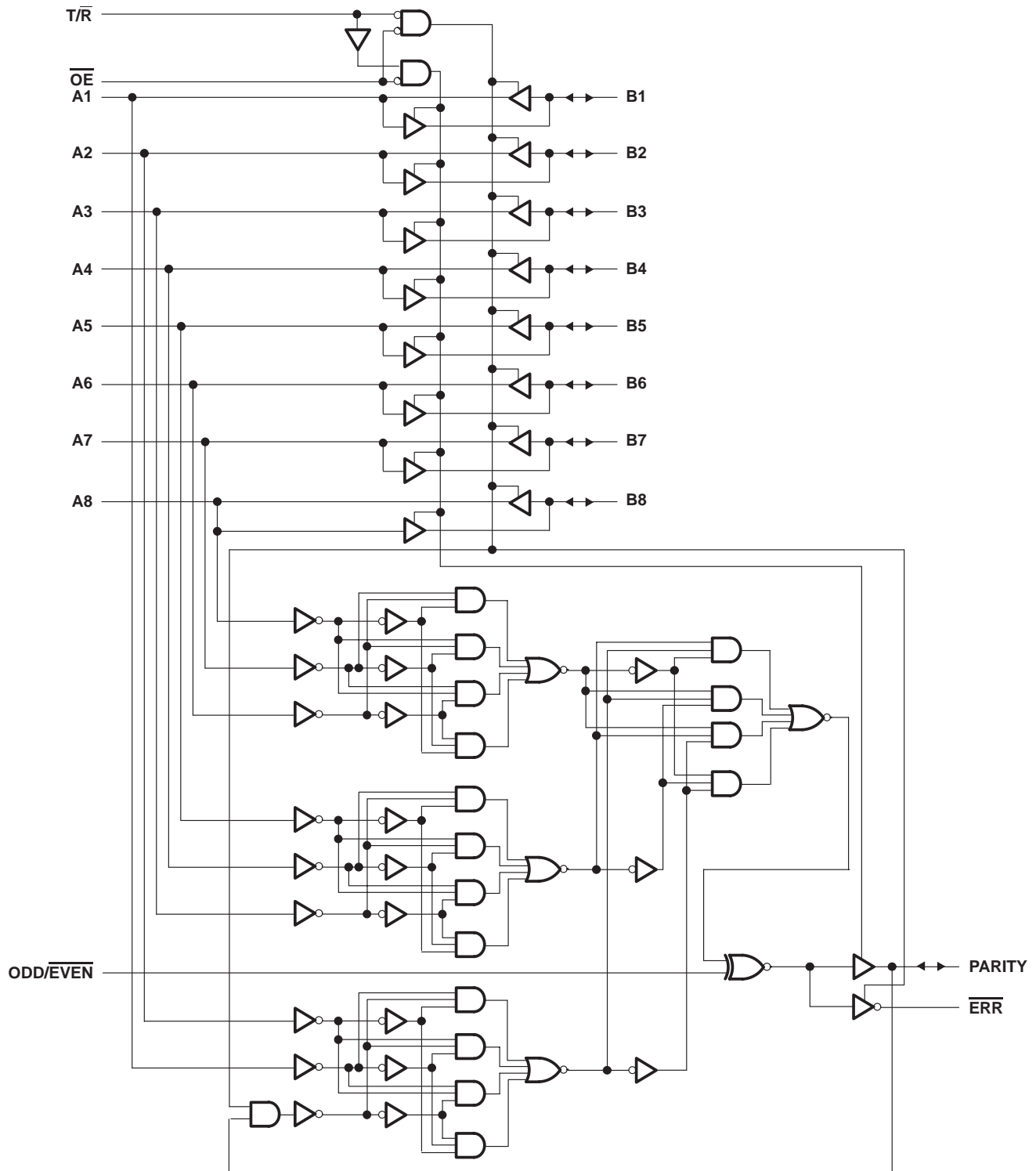
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram, each transceiver (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 500$ mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**recommended operating conditions (see Note 3)**

	54ACT16657			74ACT16657			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_I$ Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$ High-level output current			-24			-24	mA
$I_{OL}$ Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$ Operating free-air temperature	-55		125	-40		85	$^\circ\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT16657		74ACT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
I <sub>OH</sub> = -75 mA†	5.5 V				3.85		3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	0.1			0.1		0.1		V
		5.5 V	0.1			0.1		0.1		
	I <sub>OL</sub> = 24 mA	4.5 V	0.36			0.44		0.44		
		5.5 V	0.36			0.44		0.44		
I <sub>OL</sub> = 75 mA†	5.5 V				1.65		1.65			
I <sub>I</sub>	A or B ports	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		±1	μA
I <sub>OZ</sub> ‡	Control inputs	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.5			±5		±5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			80		80	μA
ΔI <sub>CC</sub> §		One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V	0.9			1		1	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5						pF
C <sub>o</sub>	$\overline{\text{ERR}}$	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	11						pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54ACT16657		74ACT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	4.1	7.3	9.6	4.1	10.7	4.1	10.7	ns
t <sub>PHL</sub>			3.2	6.8	9.8	3.2	10.6	3.2	10.6	
t <sub>PLH</sub>	A	PARITY	4	8.6	12.9	4	14.3	4	14.3	ns
t <sub>PHL</sub>			4.3	9	13.1	4.3	14.3	4.3	14.3	
t <sub>PLH</sub>	ODD/ $\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	3.7	8.3	12.3	3.7	13.7	3.7	13.7	ns
t <sub>PHL</sub>			4.1	8.8	12.8	4.1	14.1	4.1	14.1	
t <sub>PLH</sub>	B	$\overline{\text{ERR}}$	3.9	8.6	13	3.9	14.6	3.9	14.6	ns
t <sub>PHL</sub>			4.3	9	13.3	4.3	14.7	4.3	14.7	
t <sub>PLH</sub>	PARITY	$\overline{\text{ERR}}$	3.8	8.4	12.2	3.8	13.8	3.8	13.8	ns
t <sub>PHL</sub>			4.1	8	12.8	4.1	14.2	4.1	14.2	
t <sub>PZH</sub>	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	2.6	6.1	10.1	2.6	11.3	2.6	11.3	ns
t <sub>PZL</sub>			3.2	7.2	11.7	3.2	13	3.2	13	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	5.9	8.6	10.5	5.9	11.2	5.9	11.2	ns
t <sub>PLZ</sub>			5.3	8	9.8	5.3	10.5	5.3	10.5	

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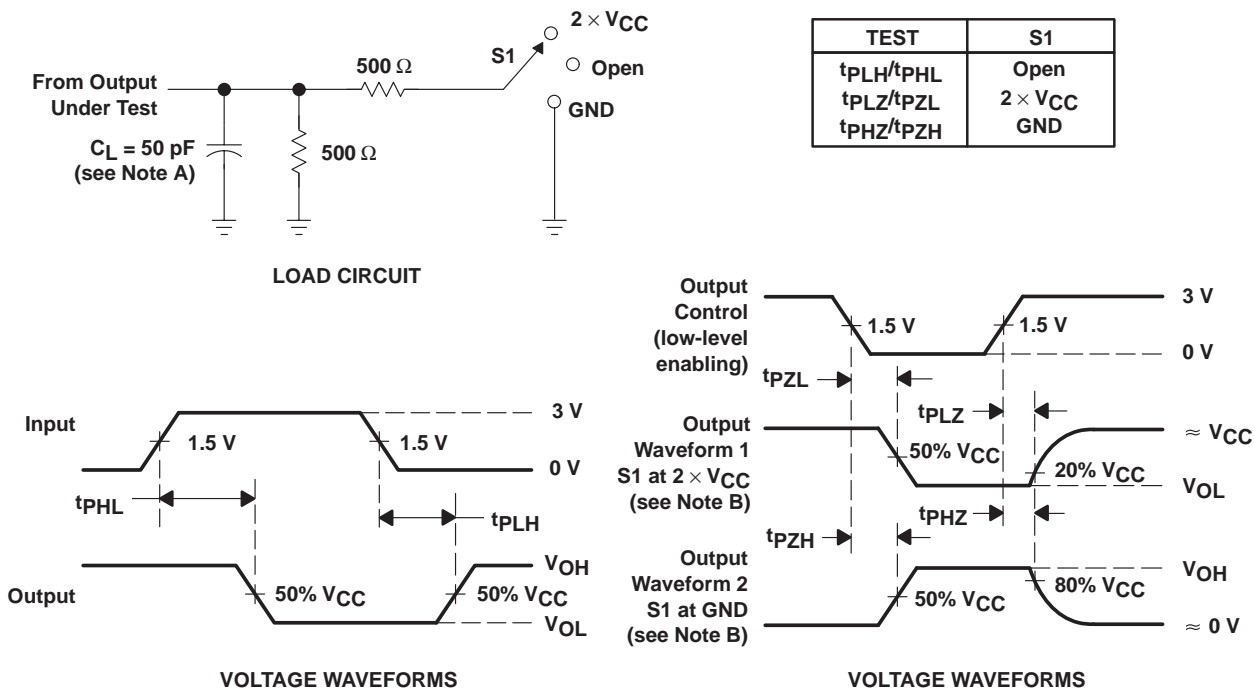
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	76	pF
		Outputs disabled	35	

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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